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RESEARCH ARTICLE

Native GaN/GaO_x Heterostructure Platform for Wafer-Scale Integration of High-Performance Complementary Transistors

Jinhua Liang[1,2], Chi Liu[1,2*], Yuning Wei[1,2], Shun Feng[1,2], Yun Sun[1,2], Yutaka Ohno[3], Hui-Ming Cheng[1,2,4], and Dong-Ming Sun[1,2*]

[1]Shenyang National Laboratory for Materials Science, Institute of Metal Research, Chinese Academy of Sciences, Shenyang 110016, China. [2]School of Materials Science and Engineering, University of Science and Technology of China, Shenyang 110016, China. [3]Department of Quantum Engineering, Nagoya University, Nagoya 464-8603, Japan. [4]Faculty of Materials Science and Engineering/Institute of Technology for Carbon Neutrality, Shenzhen Institute of Advanced Technology, Chinese Academy of Sciences, Shenzhen 518000, China.

*Address correspondence to: chiliu@imr.ac.cn (C.L.); dmsun@imr.ac.cn (D.-M.S.)

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The drive for complementary transistors with ultra-steep subthreshold swing (SS) and minimal power consumption has intensified interest in integrating low-dimensional semiconductors with wide-bandgap materials, as silicon scaling approaches its physical limits in the post-Moore era. A central bottleneck, however, lies in dielectric/semiconductor interface engineering: existing strategies based on van der Waals transfer or nonnative dielectric deposition compromise interface quality, wafer-scale uniformity, and process compatibility, preventing practical large-scale integration. Here, we demonstrate a previously unexplored in situ oxidation strategy that directly forms a high-κ gallium oxide (GaO_x) dielectric on heavily doped n-type gallium nitride (GaN) substrates, enabling high-performance, energy-efficient complementary inverters based on n-type molybdenum disulfide (MoS_2) and p-type carbon nanotube transistors. Leveraging the excellent dielectric properties of the GaN/GaO_x heterostructure, MoS_2 field-effect transistors achieve an interface trap density of 1.18×10^{11} cm^{-2} eV^{-1}, an SS at the thermionic limit of 60 mV dec^{-1}, an on/off ratio above 10^8 at 0.87 V, and a voltage gain of 134.5 at 2 V for inverters. These results establish GaN/GaO_x as a native, scalable, and complementary metal-oxide-semiconductor-compatible integration platform, offering a transformative route toward wafer-scale, low-power electronics in the post-Moore era.

Introduction

In the post-Moore era, as the scaling of traditional silicon-based transistors approaches its fundamental physical limits, severe short-channel effects lead to sharply increased off-state current and power dissipation, which severely constrain the further enhancement of integrated circuit performance [1–5]. The development of novel complementary transistors with an ultra-steep subthreshold swing (approaching the theoretical limit of 60 mV dec^{-1}) and ultralow static power consumption has consequently emerged as a critical challenge. The wide-bandgap semiconductor gallium nitride (GaN), known for its high breakdown field strength, high electron mobility, and excellent thermal stability, provides a highly promising platform for heterogeneous integration with emerging low-dimensional materials such as molybdenum disulfide (MoS_2) and carbon nanotubes (CNTs), whose atomic-scale thickness enables superior gate controllability and suppressed off-state leakage current. This material system presents a compelling route to simultaneously achieve superior gate controllability, high carrier mobility, and intrinsically low power consumption, opening new possibilities for next-generation integrated electronics [6–10]. However, a major bottleneck in this integration scheme lies in the poor control over the interface quality between low-dimensional materials and dielectric layers [11–13]. Conventional atomic layer deposition (ALD) of high-κ dielectrics (Al_2O_3 and HfO_2) often suffers from nonuniform nucleation on 2-dimensional (2D) material surfaces due to the lack of surface dangling bonds, leading to inferior interface quality that degrades subthreshold characteristics and operational stability at scaled equivalent oxide thickness (EOT) [14,15]. To address this interfacial challenge, several integration strategies have been explored, including transferred van der Waals dielectrics (such as HfO_x and h-BN) [16–18], molecular buffer interlayers (such as Sb_2O_3 and 3,4,9,10-perylene-tetracarboxylic dianhydride [PTCDA]) [19–21], and epitaxially grown crystalline dielectrics (such as CaF_2) [22] via molecular beam epitaxy. While these approaches have yielded quantifiable improvements in interface quality, their practical application is often constrained by inherent technical limitations, such as difficulties in achieving thickness uniformity in van der Waals dielectrics and the incompatibility of high-temperature epitaxial growth processes with standard CMOS technology, which hinders the

wafer-scale uniformity and process compatibility required for reliable large-scale integration in post-Moore electronics.

Here, we propose an innovative strategy of in situ growth: through controlled thermal oxidation of heavily doped n-type GaN substrates, a high-quality, high-κ gallium oxide (GaO_x) dielectric layer is directly generated on the GaN surface. This method leverages the innate properties of GaN to construct a high-performance GaN/GaO_x heterostructure platform with excellent dielectric properties. MoS_2 field-effect transistors (FETs) fabricated on this GaO_x dielectric show an interface state density as low as 1.18×10^{11} cm^{-2} eV^{-1} and a small subthreshold swing of 60 mV dec^{-1}. The GaN/GaO_x heterostructure platform is also compatible with high-performance p-type CNT FETs. Fabricated complementary inverters integrating n-type MoS_2 and p-type CNT transistors achieve a maximum voltage gain of 134.5 at a supply voltage of 2 V, which demonstrates the potential of this technology for future low-power integrated circuits.

Results

Device design and characterization

Figure 1A shows the schematic diagram of an MoS_2 transistor with a back-gate stack of MoS_2/GaO_x/GaN, where the GaO_x dielectric is prepared by thermal oxidation of the GaN substrate. A 30-nm-thick Al_2O_3 is used as the isolation layer. The Ti/Al/Ti/Au stack serves as the gate electrode and enables an ohmic contact with the GaN substrate (Fig. S1), while graphene is used as source and drain electrodes [23]. Detailed fabrication processes are shown in Figs. S2 and S3. The cross-sectional transmission electron microscopy (TEM) image of the gate stack clearly reveals a uniform 3.2-nm-thick GaO_x dielectric with atomically flat surfaces (Fig. 1B), while the elemental mapping (Fig. 1C) and the Raman spectra (Fig. S4) collectively confirm the gate stack composition. This high-quality GaN/GaO_x heterostructure platform enables exceptional MoS_2 transistor performance, including a large on/off ratio over 10^8, a small gate leakage current below 100 fA, and a near-ideal subthreshold swing (SS) of 60 mV dec^{-1} in double-sweep transfer characteristic curves (Fig. 1D).

High-κ GaO_x dielectric layer

The GaO_x dielectric layer is fabricated through thermal oxidation of GaN in an oxygen-rich environment. During this process, oxygen atoms progressively replace nitrogen atoms in the surface layers, forming GaO_x with tiny-grained oxide while

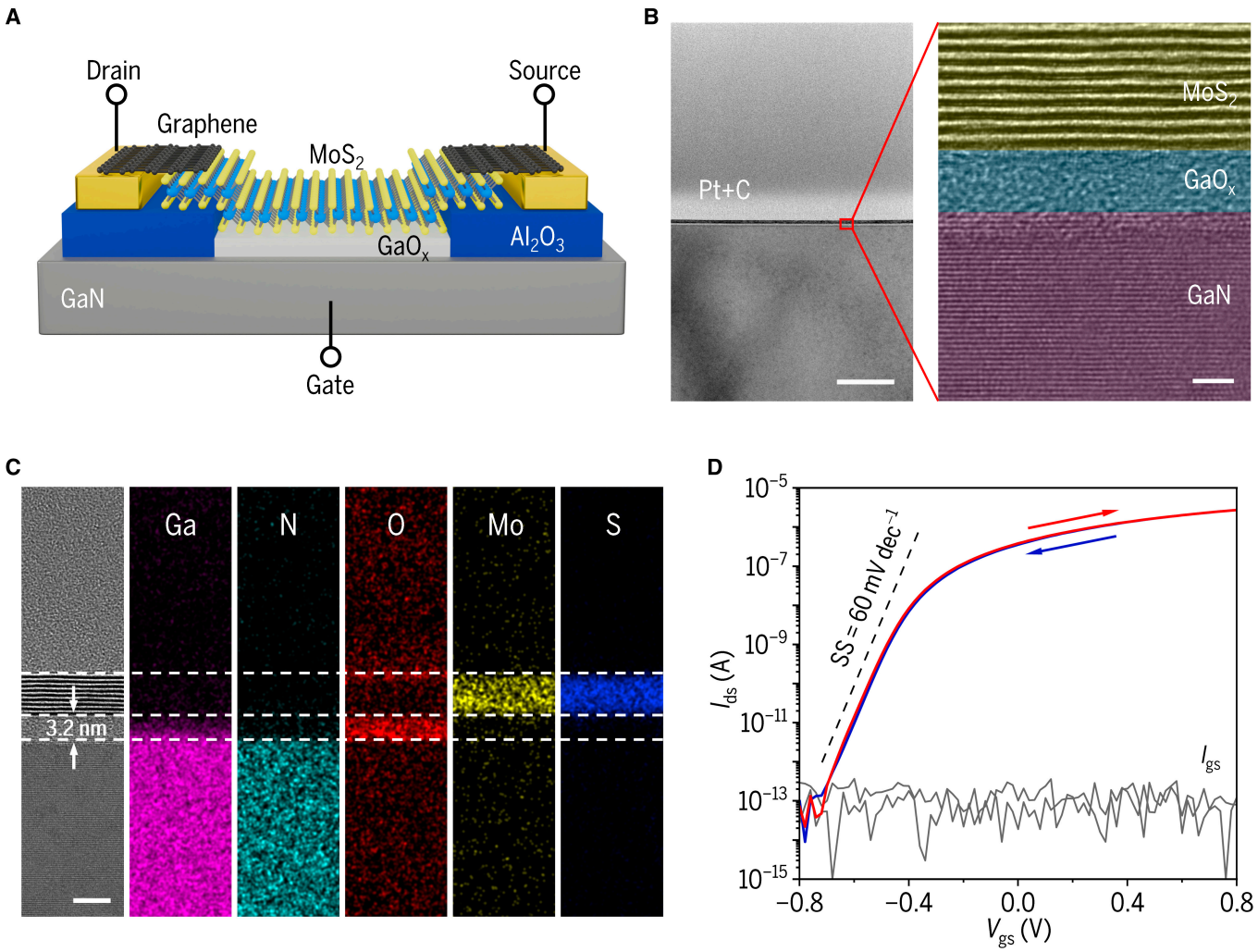


Fig. 1. Design and fabrication of device. (A) Schematic diagram of the MoS_2 transistor. (B) Cross-sectional TEM image of the MoS_2/GaO_x/GaN heterostructure showing a high-quality interface between MoS_2 and GaO_x (left scale bar: 100 nm, right scale bar: 2 nm). (C) TEM image with corresponding elemental mappings of Ga, N, O, Mo, and S, respectively (scale bar: 5 nm). (D) Double-sweep transfer characteristic curves of the MoS_2 transistor with a constant V_{ds} of 1 V, featuring a channel length of 20 μm and a width of 5 μm.

releasing NO_x gas (Fig. 2A and B) [24–26]. Importantly, this thermal oxidation process enables wafer-scale production of GaO_x dielectrics (Fig. 2C). X-ray photoelectron spectroscopy (XPS) is used to analyze the chemical composition of the GaO_x film. The experimental Ga $2P_{3/2}$ core-level spectrum is well-fitted by both Ga-N and Ga-O bonding configurations (Fig. 2D), confirming the formation of Ga-O components in the dielectric while residual Ga-N signatures remain detectable due to the ultrathin nature of the dielectric [27,28]. Consistent conclusions are obtained from the Ga 3d core-level spectrum (Fig. S5). Complementary measurements of secondary ion mass spectrometry (SIMS) further verify that the dielectric layer consists of pure Ga-O bonding, with negligible Ga-N content (Fig. S6). Atomic force microscopy (AFM) characterization demonstrates that the GaO_x dielectric exhibits exceptional uniformity and flatness at the micrometer scale, showing no discernible surface protrusions or holes (Fig. 2E). The high-quality interface enables the GaO_x dielectric to achieve complete insulation below 2 V (Fig. 2F and Fig. S7).

The dielectric constant of the GaO_x dielectric is characterized by an AFM-based PeakForce TUNA technology, which has been widely used to measure the dielectric properties of ultrathin materials [29,30]. A schematic diagram of the measurement is illustrated in Fig. 2G. Current–voltage (I–V) characteristics are measured by applying a sweeping bias voltage to the sample. The curve demonstrates that the GaO_x film is completely insulated

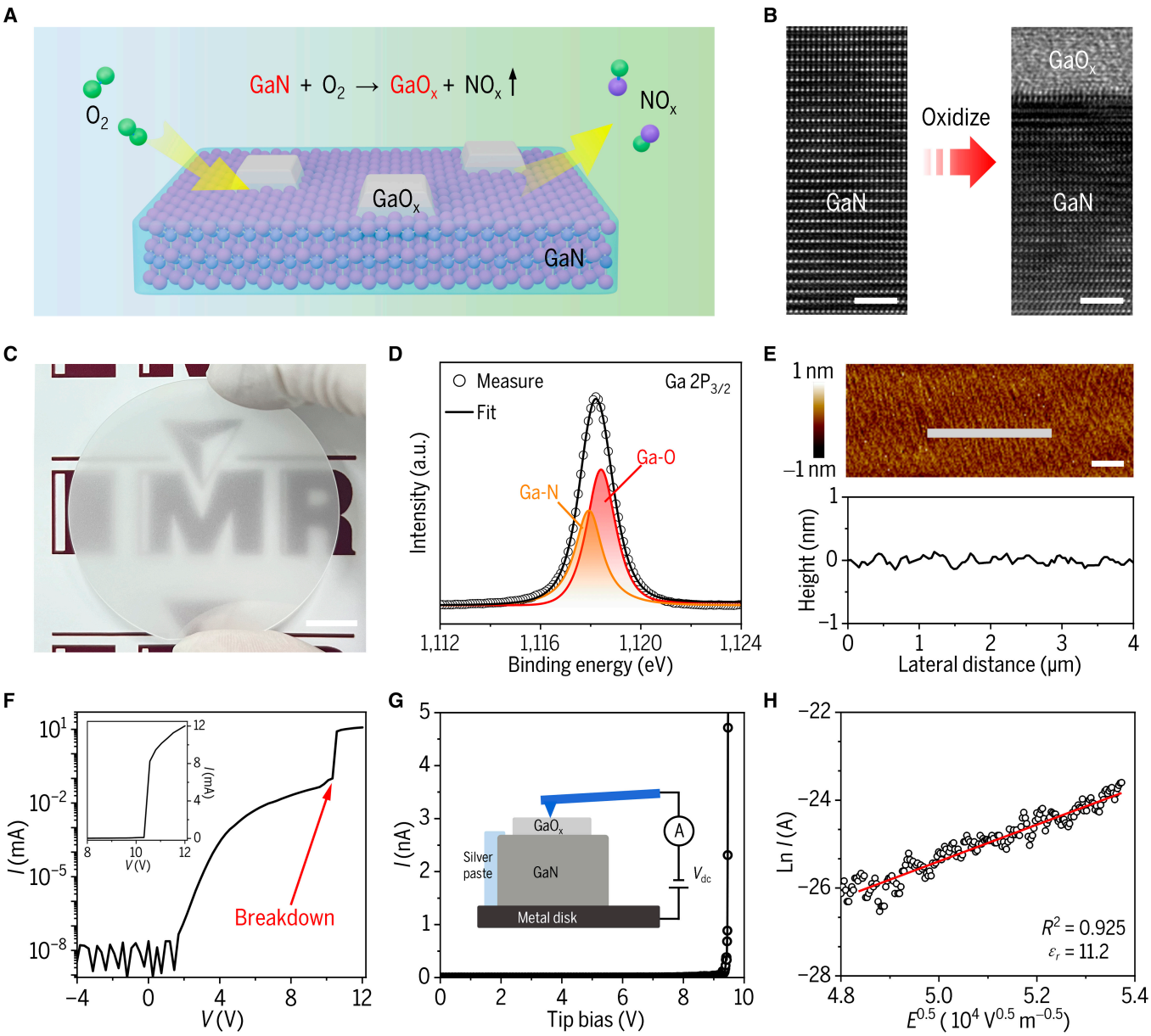


Fig. 2. Preparation and property of GaO_x dielectric. (A) Schematic diagram of GaO_x formation mechanism via thermal oxidation of the GaN (0001) substrate. (B) Cross-sectional TEM image of the in situ grown GaO_x dielectric on GaN substrate (scale bar: 2 nm). (C) Optical image of a 2-inch wafer with uniform GaO_x film (scale bar: 1 cm). (D) High-resolution XPS spectra of Ga $2P_{3/2}$ core level for the GaO_x dielectric (prepared at 300 °C for 60 min), fitted by Ga-N (low-intensity) and Ga-O (high-intensity) bonding states. (E) AFM image of the GaO_x dielectric (scale bar: 1 μm) and corresponding height profile. (F) Current leakage and breakdown characteristics of the GaO_x film. (G) Current–voltage (I–V) characteristics of the GaO_x layer. Inset: Schematic diagram of the setup for the peak force tunneling AFM (PF-TUNA) measurement. (H) Schottky emission model fitting of I–V data for dielectric constant extraction.

below 7.7 V, and the breakdown point where the current rises above the machine noise level is about 9.3 V. Using the Schottky emission model to fit and analyze the results, we calculate a dielectric constant of 11.2 for the GaO_x layer, corresponding to an EOT of 1.1 nm (Fig. 2H). In addition, repetitive measurements across multiple locations on the same sample and different samples are conducted, and similar results confirm the excellent uniformity of the GaO_x dielectric (Fig. S8). We also conduct Au/GaO_x/GaN MOSCAP measurements with double sweep at different frequencies and scan rates, and the observation of negligible hysteresis under all test conditions confirms the exceptional stability and reliability of the GaO_x dielectric layer (Fig. S9).

The effects of oxidation temperature (200 to 500 °C) and time were examined to clarify their role in the dielectric formation mechanism [31,32]. XPS analysis shows progressive shifts of the Ga $2P_{3/2}$ and Ga 3d peaks toward higher binding energies by 0.14 and 0.16 eV (Fig. S10) with concurrent bandgap reduction from 4.9 to 4.8 eV (Fig. S11), confirming temperature-dependent oxidation. The insulation performance of the GaO_x dielectric is highly dependent on the thermal activation process. Insufficient treatment (low temperature/short time) results in incomplete oxidation, whereas excessive conditions (high temperature/prolonged time) generate numerous grain boundaries. These grain boundaries serve as leakage pathways for carriers, and both extremes ultimately degrade the insulation properties, as evidenced in Figs. S12 and S13.

High-performance MoS_2 transistor

Owing to the high-quality interface and small EOT of the GaO_x dielectric, the MoS_2 transistors fabricated on a GaN/GaO_x heterostructure platform exhibit excellent electrical characteristics, including high on/off current ratios at different drain voltages, especially a high on/off current ratio over 10^8 under an operating voltage of 0.87 V when $V_{ds} = 0.5$ V (Fig. 3A and B). Similar excellent performance is also demonstrated in other devices (Fig. S14).

Additionally, negligible hysteresis (~7 mV) is observed in the reverse gate voltage scan, which is slightly influenced by the sweeping speed (Fig. 3C), signifying the high-quality MoS_2/GaO_x interface with a low interface state density (D_{it}). The D_{it} can be evaluated using the equation [17,33]:

$$D_{it} = \frac{C_G}{q}\left(\frac{qSS}{k_B T \ln 10} - 1\right) \quad (1)$$

where C_G is the capacitance per unit area of the gate, SS is the subthreshold swing, q is the elementary charge of the electron, k_B is the Boltzmann constant, and T is the temperature in kelvin. A D_{it} as low as 1.18×10^{11} cm^{-2} eV^{-1} is evaluated. Furthermore, both the multiple switching cycle tests and the bias stress stability tests confirm the superior interface quality of the GaO_x dielectric layer, as evidenced by a negligible threshold voltage shift ($\Delta V_{th} < 10$ mV) in the MoS_2 transistors (Figs. S15 and S16).

To benchmark the performance of our device, the key parameters such as D_{it}, SS, and on/off ratio are compared with the state-of-the-art MoS_2 transistors employing various dielectric integration strategies (Fig. 3D and E). These strategies encompass several established methods, including direct ALD of Al_2O_3 or ZrO_2, molecular-layer-assisted ALD with Sb_2O_3 or PTCDA, material oxidation, and the transfer of van der Waals dielectrics like BN or $SrTiO_3$. In contrast, the GaN/GaO_x heterostructure platform adopted in this work exhibits an ultralow D_{it} (1.18×10^{11} cm^{-2} eV^{-1}), enabling superior device characteristics: a near-ideal subthreshold swing of 60 mV dec^{-1} and a high on/off ratio of 10^8 at ultralow operating voltages. These results underscore the exceptional interface quality of the MoS_2/GaO_x heterostructure, highlighting its marked potential for future low-power 2D device applications.

MoS_2 and CNT transistor arrays

To investigate the potential applications of the GaN/GaO_x heterostructure platform, we have fabricated the FET arrays based on large-area monolayer CVD MoS_2 and wafer-scale GaN/GaO_x heterostructure platform (Fig. 4A), following similar fabrication procedures with the transistors of exfoliated MoS_2 (further details are provided in Fig. S2). The CVD MoS_2 FETs exhibit excellent consistency in transfer characteristic curves at different channel lengths (Fig. S17) under a V_{ds} of −0.5 V (Fig. 4B and C).

While the MoS_2 transistor arrays exhibit excellent n-type characteristics (on/off ratio over 10^7, subthreshold swing ~ 60 mV dec^{-1}), it is equally imperative to realize high-performance p-type devices for the development of complementary logic architectures. One-dimensional (1D) CNTs, with their inherent hole-transport superiority and compatibility with low-temperature processing, serve as an ideal counterpart to match with n-type MoS_2 (Fig. S18). Additionally, CNT films are compatible with uniform and scalable fabrication processes, enabling the deposition of high-quality, highly homogeneous thin films over large areas. This capability provides a reliable material foundation for the mass production of high-performance electronic devices (Fig. S19). Utilizing this GaN/GaO_x heterostructure platform, we successfully fabricated CNT transistor arrays and conducted comprehensive electrical characterization of 30 devices with identical channel lengths ($L = 30$ μm) at $V_{ds} = -1$ V (Fig. 4D and E). The CNT transistors show improved gate control (Fig. S20) with GaO_x dielectric. Statistical analysis of threshold voltages (V_{th}) for both MoS_2 and CNT transistors exhibits narrow Gaussian distributions (Fig. 4F), confirming the excellent uniformity and reproducible fabrication of the GaN/GaO_x heterostructure platform with different semiconductor materials.

Complementary inverter

As the fundamental building block of CMOS circuits, the voltage transfer characteristics (voltage gain) of inverters are intrinsically governed by the electrostatic control capability of the dielectric layer.

In this work, we successfully employed high-κ GaO_x as the gate dielectric to achieve co-integration of n-type MoS_2 and p-type CNT transistors on a GaN/GaO_x heterostructure platform. This strategy demonstrates excellent electrical matching performance and enables the fabrication of complementary inverters (Fig. 5A and B). The voltage transfer characteristic (V_{out}−V_{in}) and voltage gain (dV_{out}/dV_{in}) are measured by sweeping the input voltage (V_{in}) from −2 to 2 V under different supply voltages (V_{dd}), as depicted in Fig. 5C and D, respectively. Utilizing the superior gate control of GaO_x dielectric, the inverter exhibits sharp switching near $V_{in} = 0$ V across all V_{dd} values with V_{out} infinitely close to V_{dd} or 0 V. Notably, a maximum voltage gain of 134.5 is achieved at $V_{dd} = 2$ V. The rapid switching response provides compelling evidence for superior gate control enabled by our GaN/GaO_x heterostructure platform.

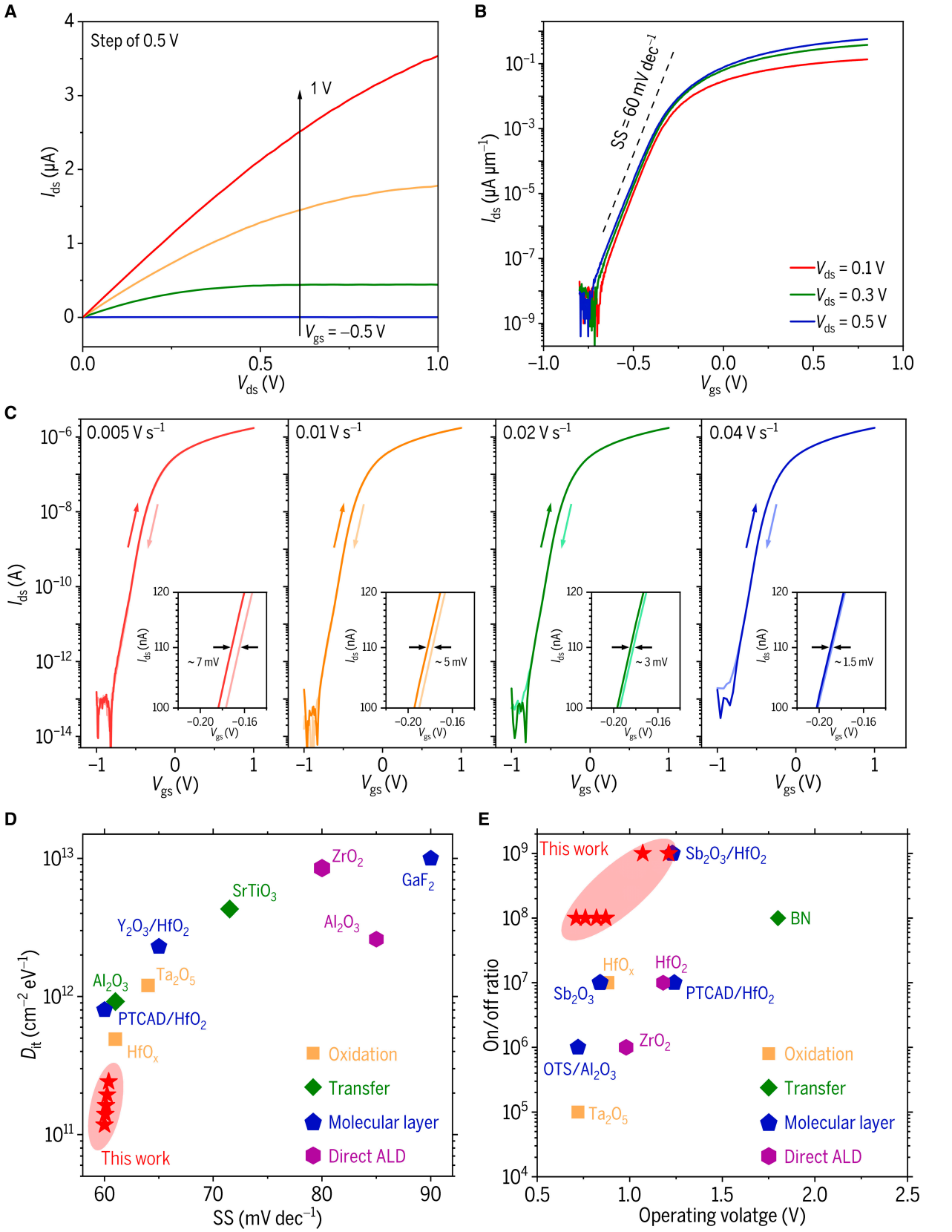


Fig. 3. Excellent performance of MoS_2 FET fabricated on a GaN/GaO_x heterostructure platform. (A) Output characteristic curves of MoS_2 transistor with V_{gs} increasing from −0.5 to 1 V at a step size of 0.5 V. (B) Transfer characteristic curves of MoS_2 transistor at different drain voltages, featuring a channel length of 7 μm and a width of 5 μm. (C) Double-sweep transfer characteristic curves of the MoS_2 transistor at various sweep rates with a constant V_{ds} of 0.5 V. (D) Subthreshold swing (SS) and interface state density (D_{it}) of our device in comparison with transistors fabricated by various approaches [18,21,22,34–39]. (E) Operating voltage and on/off ratio of our device in comparison with MoS_2 transistors fabricated by various approaches [16,19–21,37,40–43].

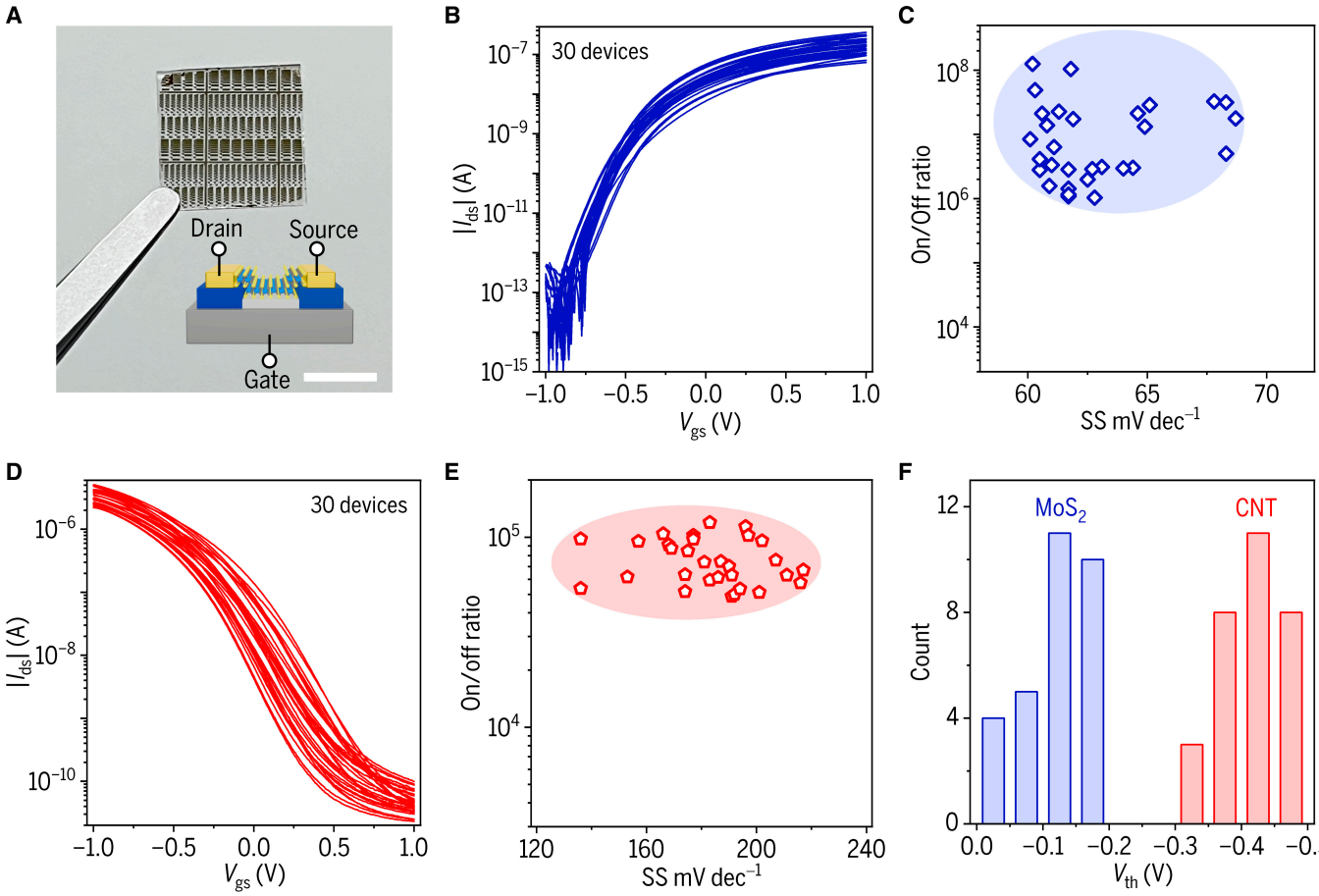


Fig. 4. MoS_2 and CNT transistor arrays. (A) Optical image of CVD MoS_2 transistor arrays fabricated on a GaN/GaO_x heterostructure platform (scale bar: 0.5 cm). Inset: Schematic diagram of the CVD MoS_2 transistor. (B and C) Transfer characteristic curves of 30 MoS_2 transistors with the same channel length (B), and their statistics of SS and on/off ratio (C). (D and E) Transfer characteristic curves of 30 CNT transistors with the same channel length (D), and their statistics of SS and on/off ratio (E). (F) Statistical distribution of V_{th} for 30 CVD MoS_2 FETs and 30 CNT FETs.

Furthermore, dynamic switching cycle tests were conducted on the fabricated inverters. The results indicated that the output voltage amplitude and waveform maintained excellent consistency over consecutive cycles, demonstrating remarkable operational stability (Fig. S21). Further benchmarking against other state-of-the-art complementary inverters reported in the literature revealed that our devices exhibit competitive performance metrics, providing strong evidence for the practical reliability of the proposed platform in integrated circuits (Fig. S22).

Discussion

In conclusion, we have developed an excellent wafer-scale high-κ GaO_x dielectric through the thermal oxidation of GaN and leveraged it for the integration of 2D and 1D materials. MoS_2 FETs fabricated on a GaN/GaO_x heterostructure exhibit excellent performance, including an ultralow D_{it} of 1.18×10^{11} cm^{-2} eV^{-1} and a high on/off current ratio of 10^8 under a small operating voltage of 0.87 V. The heterostructure platform simultaneously supports the fabrication of both CVD-grown monolayer MoS_2 and CNT FET arrays, demonstrating excellent reproducibility across multiple transistors. Complementary inverters integrating n-type MoS_2 and p-type CNT transistors achieve a record-high voltage gain of 134.5 at $V_{dd} = 2$ V. Our work presents a versatile and CMOS-compatible heterostructure integration platform that can unlock the potential of 2D/1D materials for advanced high-performance complementary electronics.

Materials and Methods

Fabrication of a GaN/GaO_x heterostructure

The heavily doped n-type GaN substrate (0001) (resistivity: <0.05 Ω cm) was cleaned sequentially in acetone and isopropanol for 5 min each to remove surface contaminants, followed by diluted HF cleaning for 30 s. The GaO_x dielectric was prepared by thermal oxidation in an oxygen atmosphere at 300 °C for 60 min.

Fabrication of MoS_2 FETs on a GaN/GaO_x heterostructure platform

After ultrasonic cleaning and acid cleaning, a photoresist layer (LOR3A) was spin-coated at 2,000 revolutions per minute (rpm) for 60 s on the GaN substrate and baked at 190 °C for 5 min. Then, another photoresist layer (S-1813) was spin-coated at 4,000 rpm for 60 s on the substrate and baked at 120 °C for 2 min. An undercut structure was fabricated by photolithography and developing processes. The ohmic contact between the metal electrodes and the GaN substrate was formed using a Ti/Al/Ti/Au (20/30/20/30 nm) stack deposited by electron-beam evaporation and lift-off, with subsequent annealing at 700 °C for 30 s in N_2. Then, the Al_2O_3 layer (30 nm thick) was deposited on the substrate via ALD at

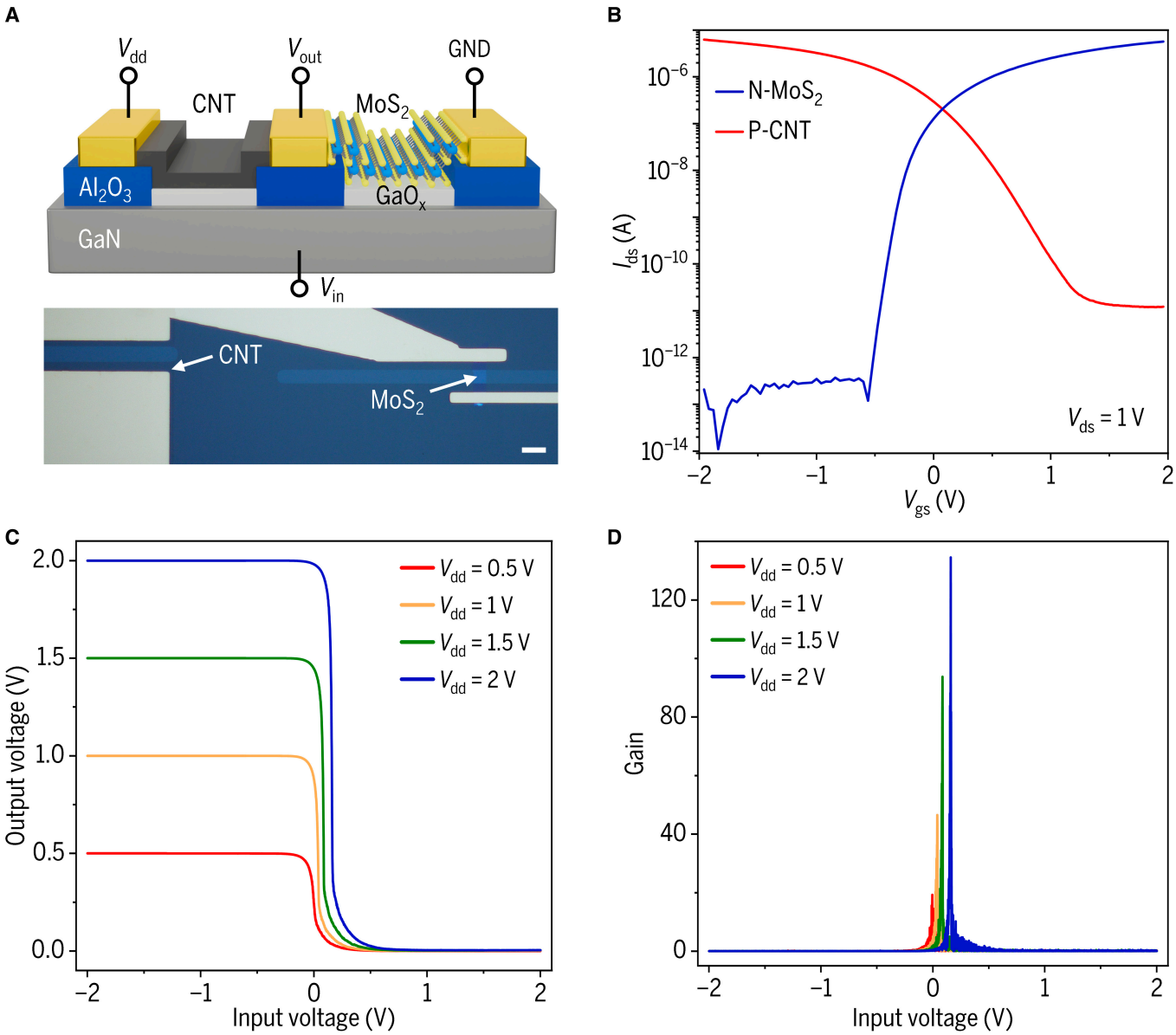


Fig. 5. Complementary inverter fabricated with n-type MoS_2 FET and p-type CNT FET. (A) Schematic diagram and optical image of the inverter fabricated on a GaN/GaO_x heterostructure platform (scale bar: 10 μm). (B) Transfer characteristic curves of MoS_2 and CNT transistors. (C) The voltage transfer characteristics of the inverter at various supply voltages. (D) Corresponding voltage gains.

150 °C, using trimethylaluminum (TMA) and water as precursors. Metal contacts (Ti/Au: 5/50 nm) of drain and source electrodes were deposited on the Al_2O_3 layer. Then, Al_2O_3 layer was patterned by photolithography and etched with H_3PO_4 at 70 °C for 3 min, leaving windows on the GaN substrate for GaO_x dielectric formation. A few-layer MoS_2 flake was mechanically exfoliated from a bulk crystal and transferred onto a polydimethylsiloxane stamp. It was then released onto the target GaO_x dielectric using an electronic van der Waals transfer station. With the same method, we transferred 2 graphene flakes onto the substrate to connect MoS_2 and the Ti/Au and completed the fabrication of the FET.

Fabrication of CVD MoS_2 and CNT FET arrays on a GaN/GaO_x heterostructure platform

The fabrication of CVD MoS_2 and CNT FET arrays followed initial steps similar to the exfoliated MoS_2 transistors. After establishing ohmic contacts to the GaN substrate, an Al_2O_3 layer (30 nm thick) was deposited and patterned via photolithography and H_3PO_4 etching, followed by GaO_x dielectric formation in the exposed regions. For MoS_2 FETs, a centimeter-scale continuous monolayer CVD MoS_2 film was first transferred onto the prepatterned substrate. Then, the excess MoS_2 film was removed by oxygen plasma treatment with an oxygen flow rate of 180 standard cubic centimeters per minute (sccm) for 2 min. Metal contacts (Ti/Au: 5/50 nm) of drain and source electrodes were deposited on the MoS_2 film using photolithography and electron beam evaporation. For CNT FETs, the drain and source electrodes (Ti/Au: 5/50 nm) were first deposited on Al_2O_3. A semiconducting CNT film was then deposited from a toluene solution at 60 °C over 2 h, followed by sequential cleaning in toluene and isopropyl alcohol at 80 °C for 10 min each. Finally, CNT channels were patterned and etched using

oxygen plasma treatment at 200 W with an oxygen flow rate of 180 sccm for 2 min.

Fabrication of complementary inverter

The complementary inverter is implemented with an n-type and a p-type transistor configured in a complementary architecture. First, the p-type CNT FET was fabricated following the standard processes described above. Subsequently, a MoS_2 flake was transferred onto the GaO_x dielectric adjacent to the CNT device, followed by deposition of source/drain electrodes (Ti/Au: 5/50 nm) to complete the n-type MoS_2 FET. Finally, the p-CNT and n-MoS_2 FETs were electrically interconnected to form a complementary inverter.

Characterization

The fabricated devices were characterized using an optical microscope (Nikon ECLIPSE LV100ND), TEM (FEI Talos F200X), XPS (Thermo VG Scientific ESCA LAB250), AFM (Bruker Dimension Icon AFM), micro-Raman analyzer (Jobin Yvon HR800 with 532-nm laser excitation), SIMS (ION TOF-SIMS 5), and x-ray diffraction. The electrical performance of the transistors was measured using a semiconductor analyzer (Agilent B1500A equipped with a B1500A-A20 capacitance measurement unit) and probe station (Cascade Microtech, 150-PK-PROMOTION).

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Author contributions: C.L. and D.-M.S. conceived the idea and supervised the project. J.L. performed device fabrication, electrical measurements, and data analysis assisted by Y.W., S.F., Y.S., and Y.O. J.L., C.L., and D.-M.S. wrote the paper. All authors discussed the results and commented on the manuscript.
Competing interests: The authors declare that they have no competing interests.

Data Availability

The study's data can be obtained from the corresponding authors upon reasonable request.

Supplementary Materials

Figs. S1 to S22

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