Research
A SCIENCE PARTNER JOURNAL

RESEARCH ARTICLE

High-Performance Edge-Contact Monolayer Molybdenum Disulfide Transistors

Jiankun Xiao[1], Xiong Xiong[1*], Xinhang Shi[2], Shiyuan Liu[1], Shenwu Zhu[2], Yue Zhang[3], Ru Huang[1], and Yanqing Wu[1,2*]

[1]School of Integrated Circuits and Beijing Advanced Innovation Center for Integrated Circuits, Peking University, Beijing 100871, China. [2]Wuhan National High Magnetic Field Center and School of Integrated Circuits, Huazhong University of Science and Technology, Wuhan 430074, China. [3]Academy for Advanced Interdisciplinary Science and Technology, Beijing Advanced Innovation Center for Materials Genome Engineering, University of Science and Technology Beijing, Beijing 100083, China.

*Address correspondence to: xiongxiong@pku.edu.cn (X.X.); yqwu@pku.edu.cn (Y.W.)

Citation: Xiao J, Xiong X, Shi X, Liu S, Zhu S, Zhang Y, Huang R, Wu Y. High-Performance Edge-Contact Monolayer Molybdenum Disulfide Transistors. *Research* 2025;8:Article 0593. https://doi.org/10.34133/research.0593

Submitted 7 November 2024
Revised 17 December 2024
Accepted 30 December 2024
Published 17 January 2025

Edge contact is essential for achieving the ultimate device pitch scaling of stacked nanosheet transistors with monolayer 2-dimensional (2D) channels. However, due to large edge-contact resistance between 2D channels and contact metal, there is currently a lack of high-performance edge-contact device technology for 2D material channels. Here, we report high-performance edge-contact monolayer molybdenum disulfide (MoS_2) field-effect transistors (FETs) utilizing well-controlled plasma etching techniques. Plasma etching with pure argon improves the edge dangling bonds and thus improves the edge-contact quality. Edge-contact monolayer MoS_2 FET shows good ohmic contact even at cryogenic temperatures (20 K), achieving a record-low contact resistance (R_c) of 1.25 kΩ·μm among all edge-contact MoS_2 devices. The record-high on-state current of 436 μA/μm and transconductance of 123 μS/μm at $V_{ds} = 1$ V are achieved on an edge-contact monolayer MoS_2 FET with $L_{ch} = 120$ nm. This work highlights the great potential of edge contacts for high-performance monolayer transition metal dichalcogenide (TMD) material electronics.

Introduction

The continuous scaling of traditional semiconductor electronics has faced increasing challenges, especially in terms of surging power consumption and more severe short channel effects. In recent years, the emergence of 2-dimensional (2D) transition metal dichalcogenide (TMD) materials has attracted widespread attention, particularly for the next generation of electronic device architectures for multi-stacked nanosheet devices, owing to their high mobility and excellent electrostatic control at atomically thin thicknesses of below 1 nm [1–6]. Both experimental and theoretical studies have demonstrated and verified the great potential of TMD materials in constructing ultra-short-channel field-effect transistors (FETs) [7–10]. Forming high-quality ohmic contacts is a prerequisite for the future application of monolayer TMD channel FETs [11–15]. The most common and convenient approach is to directly deposit metals onto monolayer TMD materials to form top contacts [16–25]. To date, depositing semi-metals such as antimony and bismuth onto monolayer molybdenum disulfide (MoS_2) with a top contact structure has resulted in a low contact resistance approaching the quantum limit [26,27]. In addition to top contacts, edge contacts have also attracted widespread interest due to their natural advantages in reducing contact length and enabling the construction of vertically stacked nanosheet FETs for ultimate device pitch scaling (Fig. 1A) [28–35]. Previous studies have shown that edge contacts on MoS_2 FETs can eliminate Fermi pinning compared to the common top contacts, attributed to the formation of covalent bonds between 2D MoS_2 and metals presenting a short-range dipole interface [36,37]. However, limited by the high contact resistance for edge contacts, key metrics of high-performance devices, such as on-state current and transconductance, remain lower than expected. Therefore, the realization of high-performance edge-contact monolayer MoS_2 FETs is imperative.

In this work, high-quality edge-contacted FETs are realized using monolayer MoS_2 grown by chemical vapor deposition (CVD), which can be clearly verified from the transmission electron microscopy (TEM) image. By using well-controlled plasma etching technology to form clean edge-contact regions, the etched areas are less susceptible to various molecules, free radicals, adsorbates, and air exposure generated during the plasma process. Specifically, nickel/gold (Ni/Au) contacts were evaporated under high vacuum at a slow deposition rate to serve as ohmic contacts. The edge-contact monolayer MoS_2 FETs exhibited a linear current–voltage relationship at a cryogenic temperature of 20 K. The extracted Schottky barrier of the edge-contact devices was as low as 32 meV, and the contact resistance was 1.25 kΩ·μm. Furthermore, the edge-contact monolayer MoS_2 FETs with $L_{ch} = 120$ nm on HfO_2 dielectric demonstrated high on-state current of 436 μA/μm and transconductance of 123 μS/μm at $V_{ds} = 1$ V, far exceeding previously reported edge-contact 2D devices.

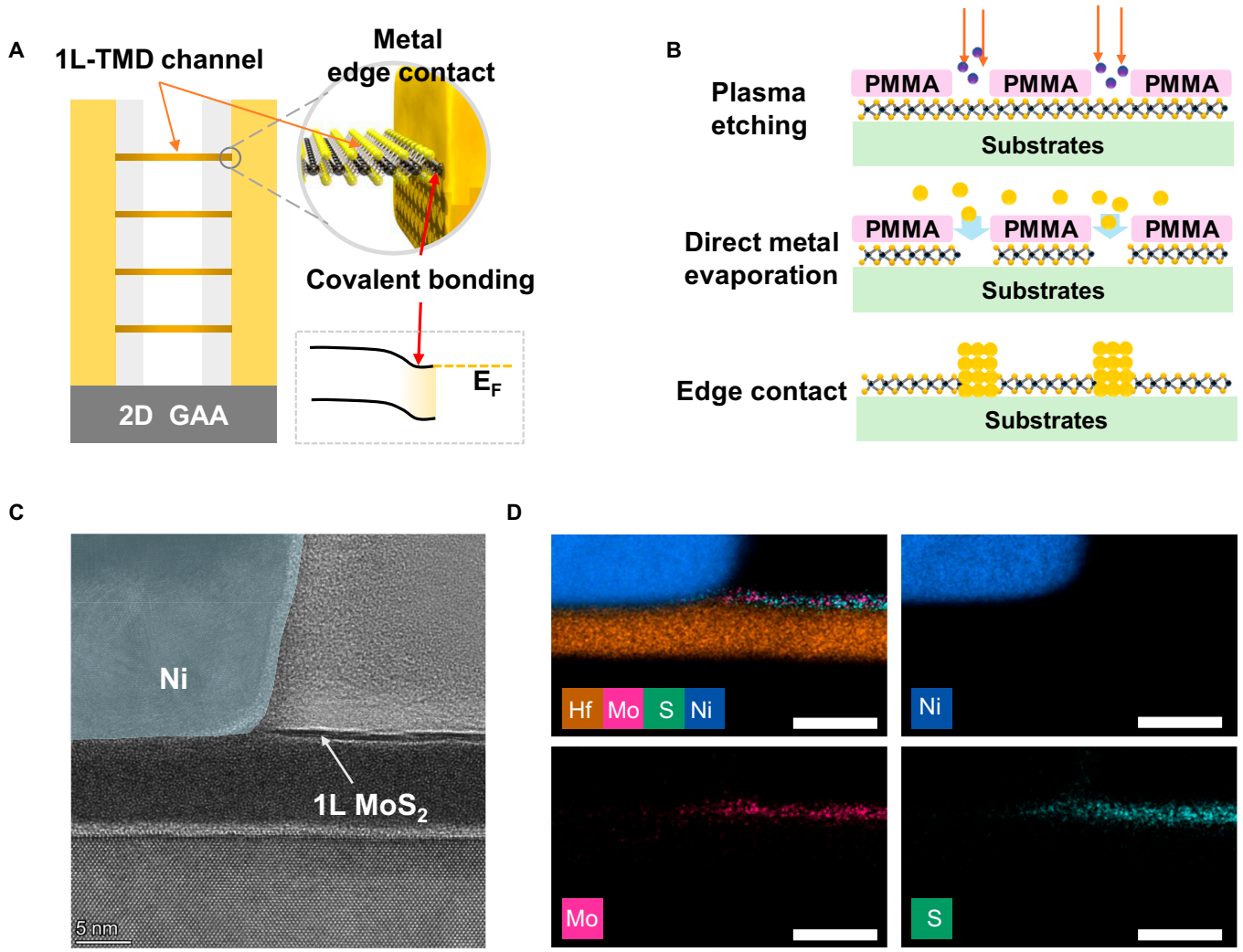

Fig. 1. Schematic diagram and characterization of edge-contact structure. (A) Schematic diagram of 2D gate-all-around (GAA) nanosheet device constructed by edge-contact structure. (B) Schematic diagram of key process flow for monolayer MoS_2 edge-contact FET fabrication. (C) Scanning transmission electron microscopy image of edge contact between metal Ni and the edge of monolayer MoS_2. Scale bar, 5 nm. (D) STEM-EDX elemental map of edge contact between metal Ni and the edge of monolayer MoS_2. The elemental map of metal Ni is connected to those of Mo and S between metal Ni and the edge of monolayer MoS_2. Scale bars, 10 nm.

Results

The manufacturing process of the edge-contact FET is depicted in Fig. 1B. Monolayer MoS_2 film was grown by using CVD method on a glass substrate [38]. The as-grown monolayer MoS_2 films were then transferred onto an HfO_2/Si substrate using polymethyl methacrylate (PMMA) as an adhesion/supporting layer by a wet transfer method. Moreover, it is crucial to note that the as-grown high-quality monolayer MoS_2 is a prerequisite for obtaining high-performance devices [39–41]. The isolation region was etched using inductively coupled plasma (ICP) to obtain a long ribbon of monolayer MoS_2. An annealing process was conducted to eliminate organic residues to achieve a high-quality monolayer MoS_2 channel. The contact regions of FETs were patterned using electron beam lithography, while the channel MoS_2 regions were covered with a PMMA photoresist. Before depositing the contact metal, monolayer MoS_2 of the contact regions was etched by pure argon (Ar) plasma [the control group was treated with oxygen/argon (O_2/Ar) plasma, which will be discussed later]. More importantly, the entire etching process was carried out in a clean room with relatively low humidity, and contact metal was deposited immediately after the etching process. This process is to avoid the reaction of numerous dangling bonds (Mo-bonds and S-bonds) of MoS_2 in the contact regions with various molecules, free radicals, oxygen, and steam in the air to form molybdenum oxide, which reduces the quality of the edge contact [42], which will be further discussed in the following sections. The source/drain contact metal of Ni/Au is evaporated under a high vacuum of 2×10^{-7} torr at a slow rate of 0.01 nm/s, because the low damage metal deposition under high vacuum is also a prerequisite for obtaining high-quality edge contact [43,44]. See Fig. S1 for device fabrication process flow.

To further verify the monolayer MoS_2 edge-contact structure more intuitively, the cross-sectional TEM characterization of the local contact regions of MoS_2/Ni was performed, as shown in Fig. 1C. It is evident that the successful construction of monolayer MoS_2 edge contact has been achieved. The edges of the monolayer MoS_2 on a 9-nm-thick HfO_2 substrate are connected to the deposited metal Ni, visually indicating the formation of edge contact. The corresponding energy-dispersive x-ray spectroscopy (EDXS) mapping shows the element distribution, and the elemental map of metal Ni is connected to those of Mo and S between metal Ni

and the edge of the etched monolayer MoS_2, proving the formation of edge contact, as shown in Fig. 1D.

In addition to the direct observation of the microscopic morphology, we further characterized the material properties of monolayer MoS_2 before and after the etching process for the edge-contact structure by spectroscopic analysis, which was used to confirm that the monolayer MoS_2 in the contact regions had been completely removed prior to contact metallization. Raman and photoluminescence (PL) spectra of the monolayer MoS_2 in the contact regions were characterized before and after the etching process, as depicted in Fig. 2A and B. As shown by the black line in Fig. 2A, the Raman spectra exhibit the E^1_{2g} and A_{1g} peaks with a position difference of 19.5 cm^{-1}, confirming that the as-grown MoS_2 is monolayer, consistent with previous reports [39,40]. The Raman spectrum of the etched monolayer MoS_2 in the contact regions completely disappeared from the E^1_{2g} and A_{1g} mode after the etching process. Similarly, the PL spectrum of the etched monolayer MoS_2 in the contact regions was also completely absent after the etching process, indicating that monolayer MoS_2 in the contact region had been fully removed.

In order to visually understand the electrical transport properties of edge contacts constructed under different etching conditions, the 2 batches of devices were compared side by side, except that different etching processes (Ar plasma or O_2/Ar plasma) were used. Figure 2C shows the transfer characteristics (I_d–V_g curves) of the edge-contact monolayer MoS_2 transistors with L_{ch} = 1 μm at V_{ds} = 0.1 V by using the O_2/Ar plasma and Ar plasma process, respectively. The edge-contact monolayer MoS_2 FET by using Ar plasma shows a 10 times higher on-state current than by using O_2/Ar plasma at the same channel length, which may be attributed to the oxidation of the edges of the etched MoS_2 by using O_2/Ar plasma. The output characteristics (I_d–V_d curves) of the transistors are shown in Fig. 2D. The edge-contact monolayer MoS_2 FET by using Ar plasma exhibits ohmic contact behavior with I_{ds} of 97 μA/μm at V_{ds} = 1 V, while the device using O_2/Ar plasma exhibits Schottky behavior with I_{ds} of 8 μA/μm at V_{ds} = 1 V. The electrical transport properties of devices fabricated under O_2/Ar etching conditions deteriorated substantially, confirming the significant impact of the channel edge dangling bonds on the edge-contact quality.

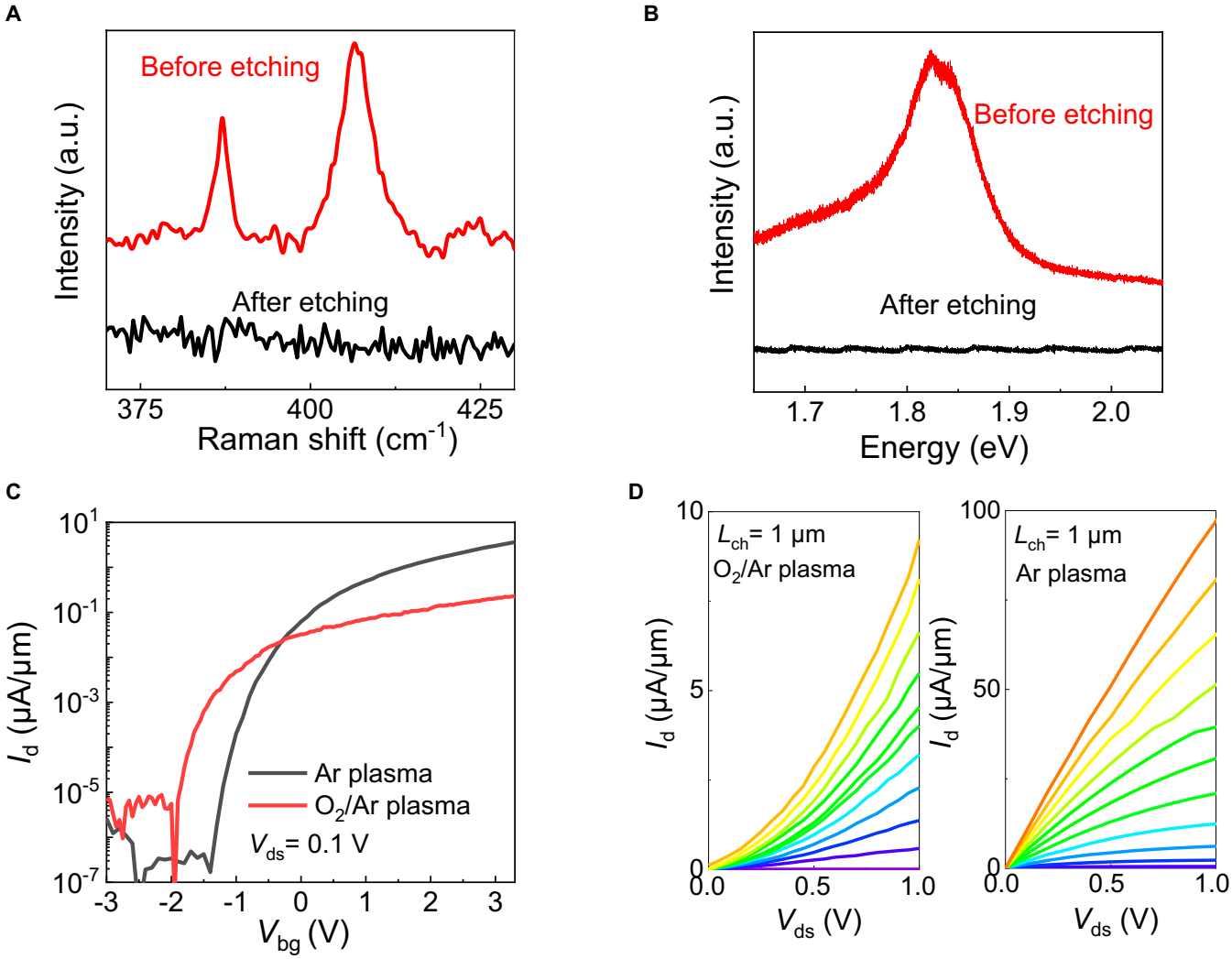

Fig. 2. The electrical characteristics of monolayer MoS_2 edge-contact FETs under different etching conditions. (A) Raman spectra and (B) PL spectra of monolayer MoS_2 before and after the etching process. (C) Transfer characteristics and (D) output characteristics of monolayer MoS_2 edge-contact FET under different etching conditions with L_{ch} = 1 μm. The back-gate voltages range from V_{bg} = −0.5 V to V_{bg} = 5.5 V in 0.5-V step.

To further examine the edge-contact quality for the Ar plasma process, we performed low-temperature measurements of edge-contact FETs with a 200-nm short channel. We present the transfer characteristics of devices with L_{ch} = 200 nm from 300 K to 20 K, as shown in Fig. 3A. It can be observed that the I_d–V_g curves at different temperatures cross around V_{bg} = 1.7 V, which is common in 2D devices and illustrates the transition of the channel from insulating to metallic properties with gate control. Figure 3B compares the output characteristic curves of the edge-contact device with L_{ch} = 200 nm at room temperature of 300 K and cryogenic temperature of 20 K (see Fig. S2). The monolayer MoS_2 edge-contact FET exhibited a linear output curve with a high output currents of 380 and 525 μA/μm at supplied drain–source voltage of 1 V and 2 V, respectively, demonstrating ohmic contact at room temperature. It is clearly shown that the saturated output current density increases from 524 μA/μm at 300 K to 710 μA/μm at 20 K under the same voltage bias of V_{ds} = 2 V and V_{bg} = 6 V, accompanied by current saturation. As depicted in Fig. 3B, the output characteristic curves remain nearly linear even at 20 K, demonstrating quasi-ohmic contact. The low-temperature quasi-ohmic contact phenomenon observed in our FETs is similar to that seen in other top contacts, such as graphene contacts [45] and h-BN/MoS_2 stacks contacts [46], and is crucial to achieving high electrical performance. The Schottky barrier height (SBH; Φ_B) was extracted using the thermionic emission equation described below.

$$I_d = A^*_{2D} T^{2/3} exp\left(-\frac{q\Phi_B}{k_B T}\right)\left[1 - exp\left(\frac{qV_{ds}}{k_B T}\right)\right]$$

In this equation, I_d is the drain–source current, A^*_{2D} is the 2D equivalent Richardson constant, T is the temperature, k_B is the Boltzmann constant, q is the electronic charge, and V_{ds} is the drain–source voltage bias. As shown in Fig. 3C, as the back-gate voltage decreases, the slope of $\ln(I_d/T^{3/2})$ versus $1{,}000/T$ on the Arrhenius plot changes from negative to positive. The extracted SBH is as low as 32 meV at a drain–source voltage bias of 0.1 V, as shown in Fig. 4D. The low SBH in the edge-contacted FETs promotes excellent electrical performance.

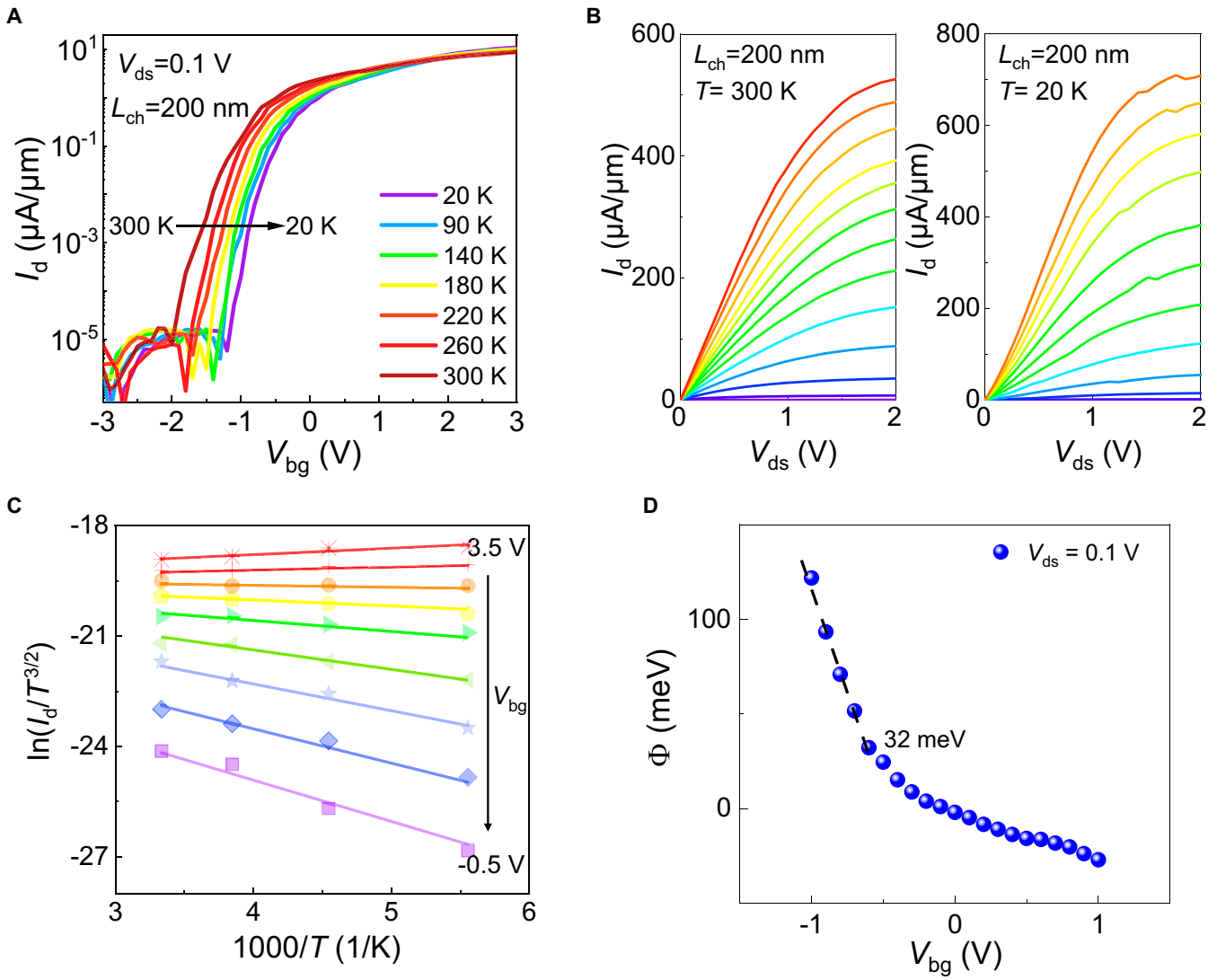

Fig. 3. Low-temperature measurements for monolayer MoS_2 edge-contact FET. (A) Transfer characteristics of monolayer MoS_2 edge-contact FET with temperature from 300 to 20 K with L_{ch} = 200 nm. (B) Output characteristics of monolayer MoS_2 edge-contact FET at 300 and 20 K with L_{ch} = 200 nm. The back-gate voltages range from V_{bg} = −0.5 V to 6 V in 0.5-V step. (C) Arrhenius plot of drain current at various back-gate voltages for calculations of the Schottky barrier heights. (D) Schottky barrier extraction from edge-contact FET.

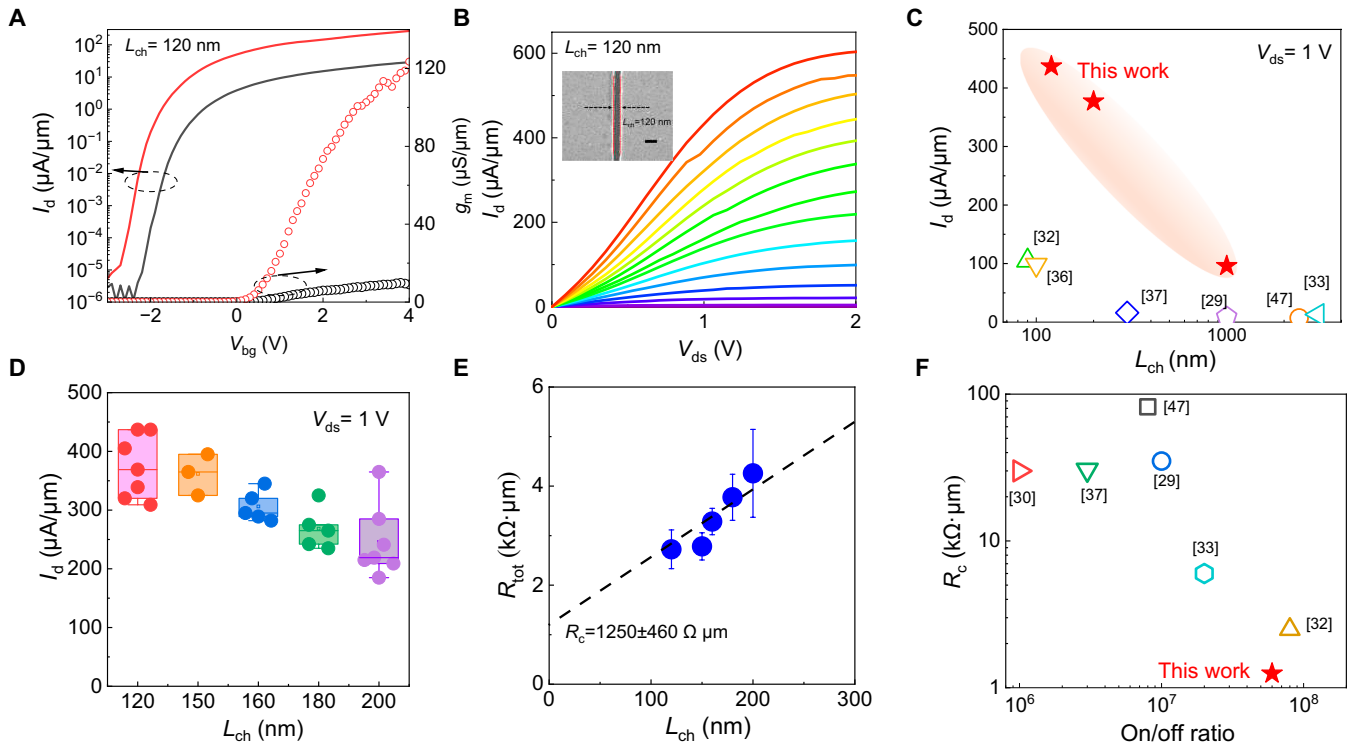

Fig. 4. The electrical characteristics of monolayer MoS_2 edge-contact FETs. (A) Transfer characteristics and transconductance of monolayer MoS_2 edge-contact FET with L_{ch} = 120 nm at V_{ds} = 1 V (red) and V_{ds} = 0.1 V (black). (B) Output characteristics of monolayer MoS_2 edge-contact FET with L_{ch} = 120 nm. The back-gate voltages range from V_{bg} = −0.5 V to 6 V in 0.5-V step. The inset figure is the corresponding SEM image of device for channel length measurement. Inset SEM image scale bar, 200 nm. (C) Output characteristics of monolayer MoS_2 edge-contact FET with L_{ch} = 120 nm. Output current benchmark of monolayer MoS_2 edge-contact FETs with channel length dependence at V_{ds} = 1 V. (D) Statistics of output current of monolayer MoS_2 edge-contact FETs with different L_{ch} at V_{ds} = 1 V. (E) Contact resistance extracted for monolayer MoS_2 edge-contact FETs with different L_{ch}. (F) Contact resistance and on/off ratio benchmark of monolayer MoS_2 edge-contact FETs.

To evaluate the potential of edge-contact monolayer MoS_2 transistors at scaled channel lengths, a 120-nm short-channel high-performance edge-contact FET was demonstrated. The corresponding scanning electron microscopy (SEM) image is shown in the inset of Fig. 4B. Figure 4A shows the transfer characteristics of the edge-contact monolayer MoS_2 FET at V_{ds} = 0.1 and 1 V. The device exhibits high on-state current, low sub-threshold swing (SS) of 150 mV/dec, and an on/off ratio of 6×10^7. Owing to the low SBH of the edge contacts and high-quality HfO_2 dielectric layer for MoS_2 transistors, the peak transconductance g_m of the device reaches 123 μS/μm at V_{ds} = 1 V. As shown in the output characteristic curves of Fig. 4B, high output current of 605 and 436 μA/μm is obtained at supplied drain–source voltage of 2 and 1 V, respectively. To the best of our knowledge, the output current of 436 μA/μm at V_{ds} = 1 V in this work represents the highest output current density for monolayer MoS_2 edge-contact FETs to date, more than 4 times higher than previous studies as shown in benchmark figure of Fig. 4C. Table S1 lists the specific comparisons of different electrical parameters. Furthermore, through statistical analysis of the measurement results of several edge-contact devices with different channel lengths (L_{ch} = 120, 150, 160, 180, and 200 nm), the repeatability of high output current in short-channel edge-contact FETs at V_{ds} = 1 V can be confirmed, as shown in Fig. 4D. Obviously, the output current of all edge-contact devices remains at a high level, verifying the high-quality edge contacts in this work.

Essentially, the high output current and on-state current of edge-contact FET can be attributed to the low R_c generated by the well-constructed bonded edge interface. By extensively analyzing the output current with different channel lengths, the R_c for the edge-contact FETs is extracted as shown in Fig. 4E. Contact resistance extracted from devices with channel lengths below 200 nm is more accurate, as the contact resistance either dominates the total resistance or is at least comparable to the channel resistance. The R_c value of edge-contact monolayer MoS_2 FETs is 1.25 ± 0.46 kΩ·μm, better than the values of edge-contact MoS_2 FETs reported in the literatures [29,30,32,33,37,47], as depicted in Fig. 4F. Furthermore, a scaled contact length (L_c) device with L_c = 120 nm and L_{ch} = 220 nm was also successfully demonstrated experimentally to show the potential of device scaling (Fig. S3).

Discussion

We have reported the high-performance edge-contact monolayer MoS_2 FET by using CVD grown monolayer MoS_2, with channel length reduced to 120 nm. The plasma etching by pure Ar improves the edge dangling bonds and thus improves the edge-contact quality. Edge-contact monolayer MoS_2 FETs exhibit good ohmic contact at both room temperature and cryogenic temperatures, and have a record-low contact resistance of 1.25 kΩ·μm among all edge-contact monolayer MoS_2 FETs. Record-high output current of 436 μA/μm and transconductance of 123 μS/μm with a steep SS of 150 mV/dec are achieved on an edge-contact monolayer MoS_2 FET with L_{ch} = 120 nm on 9-nm HfO_2 dielectric. For edge contacts, the core advantage is that it can be immune to the deterioration of performance

caused by the reduction of top contact length and can build stacked nanosheet structures, which is crucial for achieving multi-layer TMD channel stacked device structures to break through the physical gate length limitations of traditional semiconductor devices while improving device performance. Due to the limitation of experimental equipment and materials, the width of source–drain metal electrodes demonstrated in this work needs to be further reduced to 10 nm in the future, edge-contact devices for multi-bridge channels need to be explored and validated, and device reliability under this structure needs to be further explored. In addition, novel metallic materials and deposition techniques can also be employed in subsequent studies to achieve further reduction of contact resistance and achieve the robustness of the device's mechanical structure.

Materials and Methods

CVD growth of monolayer MoS_2 and material characterization

Monolayer MoS_2 was grown on molten glass. The growth was carried out using a furnace with 2 temperature zones, with temperatures of 250 and 860 °C in each zone. The sulfur powder was loaded onto the quartz boat and placed in zone I, while the MoO_3 precursor and the molten glass were loaded into a porcelain boat and placed in zone II. Ar gas was always supplied during the growth process. At 860 °C, the growth time of MoS_2 was about 35 min. MoS_2 was transferred to the target substrate through wet method. The basic morphology of MoS_2 was observed using an optical microscope. The thickness of MoS_2 was basically determined by Raman and PL.

FET fabrication

The grown MoS_2 was transferred by wet method onto the high-quality HfO_2 dielectric deposited by atomic layer deposition. Generally, the thickness of HfO_2 used is about 9 nm. To obtain a regular strip-shaped MoS_2, the electron beam lithography (Raith eLine) and Ar/CF_4 plasma etching (by reactive ion etching) were used. Subsequently, monolayer MoS_2 was annealed at 250 °C for 1 h in Ar atmosphere. After electron beam lithography and etching, monolayer MoS_2 in the contact area was removed by reactive ion etching. The contact metal (Ni/Au) was then deposited under high vacuum conditions.

Electrical measurement

The direct-current electrical measurements were conducted using a Lakeshore probe station and an Agilent B1500A semiconductor parameter analyzer. All measurements are conducted in a vacuum of 10^{-4} torr to reduce the influence of moisture and oxygen in the measurement environment.

Acknowledgments

Funding: This work was supported by the Natural Science Foundation of China (grant nos. 92364203, 92464303, 62090034, 62425402, and 62104012), the National Key Research and Development Program of China (grant nos. 2022YFB4400100 and 2021YFA1202903), Beijing Natural Science Foundation (grant no. 4242057), and Technology Innovation Program of Hunan Province (grant no. 2021RC5008).
Author contributions: Y.W. supervised the project. X.X. and Y.W. conceived the project. J.X. performed the MoS_2 growth, device fabrication, and electrical measurement. S.L. and X.S. assisted in the growth of materials and characterization of devices. S.Z. assisted in the device fabrication and electrical measurement. J.X., X.X., and Y.W. analyzed the data and co-wrote the manuscript. All authors contributed to discussions and commented on the manuscript.
Competing interests: The authors declare that they have no competing interests.

Data Availability

All data required to support the conclusions are presented in the main text and the Supplementary Materials.

Supplementary Materials

Figs. S1 to S3
Table S1

References

1. Radisavljevic B, Radenovic A, Brivio J, Giacometti V, Kis A. Single-layer MoS_2 transistors. *Nat Nanotechnol*. 2011;6:147–150.
2. Zhuo F, Wu J, Li B, Li M, Tan CL, Luo Z, Sun H, Xu Y, Yu Z. Modifying the power and performance of 2-dimensional MoS_2 field effect transistors. *Research*. 2023;6:0057.
3. Xiong X, Liu S, Liu H, Chen Y, Shi X, Wang X, Li X, Huang R, Wu Y. Top-gate CVD WSe_2 pFETs with record-high I_d~ 594 μA/μm, G_m~ 244 μS/μm and WSe_2/MoS_2 CFET based half-adder circuit using monolithic 3D integration. Paper presented at: 2022 International Electron Devices Meeting (IEDM); 2022; San Francisco, CA, USA.
4. Wei X, Zhang X, Yu H, Gao L, Tang W, Hong M, Chen Z, Kang Z, Zhang Z, Zhang Y. Homojunction-loaded inverters based on self-biased molybdenum disulfide transistors for sub-picowatt computing. *Nat Electron*. 2024;7(2):138–146.
5. Cao W, Bu H, Vinet M, Cao M, Takagi S, Hwang S, Ghani T, Banerjee K. H wang S, Ghani T, Banerjee K. The future transistors. *Nature*. 2023;620:501–515.
6. Kim KS, Kwon J, Ryu H, Kim C, Kim H, Lee EK, Lee D, Seo S, Han NM, Suh JM, et al. The future of two-dimensional semiconductors beyond Moore's law. *Nat Nanotechnol*. 2024;19(7):895–906.
7. Desai SB, Madhvapathy SR, Sachid AB, Llinas JP, Wang Q, Ahn GH, Pitner G, Kim MJ, Bokor J, Hu C, et al. MoS_2 transistors with 1-nanometer gate lengths. *Science*. 2016;354(6308):99–102.
8. Liu H, Neal AT, Ye PD. Channel length scaling of MoS_2 MOSFETs. *ACS Nano*. 2012;6(10):8563–8569.
9. Cao W, Liu W, Kang J, Banerjee K. An ultra-short channel monolayer MoS_2 FET defined by the curvature of a thin nanowire. *IEEE Electron Device Lett*. 2016;37(11):1497–1500.
10. Liu Y, Guo J, Wu Y, Zhu E, Weiss NO, He Q, Wu H, Cheng HC, Xu Y, Shakir I, et al. Pushing the performance limit of sub-100 nm molybdenum disulfide transistors. *Nano Lett*. 2016;16(10):6337–6342.
11. Allain A, Kang J, Banerjee K, Kis A. Electrical contacts to two-dimension semiconductors. *Nat Mater*. 2015;14(12):1195–1205.
12. Schulman DS, Arnold AJ, das S. Contact engineering for 2D materials and devices. *Chem Soc Rev*. 2018;47:3037.

13. Liu X, Choi MS, Hwang E, Yoo WJ, Sun J. Fermi level pinning dependent 2D semiconductor devices: Challenges and prospects. *Adv Mater*. 2022;34(15):Article 210842.
14. Kang J, Liu W, Sarkar D, Jena D, Banerjee K. Computational study of metal contacts to monolayer transition metal dichalcogenide semiconductors. *Phys Rev X*. 2014;4: Article 031005.
15. Kim C, Moon I, Lee D, Choi MS, Ahmed F, Nam S, Cho Y, Shin HJ, Park S, Yoo WJ. Fermi level pinning at electrical metal contacts of monolayer molybdenum dichalcogenides. *ACS Nano*. 2017;11(2):1588–1596.
16. Radisavljevic B, Kis A. Mobility engineering and a metal insulator transition in monolayer MoS_2. *Nat Mater*. 2013;12:815–820.
17. Zou Y, Li P, Su C, Yan J, Zhao H, Zhang Z, You Z. Flexible high-temperature MoS_2 field-effect transistors and logic gates. *ACS Nano*. 2024;18:9627–9635.
18. Si M, Su CJ, Jiang C, Conrad NJ, Zhou H, Maize KD, Qiu G, Wu CT, Shakouri A, Alam MA, et al. Steep-slope hysteresis-free negative capacitance MoS_2 transistors. *Nat Nanotechnol*. 2018;13(1):24–28.
19. Xiao J, Chen K, Zhang X, Liu X, Yu H, Gao L, Hong M, Gu L, Zhang Z, Zhang Y. Approaching ohmic contacts for ideal monolayer MoS_2 transistors through sulfur-vacancy engineering. *Small Methods*. 2023;7:2300611.
20. Liu Y, Guo J, Zhu EB, Liao L, Lee SJ, Ding MN, Shakir I, Gambin V, Huang Y, Duan XF. Approaching the Schottky-Mott limit in van der Waals metal-semiconductor junctions. *Nature*. 2018;557:696–700.
21. Wang Y, Kim JC, Wu RJ, Martinez J, Song XJ, Yang J, Zhao F, Mkhoyan A, Jeong HY, Chhowalla M. Van der Waals contacts between three-dimensional metals and two-dimensional semiconductors. *Nature*. 2019;568(7750):70–74.
22. Kappera R, Voiry D, Yalcin SE, Branch B, Gupta G, Mohite AD, Chhowalla M. Phase-engineered low-resistance contacts for ultrathin MoS_2 transistors. *Nat Mater*. 2014;13(12):1128–1134.
23. Chee SS, Seo D, Kim H, Jang H, Lee S, Moon SP, Lee KH, Kim SW, Choi H, Ham MH. Lowering the Schottky barrier height by graphene/Ag electrodes for high-mobility MoS_2 field-effect transistors. *Adv Mater*. 2019;31(2):1804422.
24. Das S, Chen HY, Penumatcha AV, Appenzeller J. High performance multilayer MoS_2 transistors with scandium contacts. *Nano Lett*. 2013;13(1):100–105.
25. Cao Z, Lin F, Gong G, Chen H, Martin J. Low Schottky barrier contacts to 2H-MoS_2 by Sn electrodes. *Appl Phys Lett*. 2020;116:002101.
26. Shen PC, Su C, Lin Y, Chou AS, Cheng CC, Park JH, Chiu MH, Lu AY, Tang HL, Tavakoli MM, et al. Ultralow contact resistance between semimetal and monolayer semiconductors. *Nature*. 2021;593(7858):211–217.
27. Li W, Gong X, Yu Z, Ma L, Sun W, Gao S, Köroğlu Ç, Wang W, Liu L, Li T, et al. Approaching the quantum limit in two-dimensional semiconductor contacts. *Nature*. 2023;613(7943):274–279.
28. Cao Q, Han SJ, Tersoff J, Franklin AD, Zhu Y, Zhang Z, Tulevski GS, Tang J, Haensch W. End-bonded contacts for carbon nanotube transistors with low, size-independent resistance. *Science*. 2015;350(6256):68–72.
29. Jain A, Szabó Á, Parzefall M, Bonvin E, Taniguchi T, Watanabe K, Bharadwaj P, Luisier M, Novotny L. One-dimensional edge contacts to a monolayer semiconductor. *Nano Lett*. 2019;19(10):6914–6923.
30. Guimaraes MH, Gao H, Han Y, Kang K, Xie SE, Kim CJ, Muller DA, Ralph DC, Park J. Atomically thin ohmic edge contacts between two-dimensional materials. *ACS Nano*. 2016;10(6):6392–6399.
31. Cui X, Lee GH, Kim YD, Arefe G, Huang PY, Lee CH, Chenet DA, Zhang X, Wang L, Ye F, et al. Multi-terminal transport measurements of MoS_2 using a van der Waals heterostructure device platform. *Nat Nanotechnol*. 2015;10(6):534–540.
32. Xiao J, Kang Z, Liu B, Zhang X, Du J, Chen K, Yu H, Liao Q, Zhang Z, Zhang Y. Record-high saturation current in end-bond contacted monolayer MoS_2 transistors. *Nano Res*. 2022;15(1):475–481.
33. Lee S, Wang X, Shin H, Ali N, Ngo TD, Hwang E, Kim GH, Yeom GY, Watanabe K, Taniguchi T, et al. Semi-metal edge contact for barrier-free carrier transport in MoS_2 field effect transistors. *ACS Appl Electron Mater*. 2024;6:4149–4158.
34. Choi MS, Ali N, Ngo TD, Choi H, Oh B, Yang H, Yoo WJ. Recent progress in 1D contacts for 2D-material-based devices. *Adv Mater*. 2022;34(39):2202408.
35. Cheng Z, Yu Y, Singh S, Price K, Noyce SG, Lin YC, Cao L, Franklin AD. Immunity to contact scaling in MoS_2 transistors using in situ edge contacts. *Nano Lett*. 2019;19(8):5077–5085.
36. Yang Z, Kim C, Lee KY, Lee M, Appalakondaiah S, Ra CH, Watanabe K, Taniguchi T, Cho K, Hwang E, et al. A fermi-level-pinning-free 1D electrical contact at the intrinsic 2D MoS_2–metal junction. *Adv Mater*. 2019;31(25):1808231.
37. Hung TY, Wang SY, Chuu CP, Chung YY, Chou AS, Huang FS, Chen T, Li MY, Cheng CC, Cai J, et al. Pinning-free edge contact monolayer MoS_2 FET. Paper presented at: 2020 IEEE International Electron Devices Meeting (IEDM); 2020; Virtual.
38. Zhang Z, Xu X, Song J, Gao Q, Li S, Hu Q, Li X, Wu Y. High-performance transistors based on monolayer CVD MoS_2 grown on molten glass. *Appl Phys Lett*. 2018;113: Article 202103.
39. Zhang XK, Liao QL, Liu S, Kang Z, Zhang Z, Du JL, Li F, Zhang SH, Xiao JK, Liu BS, et al. Poly(4-styrene sulfonate)-induced sulfur vacancy self-healing strategy for monolayer MoS_2 homojunction photodiode. *Nat Commun*. 2017;8:15881.
40. Zhang XK, Liao QL, Kang Z, Liu BS, Ou Y, Du JL, Xiao JK, Gao L, Shan H, Luo Y, et al. Self-healing originated van der Waals homojunctions with strong interlayer coupling for high-performance photodiodes. *ACS Nano*. 2019;13(3):3280–3291.
41. Chang MC, Ho PH, Tseng MF, Lin FY, Hou CH, Lin IK, Wang H, Huang PP, Chiang CH, Yang YC, et al. Fast growth of large-grain and continuous MoS_2 films through a self-capping vapor-liquid-solid method. *Nat Commun*. 2020;11(1):3682.
42. Santosh KC, Longo RC, Addou R, Wallace RM, Cho K. Electronic properties of MoS_2/MoO_x interfaces: Implications in tunnel field effect transistors and hole contacts. *Sci Rep*. 2016;6:33562.
43. English CD, Shine G, Dorgan VE, Saraswat KC, Pop E. Improved contacts to MoS_2 transistors by ultra-high vacuum metal deposition. *Nano Lett*. 2016;16(6):3824–3830.
44. Sun Z, Kim SY, Cai J, Shen J, Lan HY, Tan Y, Wang X, Shen C, Wang H, Chen Z, et al. Low contact resistance on monolayer MoS_2 field-effect transistors achieved by CMOS-compatible metal contacts. *ACS Nano*. 2024;18(33):22444–22453.
45. Liu Y, Wu H, Cheng HC, Yang S, Zhu E, He Q, Ding M, Li D, Guo J, Weiss NO, et al. Toward barrier free contact to molybdenum disulfide using graphene electrodes. *Nano Lett*. 2015;15(5):3030–3034.

46. Cui X, Shih EM, Jauregui LA, Chae SH, Kim YD, Li B, Seo D, Pistunova K, Yin J, Park JH, et al. Low-temperature ohmic contact to monolayer MoS_2 by van der Waals bonded Co/h-BN electrodes. *Nano Lett*. 2017;17(8):4781–4786.

47. Conde-Rubio A, Liu X, Boero G, Brugger J. Edge-contact MoS_2 transistors fabricated using thermal scanning probe lithography. *ACS Appl Mater Interfaces*. 2022;14(37): 42328–42336.