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REVIEW

Modifying the Power and Performance of 2-Dimensional MoS_2 Field Effect Transistors

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Over the past 60 years, the semiconductor industry has been the core driver for the development of information technology, contributing to the birth of integrated circuits, Internet, artificial intelligence, and Internet of Things. Semiconductor technology has been evolving in structure and material with co-optimization of performance–power–area–cost until the state-of-the-art sub-5-nm node. Two-dimensional (2D) semiconductors are recognized by the industry and academia as a hopeful solution to break through the quantum confinement for the future technology nodes. In the recent 10 years, the key issues on 2D semiconductors regarding material, processing, and integration have been overcome in sequence, making 2D semiconductors already on the verge of application. In this paper, the evolution of transistors is reviewed by outlining the potential of 2D semiconductors as a technological option beyond the scaled metal oxide semiconductor field-effect transistors. We mainly focus on the optimization strategies of mobility (μ), equivalent oxide thickness (EOT), and contact resistance (R_C), which enables high ON current (I_{on}) with reduced driving voltage (V_{dd}). Finally, we prospect the semiconductor technology roadmap by summarizing the technological development of 2D semiconductors over the past decade.

Introduction

In 1965, Gordon Moore, the cofounder of Intel, extrapolated an observation and projection through historical trend that the number of transistors in a dense integrated circuit (IC) doubles about every 2 years, which has become an indestructible economic driver for the exponential growth of the semiconductor industry. It is important to note that Moore's Law [1] is not a law of nature, but a guideline that the semiconductor industry uses as a goal. In a sense, this law will fail one day as the atomic scaling approaches. The first 50 years of Moore's Law is the miniaturization of device scale, and then the optimized performance and power consumption are obtained naturally, which is the so-called "happy scaling era". After that, the benefits of scaling down have not been enough to meet the needs for performance improvement, and the industry aimed at more extreme interconnection, mobility, and dielectric engineering, and even subverted the bulk/planar structure to obtain the performance improvement and power consumption reduction. The characteristic field effect transistor (FET) scaling length is derived as $\lambda = \sqrt{EOT \bullet \varepsilon_s \bullet t_s / \varepsilon_{ox}}$, where EOT, ε_{ox}, ε_s, and t_s are the equivalent oxide thickness of gate oxide, the dielectric constant of gate oxide, the dielectric constant, and the thickness of channel materials, respectively. Therefore, transistors demand larger gate capacitances (high dielectric constant and thinner oxide thickness) and thinner channel thicknesses to maintain ideal switching characteristics at sufficiently small dimensions.

Figure 1 reviews the development of semiconductor technology since the 1990s. The early device characteristics roughly follow the Denard Scaling principle; that is, the channel length and the driving voltage V_{dd} of the new-generation devices are reduced by 30% to ensure a constant electric field, which, in turn, leads to a 30% lower circuit delay τ. Crucially, after the 130-nm node, Dennard Scaling [2] is out of work, enabling explosive new technologies beyond scaling down. Before the 65-nm node, aluminum was replaced by copper for interconnect, resulting in lower series resistance [3]. On the other hand, SiGe increased silicon mobility by 35% through lattice strain [4,5]. During this period, the reduction of power consumption was just a windfall of the reduced V_{dd} that comes with shrinking channel dimensions. In the following 45-nm node, the severe short-channel effect caused leakage current and degradation of the subthreshold slope ($SS = \frac{ln(10)k_BT}{e}\left(1 + \frac{C_s}{C_{ox}}\right) = \frac{ln(10)k_BT}{e}\left(1 + \frac{C_s + eD_{it}}{C_{ox}}\right)$,

where k_B, T, e, C_s, C_{ox}, and D_{it} are the Boltzmann constant, the absolute temperature, the elementary charge, the areal channel capacitance, the areal gate oxide capacitance, and the density of interface traps, respectively). In fact, the industry has employed oxynitride instead of pure SiO_2 as a gate dielectric since the 1990s to raise the dielectric constant and to offer other advantages against dopant diffusion. By the 65-nm node, the thickness of oxynitride has been reduced to 1.2 nm [6], which approaches the quantum tunneling limit, and the next-generation devices (45 nm node) have to introduce a higher dielectric constant (high-κ metal gate abbreviated as HKMG) to enhance gate modulation while suppressing tunneling current [7].

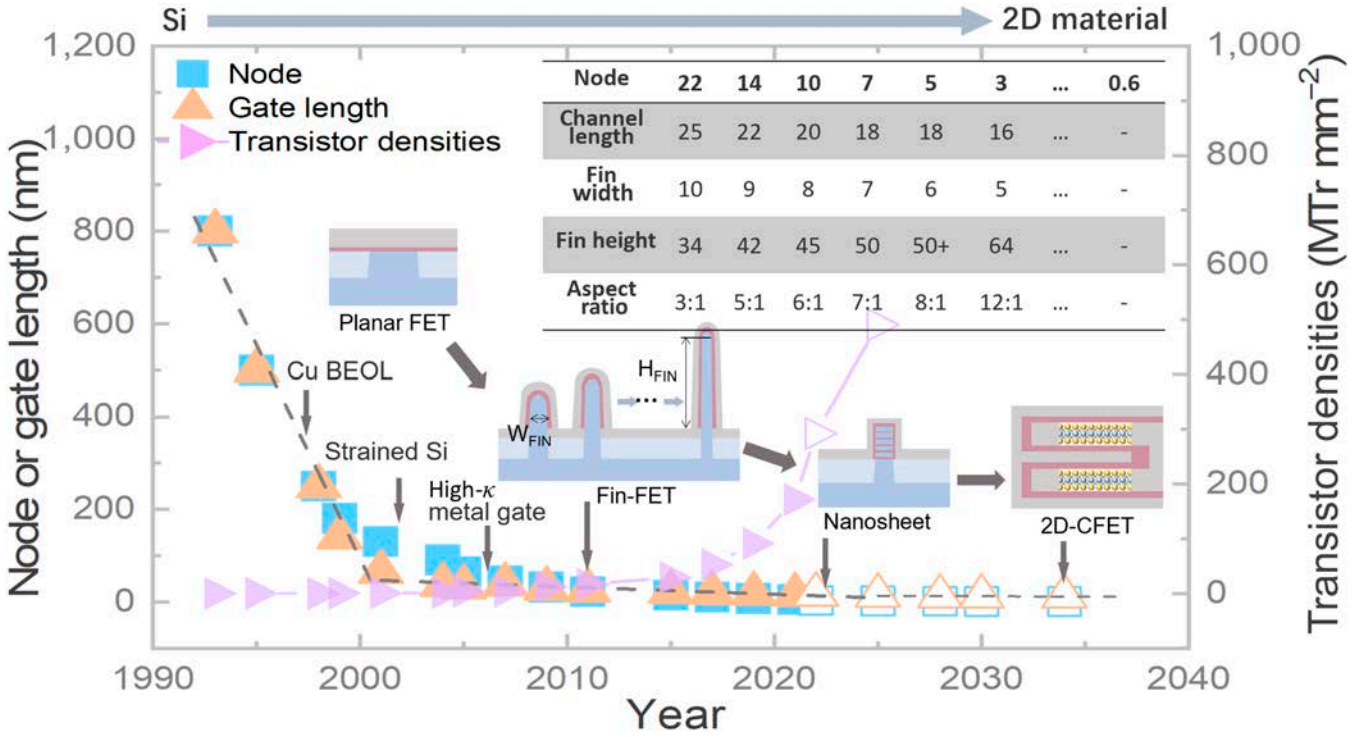
An even bigger technological leap occurred at 22 nm, and since then, semiconductor devices embraced the biggest structural revolution since complementary metal oxide semiconductor, with Fin-FET and ultrathin body silicon on insulator (UTB-SOI) replacing the planar devices and bulk silicon technologies, respectively [8]. For more advanced nodes, SOI requires a wafer-scale fully depleted nanosheet with a thickness of sub-3 nm, which is a huge challenge to the present technology. As shown in the inset of Fig. 1, Fin-FET has undergone sixth-generation testing since its commercial application, up to the state-of-the-art 3-nm node. It is worth noting that, to obtain more effective gate control, the Fin thickness is continually decreased with increasing gate height to compensate for current decline. For the 3-nm node, the aspect ratio exceeds 12:1 (64 nm vs. 5 nm) [9], while maintaining a smooth interface. Manufacturing such an aspect ratio extremely challenges both cost and processing, and therefore, gate-all-around (GAA)-FET is proposed to enhance gate control, thanks to the more comprehensive gate coverage and thinner channel compared to Fin-FETs. Remarkable performance and *SS* improvements have been achieved by vertically stacking multi-bridge channel (MBC) FET [8].

For device structure, both Fin-FET and MBC-FET are approaching quasi-2-dimensional (2D) nanosheets, and a better solution is the thinner semiconductor layer. 2D semiconductors, especially transition metal dichalcogenides (TMDs) with a general chemical formula of MX_2, exhibit atomically thin thickness and provide perfect gate modulation on an extremely scaled planar or MBC-FET structure [10–21]. TMD materials also show tunable bandgap and carrier mobility by engineering the element composition [22–24], layer number [25,26], and strain [26,27], which are promising for high-performance transistors at sub-3-nm nodes. Moreover, the growth of TMD single crystal over wafer was realized, which is the key step toward commercialization [28,29]. Therefore, with the proper combination of materials and structures, TMD and their heterojunctions will enable numerous new electronic and optoelectronic applications [30–32].

In this paper, we will review the development of TMD logic devices, especially the key technologies to achieve high-performance, low-power transistors through systematic optimizations of mobility, dielectric, and contact. First, we expound the characteristics of ideal 2D metal oxide semiconductor field-effect transistors. Next, we start with key device metrics and summarize the most important progresses published in the literature. Finally, we discuss the optimal device performance data reported to date and prospect the requirements for future industrial applications.

The Ideal 2D Transistor

Benefiting from van der Waals (vdW) stacking of 2D semiconductors, it is more feasible to realize MBC-FET and complementary FET (CFET) structures compared to bulk materials, and thus to obtain superior device characteristics. Figure 2A schematically illustrates the typical 2D MBC-FET, consisting



Node	22	14	10	7	5	3	...	0.6
Channel length	25	22	20	18	18	16	...	-
Fin width	10	9	8	7	6	5	...	-
Fin height	34	42	45	50	50+	64	...	-
Aspect ratio	3:1	5:1	6:1	7:1	8:1	12:1	...	-

Fig. 1. Evolution of transistors: from Si-FET to 2D-FET. The blue solid square symbol, orange solid regular triangle symbol, and purple solid triangle symbol show the relationship of node, gate length, and transistor density with year, respectively. The open symbols are the prediction data adapted from IRDS 2021 [9]. The table on the upper right gives the related parameters of Fin-FET evolution starting from 22 nm.

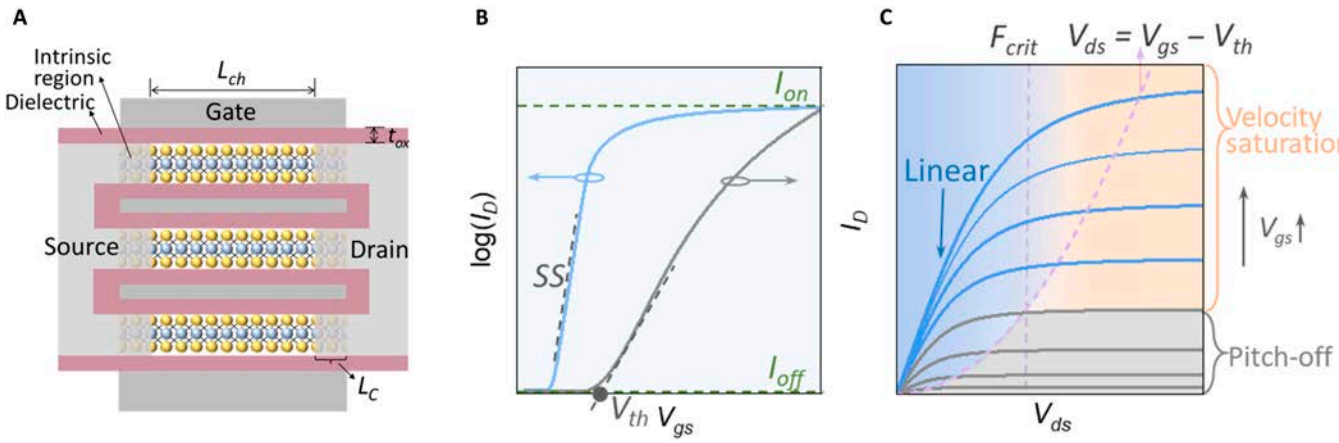


Fig. 2. Ideal 2D MBC-FET and its electrical characteristics. (A) Structure of a typical 2D MBC-FET. The L_C, L_{ch}, and t_{ox} are the contact length, the effective channel length, and the thickness of the gate dielectric, respectively. (B and C) Transfer ($I_D - V_{gs}$) and output ($I_D - V_{ds}$) characteristics of a typical n-type 2D-FET. The *SS*, V_{th}, I_{on}, I_{off}, and F_{crit} are the subthreshold swing, the threshold voltage extracted in the linear region, the on-state and off-state current, and the critical field, respectively.

of multiple vertically stacked 2D semiconductor channels. Paralleling multiple channels provides a larger drive current while saving footprint on wafer. The total resistance arises mainly from the contact resistance (R_C) and the channel resistance (R_{ch}). The latter can be expressed as:

$$R_{tot} = \left(R_C + \frac{L}{WC_{ox}\mu\left(V_{gs} - V_{ds}\right)} \right) / N \quad (1)$$

where L, W, N, C_{ox}, μ, V_{gs}, and V_{ds} are the effective channel length and width, the stacking layer number, the areal capacitance of the gate oxide, the mobility, the gate voltage, and the drain voltage, respectively. Therefore, for a specific node, lower R_c, higher mobility, and greater areal capacitance are critical for better drive capability. Figure 2B and C plots the representative transfer and output curves, where some key metrics are marked beside. Note that, small *SS* and low off-state current are essential for low power consumption (dynamic and static). On the other hand, a large on-state current is also highly desired, as seen in both the output and transfer curves, which points to good contact and high mobility. Furthermore, a well-controlled threshold voltage (V_{th}) that can serve as an indicator of process variation is especially important for large-scale integration. Next, we will systematically discuss the principal performance metrics at the device level.

Scattering and Mobility Booster

Carrier mobility represents the drift velocity per unit electric field, and is a key parameter to characterize the charge transport. Mobility can be expressed as $\mu = \frac{e\tau_m}{m*}$, closely related to the mean free time (τ_m) and the effective mass (m^*). For a specific semiconductor, scattering determines τ_m and thus its mobility. Compared with that in Si, the charge transport in TMD is more susceptible to scattering (intrinsic and extrinsic). According to Matthiessen's Law, in a TMD containing multiple scattering mechanisms, the free carrier mobility can be evaluated by [33,34]

$$\mu(T)^{-1} = \mu_{ph}(T)^{-1} + \mu_{SO}(T)^{-1} + \mu_{CI}(T)^{-1} + \mu_{DE}{}^{-1} \quad (2)$$

where μ_{ph}, μ_{SO}, μ_{CI}, and μ_{DE} are the mobilities associated with the intrinsic phonons, the surface optical phonons (SOs), the Coulomb impurities (CIs), and the defects, respectively. Therefore, quantitatively determining the contributions of the various scatterings to the resistivity poses an enormous challenge, which invokes collaboration between the experimental study with precisely controlled parameters and the numerical modeling so as to interpret the relevant mobility variations with scattering.

Take MoS_2 as an example, the $\mu - T^{-1}$ relationship under different scattering mechanisms is qualitatively plotted in Fig. 3A. The highest or theoretical mobility of ~410 $cm^2 V^{-1} s^{-1}$ for monolayer MoS_2 at room temperature should signify a transport mode dominated by the intrinsic phonon scattering, which consists of longitudinal acoustic (Fig. 3A (I)) and optical (Fig. 3A (II)) wave phonons. Acoustic phonon scattering contributes mainly at low temperatures less than 100 K and its scattering rate linearly depends on the temperature (T), and thus the intrinsic phonon-limited mobility varies as $\mu \propto T^{-1}$. When the temperature is greater than 100 K, the optical wave phonons become the major contributor, and then the intrinsic phonon-limited mobility varies as $\mu \propto T^{-1.69}$ [35]. Apart from the intrinsic electron-phonon scattering, remote interaction with the polar optical phonons at the dielectric surface (Fig. 3A (III)), named SO scattering, gives rise to even stronger temperature dependence, in particular at high temperatures [36]. SO scattering is proportional to the ionization strength of the chemical bonds in dielectric, and the molybdenum-oxygen (Mo-O) bonds of oxide with high dielectric constants have stronger ionization strengths, which can lead to more severe SO scattering [37]. Differing from that in traditional Si transistors, SO scattering could significantly degrade the mobility of 2D-FETs, especially for GAA devices with double-side high-κ dielectric [36]. Under the combined influence of intrinsic phonons and SO, the room-temperature mobility of monolayer MoS_2 FETs using high-κ dielectric may be as low as 200 $cm^2 V^{-1} s^{-1}$ [38,39]. Even so, the experimental mobility of monolayer MoS_2 could be much lower than the theoretical value. The nature of the charge transport in MoS_2, however, remains poorly understood despite the extensive theoretical and experimental studies performed to date. In the early days, the mobility of monolayer MoS_2 was around 10 $cm^2 V^{-1} s^{-1}$, and the $\mu - T^{-1}$ relationship exhibited obvious insulating behaviors [40–42] (Fig. 3A (VII)). Combining the electrical transport measurements and

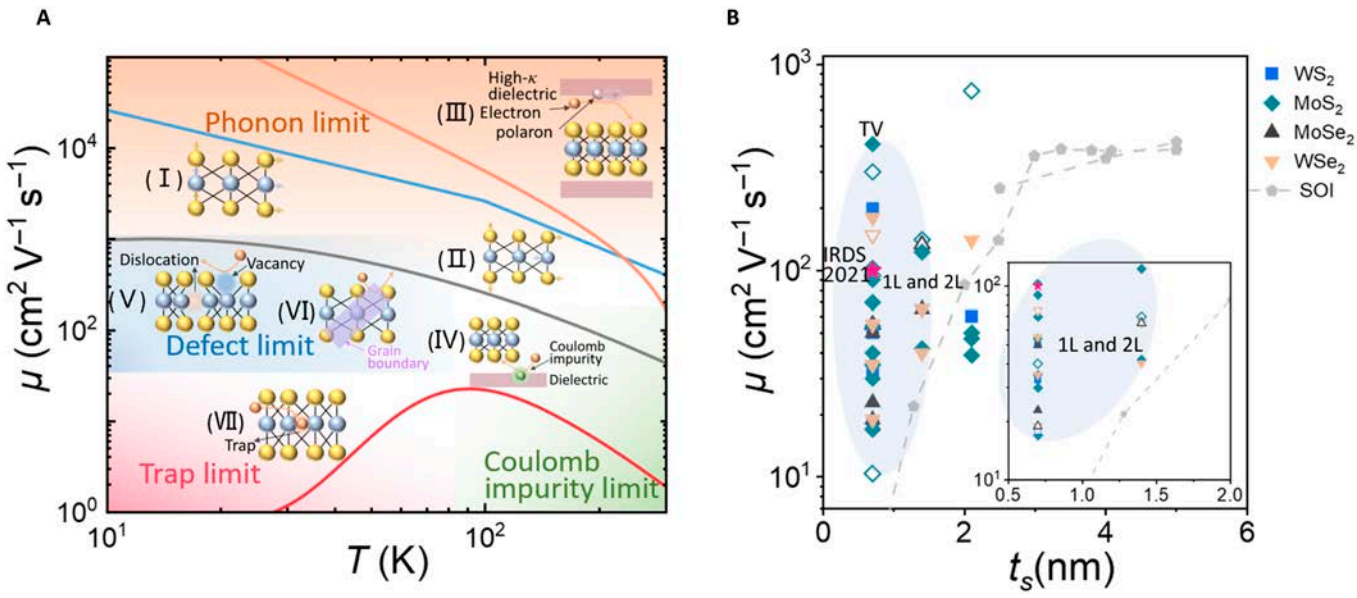


Fig. 3. Scattering and mobility in 2D-FETs. (A) Mobility as a function of *T* for different scatterings in a typical MoS_2 transistor. The orange, blue, and gray lines represent mobilities limited by the SO scattering, the intrinsic phonon scattering, and the Coulomb impurity scattering in monolayer MoS_2, respectively. The red line reveals mobility degeneration after introducing the effect of localized states and traps. (I) Deformation potential of phonons caused by atomic vibrations. (II) Frohlich interaction caused by polar optical phonons. (III) Surface phonon scattering. (IV) Coulomb impurity scattering. (V) Atomic defect scattering. (VI) Defect and grain boundary scattering. (VII) Trap effects. All halos in schematics represent potential. (B) Mobility versus the channel film thickness for CVD-growth TMD (solid symbols), mechanically exfoliated TMD (hollow symbols), and ultrathin silicon-on-insulator. The oval region highlights the mobility of monolayer and bilayer TMD. TV is the abbreviation of the theoretical value, for monolayer MoS_2. The inset shows more details of the sub-2-nm region. The mobility values of MoS_2, WSe_2, $MoSe_2$, WS_2, and SOI are reproduced from Refs. [14, 29, 32, 49–53, 56, 57, 60–62, 67, 69, 70, 72, 73, 127, 128, 148–151], Refs. [110, 152–155], Refs. [156–158], Refs. [110, 129, 159], and Refs. [160–164], respectively.

the atomic-resolution transmission electron microscopy, Qiu et al. found a large number of intrinsic sulfur vacancies presented in the MoS_2 lattice. These vacancies acted as localized states, giving rise to hopping transport at low carrier concentration (n_{2D}) [43]. Besides, a particularly important source of scattering stems from the CIs at the semiconductor/dielectric interface, which are believed to be the limiting factor of the present MoS_2 devices [44]. The intensity of CI scattering depends on the CI density. The essence of CI scattering is the interaction with the electric field, which can be screened by the external field. Accordingly, the screened potential reads [45,46] $\phi_q^{scr} = \frac{\phi_q}{\varepsilon_{2D}(q,T)}$, where $\phi_q = \frac{e^2}{(\varepsilon_{box}+\varepsilon_0)q}$ and $\varepsilon_{2D}(q,T) = 1 + \frac{2\varepsilon_{el}(q)}{\varepsilon_{box}+\varepsilon_0}$ are the bare potential and the screening effect by the substrate and the free electrons, respectively; ε_{box} and ε_0 are the permittivity of the substrate and vacuum; $\varepsilon_{el}(q)$ corresponds to the electronic part of the dielectric function and depends on the carrier density n. As n and ε_{box} increase, screening gets stronger, reducing the scattering potential and thus increasing the CI-limited mobility.

To obtain higher mobility, numerous interface and defect engineering designs have been proposed for TMD. Yu et al. [34] developed thiol chemistry to achieve in situ defect modification, which effectively passivates defects and traps, significantly increasing mobility at room temperature. Furthermore, they introduced the screening effect through a high-κ with high carrier concentration to suppress CI scattering and realized a phonon-limited mobility of ~150 $cm^2\ V^{-1}\ s^{-1}$ at room temperature in monolayer MoS_2 [33]. It was demonstrated that by sandwiching a monolayer MoS_2 channel in-between boron nitride (BN) layers, CI scattering can be considerably suppressed, leading to high mobility at room temperature and at low temperatures [41,47,48]. Moreover, optimized chemical vapor deposition (CVD), especially single-crystal growth, is an effective and industry-compatible technique to reduce defects and increase mobility [29,30,32,49–73]. Currently, for most 2D semiconductors, CVD films exhibit properties that far exceed those of mechanically exfoliated flakes.

Figure 3B summarizes the thickness-dependent mobility of Si and 2D semiconductors, including MoS_2, $MoSe_2$, WS_2, and WSe_2. The conventional Si is subject to the repeated thinning and etching processes, and its mobility drops sharply as the SOI thickness reduces below 3 nm. This will severely restrict the device performance at the advanced nodes. By contrast, the thickness of monolayer TMDs is only 0.7 nm. Although the experimental mobility is far lower than the theoretical prediction, it still holds distinct advantage against SOI to provide one-decade higher mobility at similar thickness. In future, an ultraclean, nondestructive manufacturing environment and the delicate design of device structures are vital to the development of 2D-FETs.

Dielectric Integration and Interface Engineering

Scaling down has long relied on dielectric thinning for greater gate controllability (small *SS* and high transconductance) and for lower leakage. As native oxide, SiO_2 benefits from the nearly perfect interface with Si and has transformed from an ideal dielectric layer to an ideal interface layer in the high-κ era (Figure 4A) [74,75] with D_{it} below $10^{10}\ cm^{-2}\ eV^{-1}$ at the SiO_2/Si interface [76] and an *EOT* of 0.6 nm for the state-of-the-art technology node [77]. Nowadays, atomic layer deposition (ALD) can produce very precise ultrathin high-κ dielectric with SiO_2 as a buffer

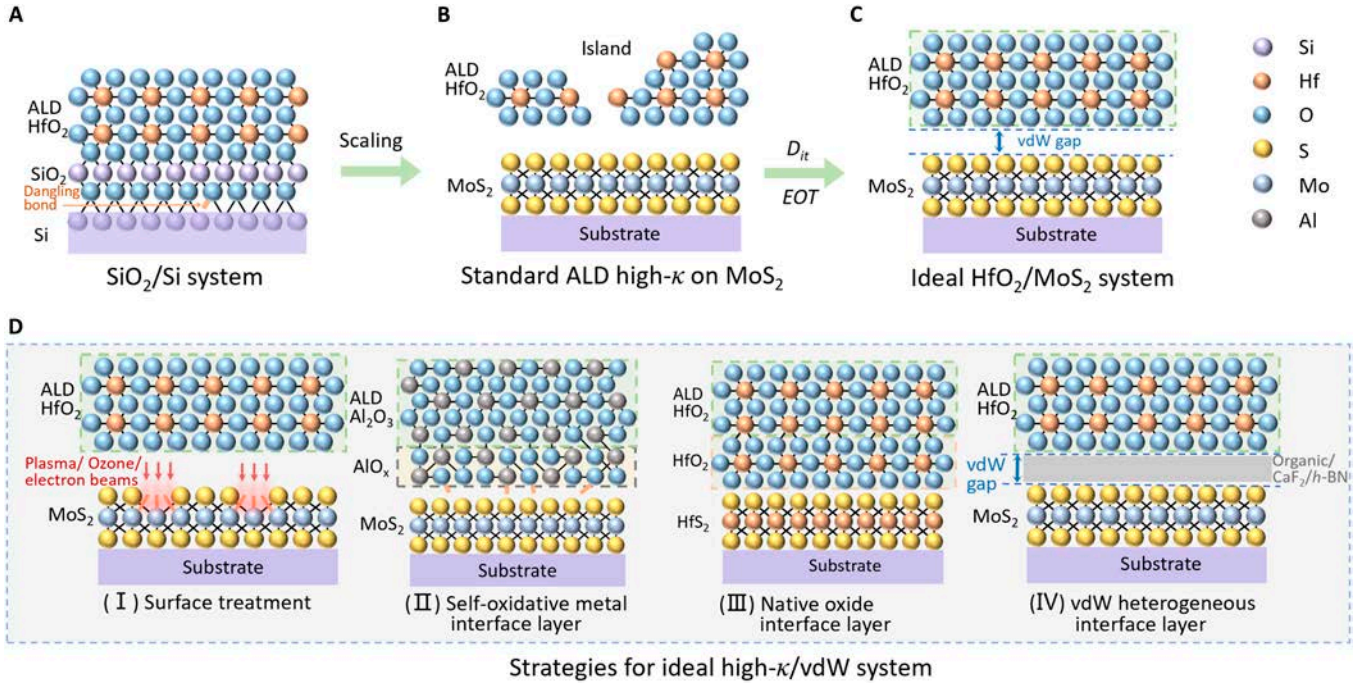


Fig. 4. Dielectric engineering in 2D-FETs. (A) Schematic of high-quality SiO_2/Si interface ($D_{it} < 10^{10}$ cm^{-2} eV^{-1}) thanks to a tight covalent bond. (B) Schematic of direct ALD high-κ dielectric on 2D channel to continue Moore's Law such as HfO_2/MoS_2. (C) Schematic of an ideal dielectric/2D semiconductor system. (D) Schematic illustration of 4 strategies for integrating high-κ dielectric onto 2D channels, where (I) is for surface functionalization strategy, (II) is for oxidation of the metal seed layer above the channel, (III) is for channel self-oxidation, and (IV) is for vdW integration strategy by inserting an intermediate buffer layer between the 2D channel and high-κ dielectric layer, such as organic/CaF_2/*h*-BN.

layer. The layer-by-layer deposition of ALD depends on the precursor adsorption and nucleation by interfacial dangling bonds. Therefore, the surface rich in dangling bonds is the key to achieving a high-quality ALD dielectric. For 2D materials, however, the inherent absence of out-of-plane dangling bonds, responsible for vdW stacking, poses a huge obstacle to ALD-based dielectric integration. When dielectric is directly deposited on 2D materials by ALD, the precursors preferentially nucleate at the sites of lattice defects to form island-like growth, which exacerbates interface properties (Figure 4B). In fact, the ideal integration of dielectric for 2D devices should be through direct vdW stacking of high-κ dielectric and 2D materials (Fig. 4C). However, these methods are neither compatible with industrial technology nor applicable to top-gate architecture. Therefore, dielectric integration in manufacturing top-gate 2D-FETs must involve interfacial modifications.

In the past decade, several strategies have been developed for interfacial modification of 2D materials, especially for 2D semiconductors (Fig. 4D): (I) surface treatment, (II) self-oxidative metal interface layer, (III) native oxide interface layer, and (IV) vdW heterogeneous interface layer. Regardless of the method utilized, the effective *EOT* will be the sum of the *EOT* of interface layer and ALD oxide. Thus, the optimum interface layer should exhibit the lowest *EOT* while maintaining the extremely low D_{it}.

The purpose of surface treatment is to create uniform point defects and dangling-bonds on 2D surface, which assist the adsorption and the nucleation of ALD precursors. Typical treatment methods include plasma [78–80], ozone [81,82], and electron beam irradiation [83,84]. Obviously, surface treatment sacrifices interface quality and will sizably raise D_{it}. Furthermore, introduction of these interfacial defects further increases the source of CI scattering, resulting in irreversible degradation of mobility. Huang et al. [78] achieved ~1.5 nm of Al_2O_3 through water plasma treatment and the corresponding D_{it} reached 2.1×10^{12} cm^{-2} eV^{-1}, which is more than 2 orders of magnitude higher than that at SiO_2/Si [76]. Another widely used interface layer aims to evaporate a thin chemically active metal (such as aluminum [85–87], magnesium [85], and yttrium [85,88,89]). The self-oxidative product can serve as a dielectric or ALD interface layer. This method is also commonly applicable to other systems such as carbon nanotube [90] and organic transistors [91]. The self-oxidative metal methodology has good versatility for different materials. The resultant interface layer maintains a relatively high dielectric constant, but inevitably incurs channel damage during the evaporation process [92]. The fatal drawback is that, in order to ensure the interface uniformity and controllable leakage, the thickness of the accompanying self-oxidative layer usually exceeds a few nanometers, which is difficult to meet the *EOT* requirements of advanced node. As a result of combining the advantages of the aforementioned methods, a more advanced interface layer—2D native oxide—was invented recently. Typical examples are HfS_2 [93] and Bi_2O_2Se [94]. Lai et al. [93] fabricated top-gate FET with a low D_{it} of 6×10^{11} cm^{-2} eV^{-1} between HfS_2 channel and converted HfO_2 dielectric. Li et al. [94] achieved 0.9 nm of *EOT* dielectric layers of Bi_2SeO_5 through layer-by-layer oxidation of the underlying 2D Bi_2O_2Se semiconductor. The corresponding leakage current was lower than 1×10^{-7} A·cm^{-2} under an external field strength of 1 MV·cm^{-1}. This method is expected to meet both of the requirements for interface quality and *EOT* under precise control. However, the problem is also obvious: only a few specific 2D semiconductors can form dense native

oxide, especially Mo-based and W-based TMD with the greatest application potential, for which this methodology is completely infeasible. Hence, another strategy, viz., vdW heterogeneous interface layer, is more friendly to 2D materials owing to ultrasmooth interface and damage-free vdW interaction. Wang et al. [95] used organic molecule perylene tetracarboxylic acid (PTCA) to treat graphene and realized noncovalent functionalization, assisting the deposition of high-quality ALD dielectric. Afterwards, Li et al. attained an organic crystal interface monolayer of only 0.3 nm by choosing new organic molecules of perylenetetracarboxylic dianhydride (PTCDA) in conjunction of optimizing the molecular deposition process. Breaking through of 1 nm of *EOT* was made for 2D materials [96]. In further statistical studies, Yu et al. [97] proved that the PTCDA interface layer could enable high dielectric reliability comparable to that of SiO_2/Si. The noncovalent monolayer of organic crystal has excellent interface quality, versatility, and reliability for 2D devices, but is restricted by the intrinsic low dielectric constant. Therefore, it is still very challenging to achieve a more aggressive *EOT* of sub-1 nm by means of this technique. More recently, Liu et al. employed a 2D inorganic molecular crystal of Sb_2O_3 as an ALD interface layer. Benefiting from its ultrahigh dielectric constant of 11.5 and the equally perfect interfacial quality to PTCDA, inorganic molecular crystals demonstrated great potential to become a new candidate of interfacial layer [98].

In addition to the traditional ALD oxide, 2D layered dielectrics have also been considered to be a unique solution for their 2D vdW properties. The representative, first-generation layered dielectric should be hexagonal BN (*h*-BN). Yet, its dielectric constant is only 4 [99]. Moreover, the serious leakage current [100] and the layer-by-layer transfer make *h*-BN almost impossible to be applied for larger-scale integration. A new generation of layered dielectric has been reported in recent years. For example, layered calcium fluoride [101,102] and strontium titanate [103] permitted vdW integration, realizing a record *EOT* down to 0.6 nm with excellent interface between high-κ and 2D semiconductors. However, such technologies are still in demonstration for back-gate devices. Future development of top-gate integration will be essential for CFETs and MBC-FETs.

In principle, *EOT*, gate leakage currents (I_g), and D_{it} of high-quality dielectric/semiconductor systems must be strictly controlled to be lower than 1 nm, 10^{-2} A·cm^{-2} [104], and 10^{10} cm^{-2} eV^{-1} [96,105], respectively. The quality of the 2D channel and the gate dielectric layer, and the breakdown voltage are critical for top-gate or GAA 2D-FET as well. Currently, vdW integration (as shown in Fig. 4D (IV)) is a promising solution to the damage-free manufacturing of high-κ dielectrics onto 2D semiconductors, while satisfying the needs of *EOT*, I_g, and D_{it}. Of course, the premise is to find a high-κ 2D dielectric material suitable for 2D semiconductors.

Ohmic Contact for 2D-FET

At the advanced nodes, the physical channel length is only of dozen nanometers, and (quasi-)ballistic transport within mean free path dominates [106]. Consequently, the influence of mobility on the on-state current of metal oxide semiconductor field-effect transistors greatly attenuates. For ultrashort channel, R_C contributes mostly to the total resistance [107]. The Schottky barrier (SB), which is the energetic difference between the valence (or conduction) band edge of the semiconductor and the work function (WF) of the contact metal, blocks carrier injection from the source into the semiconductor and becomes the most important origin of R_C. According to the Schottky–Mott limit, the SB height of metal–semiconductor (M–S) contact can be manipulated by adjusting metal's WF. However, SB height is usually insensitive to WF. In reality, the Fermi level is often pinned by interface states, known as Bardeen limit [108,109]. Fermi level pinning (FLP) influences charge injection from metal into semiconductor at 2 levels: (a) metal-induced gap states (MIGS), which are ubiquitous in M–S contact [110–113] and (b) surface states resulting from contact interface traps or defects. FLP effect presents in almost all M–S junctions and has never been resolved. Yet, in commercial devices, this issue can be effectively circumvented by using degenerate doping to form an ultrathin tunneling barrier [114–116]. Owing to the atomic-scale thickness and the doping-free nature, SB in 2D-FET is significantly dictated by the contact characteristics. Take the conventional evaporated metal on MoS_2 as example (see Fig. 5A and E for details), the intrinsic and extrinsic defects (created by high-energy metal atoms and clusters bombarding during metal deposition) introduce large density of states, which, in turn, pins the Fermi level near the midgap states [92,117–120]. In this case, no matter how the metal's WF changes, the carriers will always experience a similar injection barrier, manifesting almost the same transport behavior [121–126].

Therefore, in order to satisfactorily obtain R_c, 2 strategies can be utilized: (a) contact doping to make metallic contact or tunneling barrier and (2) MIGS suppression to minimize the SB height. The mainstream strategies for R_C optimization are summarized in Fig. 5I. Inherited from silicon technology, contact doping is a consequential approach to reducing injection barrier and thus R_C for whatever n-type and p-type devices [127–134]. Yang et al. [129] reported that, by employing chloride molecular doping to reduce SB width, R_C of few-layer WS_2 and MoS_2 were decreased to 0.7 kΩ·μm and 0.5 kΩ·μm, respectively. Gao et al. [130] achieved degenerate p-type doping and observed hole transport in the MoS_2 channel for the first time, where the specified MoS_2 was treated by electronegative materials such as MoO_3 or MoO_2. Metallic phase 2D materials are another effective strategy [135–138]. The metallic 1T phase of MoS_2 can be locally induced by alkali metal intercalation on semiconducting 2H phase, thus decreasing R_c to 200 to 300 Ω·μm at zero gate voltage [135]. Also, the metallic 1T phase of vdW materials can be locally induced by strain [136], laser beam irradiation [137], and argon plasma bombardment [138] on semiconducting 2H phase. Recently, Wu et al. attained R_C as low as 250 Ω·μm through atomically ultraclean vdW vanadium diselenide contacts [139]. A schematic of the energy band diagram and the structure of phase-engineered contacts are provided in Fig. 5C and G, respectively. For 2D semiconductors, however, the metallic phase is a thermodynamically metastable structure, which causes serious reliability and stability issues to the potential electronic applications. The vdW interaction of 2D semiconductors is thus expected to fundamentally eliminate the FLP effect so as to achieve ohmic contacts, as told by the Schottky–Mott limit. Yet, in the early works, the tunneling interface layer was the mainstream solution to reduce defects caused by evaporation. Researchers employed ALD-deposited oxide or transferred *h*-BN intercalated interfaces to form metal–insulator–semiconductor contacts, effectively reducing the SB height to be around 35 meV (see Fig. 5B)

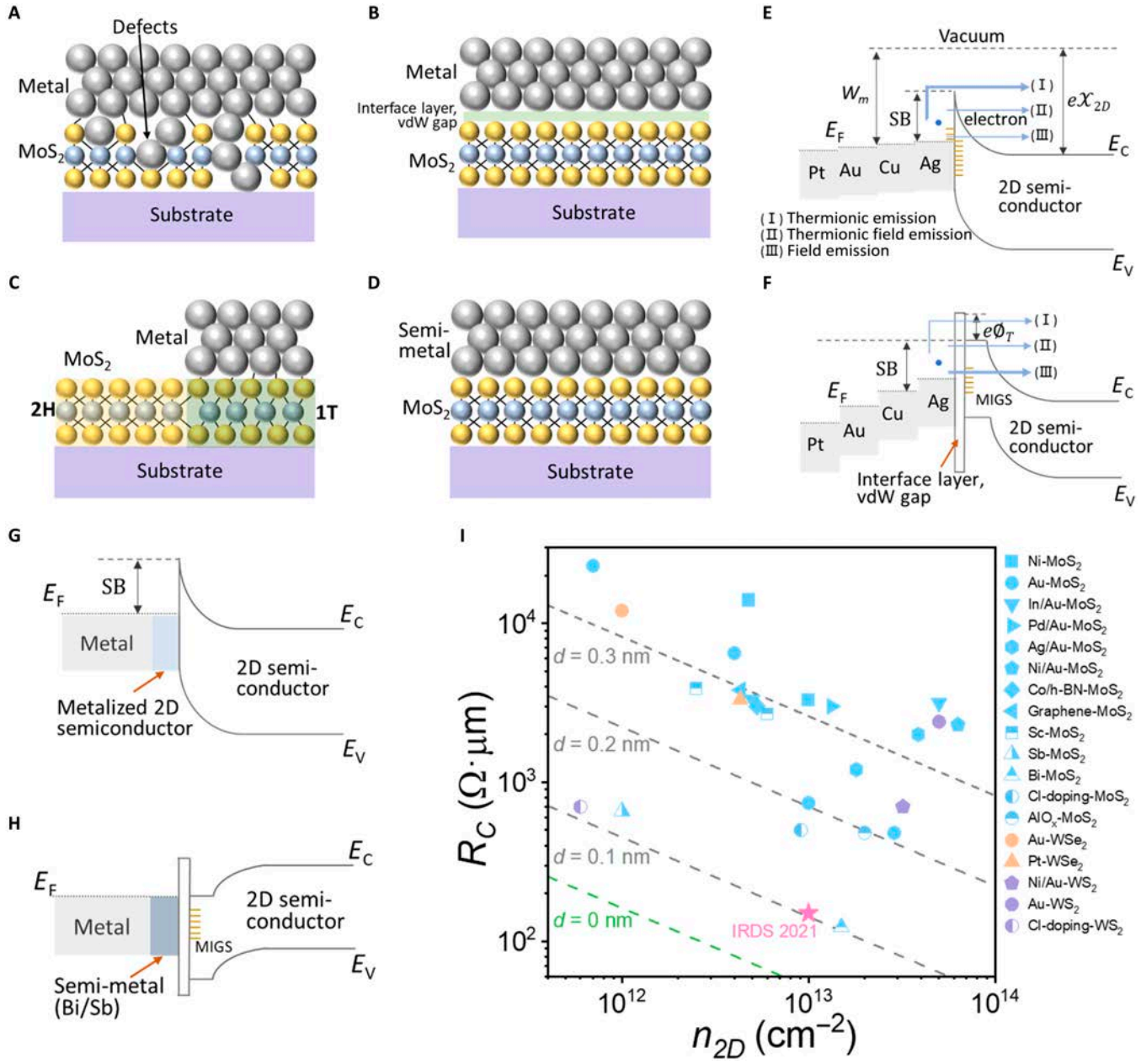


Fig. 5. Contact engineering in 2D-FETs. (A to D) Schematics of 4 kinds of contact strategies. (A) Conventional metal deposition accompanied by a lot of defects generated on MoS_2 surface. (B) Metal–insulator–semiconductor contact with a vdW gap between metal and MoS_2. (C) Metallic phase 2D materials contact. (D) Semimetal/MoS_2 contact. (E to H) Energy band diagram of different metal–2D semiconductor contacts, corresponding to the strategies of (A) to (D), respectively. There are 3 different injection mechanisms in (E) and (F), including thermionic emission (I), thermionic field emission (II), and field emission (tunneling) (III). In (E), the thermionic emission dominates. In (F), the tunneling current dominates. The yellow, dense short lines represent FLP. E_F, E_C, and E_V represent the Fermi level of the metal, and the conduction and valence bands of the 2D semiconductor, respectively. (I) Benchmark R_C for monolayer 2D semiconductors with different contacts. The dashed lines exemplify the theoretical R_c at different thicknesses of the vdW gap (d). The green dashed line ($d = 0$ nm) denotes the quantum limit for R_c approached by mature semiconductor technologies. The R_c values of WSe2, MoS2, and WS2 are reproduced from Refs. [146, 165], Refs. [110, 121, 125, 129, 133, 134, 147, 148, 166–173], and Refs. [129, 147, 174], respectively.

[122,140–143]. In addition, the graphene interface layer exhibits better conductivity and tunable Fermi level, offering more possibilities to new contact structures [144,145]. Despite that, the interface layer widens the vertical tunnel barrier ($e\varnothing_T$) between metal and 2D semiconductor (see Fig. 5F), raising R_C again. On this basis, Liu et al. proposed a laminating metal contact with weak dipole polymer as channel capping layer to create substantially disorder-free interface. The SB height was dictated by the metal's WF and thus highly tunable, approaching the Schottky–Mott limit [92]. Other researches also showed that deposition of indium and platinum at low temperature and with low diffusion energy can produce ultraclean vdW interface, which led to R_C as low as 0.8 kΩ·μm and 3.3 kΩ·μm, for n-type and p-type transistors, respectively [146,147]. Compared with the transferred electrodes, this method is more industrially compatible. Recently, Shen et al. [110] reported a new approach to make ohmic contacts for monolayer MoS_2 by using semimetallic bismuth (Bi), where MIGS were considerably

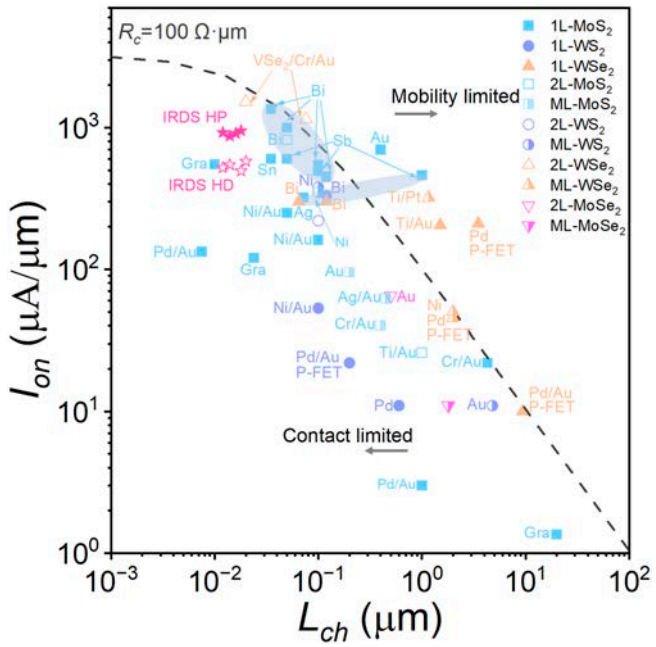


Fig. 6. Benchmark of L_{ch} versus I_{on} in 2D transistors employing different contact technologies. The gate voltage V_{gs} is the maximum reported in the respective experimental study. The blue ovals highlight semimetallic contacts such as Bi and Sb. The word "Gra" is the abbreviation of the word "Graphene". All transistors in the figure are N-FETs except the labeled P-FETs. The I_{on} values of WSe_2, MoS_2, WS_2, and $MoSe_2$ are extracted from Refs. [110, 139, 152, 154, 155, 175–180], Refs. [31, 85, 110, 135, 148, 159, 167, 169, 170, 181–189], Refs. [68, 110, 129, 185, 190–192], and Refs. [156, 193], respectively. HD, high density; HP, high performance.

suppressed and degenerate states were spontaneously generated in the TMD (Fig. 5D and H). As a result, they achieved zero SB height and a record-low R_C of 123 Ω·μm, which paved a new way toward ultralow R_C for 2D ohmic contact. Following that, a new semimetal contact of stibium (Sb) was discovered by Intel, TSMC, etc. [148], which showed similar contact characteristics to Bi but with better stability and reliability.

Finally, one can explore what are the critical factors of R_C in a vdW system. Theoretically, the quantum limit of R_C can be expressed by [149]

$$R_{c,min}W = \left(\frac{h}{2e^2}\right) e^{\frac{4\pi d\sqrt{m*(W_m+\chi_{2D})}}{h}} \sqrt{\frac{\pi}{2g_v n_s}} \qquad (3)$$

where W_m is the metal's WF, n_s is 2D sheet carrier density, h is the Planck constant, g_v is the valley degeneracy ($g_v = 2$ for monolayer vdW materials), d is the effective tunneling gap, and χ_{2D} is the affinity energy of the 2D semiconductor. According to Eq. 3, the theoretical quantum limits of R_C is linearly dependent on the tunneling gap induced by the vdW gap. As depicted in Fig. 5I, the dashed lines that represent R_c at different vdW gaps ($d = 0$ nm, 0.1 nm, 0.2 nm, and 0.3 nm) all display a strong dependency on the channel's carrier concentration. It implies that, in addition to designing a perfect vdW interface with the matched WF, enhancing the coupling between 2D semiconductor and contact metal is crucial to reduce the R_c further, approaching the quantum limit.

Driving Current Improvement of 2D Transistors

After going through the optimizations discussed above, we then focus on the most important performance parameter for IC application—I_{on}, which can be approximated as $I_{on} = V_{ds}/R_{tot}$. Figure 6 shows the measured I_{on} as a function of the channel length (L_{ch}) for monolayer 2D-FETs reported in the literature, where I_{on} is extracted at V_D equal to 1 V with maximum V_{gs}. The dashed line illustrates prediction using $R_{tot} = L_{ch}R_{sh} + 2R_C$, where the average sheet resistance of the channel $R_{sh} = (e\mu n_{2D})^{-1} \approx 1{,}524\,\Omega{\cdot}sq^{-1}$ with $n_{2D} = 10^{13}\,cm^{-2}$, $\mu = 125\,cm^2\,V^{-1}\,s^{-1}$ (IRDS 2021), $V_{ds} = 0.75$ V (IRDS 2021), and $R_C = 100$ Ω·μm. Apparently, I_{on} is significantly limited by the channel mobility for long-channel devices, but becomes strongly dependent on R_C for short-channel devices. As shown in Fig. 6, the theoretical prediction saturates as $L_{ch} < 100$ nm. In the past decade, the I_{on} of short-channel 2D-FET has been successively improved through contact and material optimizations. Nowadays, n-type MoS_2-FETs demonstrated I_{on} up to 1,135 μA/μm at $L_{ch} = 35$ nm for monolayer [110] and 1,270 μA/μm at $L_{ch} = 50$ nm for bilayer [67], respectively. In addition, the p-type 2D-FETs have also achieved several important breakthroughs recently. By modifying the vdW gap at the contact interface and employing platinum electrodes, the contact resistance of p-type few-layer WSe_2-FET has been reduced to 3.3kΩ·μm [146]. Besides, with a 20-nm-long p-type bilayer WSe_2-FET, an I_{on} of 1,720 μA/μm and a contact resistance of 250 Ω·μm have been achieved by employing the vdW–epitaxy VSe_2 contact [139], showing comparable performance to the n-type counterparts. The red star symbols in Fig. 6 indicate the future requirements for high-performance and high-density devices at technology nodes below 7 nm, respectively. The highest current density in advanced process is about 952 μA/μm at $L_{ch} = 18$ nm [9], which means that the device performance of both p-type and n-type 2D semiconductors has to meet or exceed the performance requirements of IRDS. Table summarizes the representative works with detailed metrics of performance, processes, and optimization strategies.

Summary and Prospect

To extend the relentless downscaling, Fin-FET, nanosheet FET, and envisaged Fork-sheet and CFET have been developed (see the top panel of Fig. 7). As the device scale approaches the quantum limit, some issues (e.g., the quantum confinement effect) arise. The advantages of silicon-based technology by means of node evolution, such as energy efficiency and cost, will not exist any longer. Thus, research of new semiconductors suited for industry application is inevitable. 2D-FETs attract tremendous interest for the atomically thin channels to mitigate short-channel effects and to extend "Moore's Law". In this review, we summarize the key technologies for achieving high-performance, low-power 2D-FETs through optimizations of mobility, dielectric, and contact. Finally, we show a roadmap of 2D-FET technology in Fig. 7. As for mobility, it is determined by material itself (intrinsic mobility) and impurity scattering as well. The wafer-scale growth of 2D single crystals is highly expected to break through material limitations. Meanwhile, the interface engineering is essential to reduce the number of defects and to restrain the CI scattering. For dielectric engineering, the main aim is to construct a high-quality high-κ/2D semiconductor interface and then to realize low EOT. The surface modification strategy or the selection of interfacial layer should take low D_{it}, low EOT, and low I_g all into account. For contact engineering, the key is to reduce the height and the width of SB and suppress MIGS, and then to realize stable ohmic contacts with ultralow R_C. Controllable contact-localized doping and suitable contact

Table. The state-of-the-art metrics values in TMD FETs. All values are extracted at $V_{ds} = 1$ V and $T = 300$ K. The gate voltage V_{gs} is the maximum reported in the respective experimental study. The word "Ref." is the abbreviation of the word "reference". The table is sorted by material type.

Material	Preparation method	Number of layers	μ ($cm^2 V^{-1} s^{-1}$)	Doping	Contact material	L_{ch} (μm)	I_{on} (μA/μm)	n_{2D} (10^{12} cm^{-2})	R_C (kΩ•μm)	Ref.
MoS_2	Exfoliated	2	-	N	Ti/Au	1	26	10	-	[31]
MoS_2	Exfoliated	3	47	N	Cr/Au	0.4	40	37	-	[85]
MoS_2	Exfoliated	3	-	N	Au	0.2	95	25	2.9	[188]
MoS_2	Exfoliated	3	50	N	Li phase changed	1.2	85	8	-	[135]
MoS_2	CVD	1	122.6	N	In/Au	2	18	5	3.3	[147]
MoS_2	Exfoliated	Few	167	N	In/Au	2	100	3.1	0.8	[147]
MoS_2	CVD	1	54	N	Au	1	55	-	-	[69]
MoS_2	CVD	1	102.6	N	Au	0.5	62	-	-	[29]
MoS_2	CVD	1	30	N	Ti/Au	1.6	10	4	-	[57]
MoS_2	Exfoliated	1	20	N	Bi/Au	0.035	854	15	0.123	[110]
MoS_2	CVD	2	122.6	N	Bi/Au	0.05	820	-	0.3	[67]
MoS_2	Exfoliated	1	-	N	Gra	0.01	185	4.3	5.5	[121]
WSe_2	CVD	2	-	P	VSe_2/Cr	0.02	1,520	-	0.25	[139]
WSe_2	CVD	2	100	P	VSe_2/Cr	1.8	190	-	-	[194]
WSe_2	Exfoliated	3	-	N	Au	6.2	12	-	-	[178]
WSe_2	CVD	1	-	P	Pt	1.5	8	-	229	[146]
WSe_2	Exfoliated	1	-	N	Bi/Au	0.12	323	-	-	[110]
WSe_2	Exfoliated	1	180	P	Pd/Au	2.4	34	-	10	[152]
WS_2	CVD	6	3	P	W	0.04	12	2	-	[68]
WS_2	Exfoliated	7	50	N	Ni	0.1	380	13	-	[129]
WS_2	CVD	1	21	N	Bi/Au	0.15	100	-	-	[110]
$MoSe_2$	CVD	2	3	N	Au	0.5	65	-	60	[156]

(semi)metal selection are 2 major strategies. Now, the special semimetal (Sb and Bi) contacts show great potential in this regard [110,148].

The following are several prospects of 2D transistors for future development. Although material-level progresses are the earliest and most accessible, it is still urgent to make a major breakthrough in terms of stable growth method and the relevant industry-compatible CVD reactor for making high-quality 2D semiconductor single crystals over a large area. Due to the good electrostatic control, as well as the smaller bandgap and higher mobility than monolayers, precise layer-controlled TMD single crystal (including bilayer and trilayer) epitaxy with large-area homogeneity would further boost the performance of 2D TMD devices [67]. Also, the synthesis of high-κ 2D dielectrics is another vital task that may be easily overlooked. In addition, the present methods to prepare 2D materials mainly adopt solid-phase precursors as raw materials. Their sublimation and diffusion are complex and hard to control, limiting controllability and reproducibility. Thus, the growth method based on all gaseous precursors deserves more exploration.

At the device level, as discussed before, the comprehensive optimization, including mobility, dielectric, and contact, should continue uninterruptedly until the expected target for 2D-FETs is satisfied, i.e., $\mu_e = 410$ cm^2 V^{-1} s^{-1}, $\mu_h = 219$ cm^2 V^{-1} s^{-1}, $R_C < 100$ Ω·μm at $n_{2D} = 10^{13}$ cm^{-2}, $D_{it} < 10^{10}$ cm^{-2} eV^{-1}, $EOT <$ 1 nm, and $I_g < 10^{-2}$ A·cm^{-2}, where μ_e (μ_h) is the electron (hole) mobility of n-type (p-type) 2D transistors. Achieving these performance merits actually implies the maturity of 2D-FET technology. From another point of view, the operating frequency of 2D transistors is also a recognized indicator and should be considered to systematically evaluate device performance. At present, the oscillating frequency of the reported ring oscillator based on 2D transistors is still far below 1 GHz, which hardly meets the requirement for commercial ICs. This means that, despite impressive progresses made in laboratory, more effort should be dedicated to device array and integration, i.e., not just a single transistor. Hence, more attention should be paid to their uniformity, reliability, and yield. Moreover, the CFET is the mainstream development direction for 2D transistors. Although the performance of p-type 2D-FET has made great breakthrough, its process compatibility with n-type device remains to be solved.

At the application level, although 2D-FET technology is considered to be one of the most promising candidates in the post-Moore era, it is still implausible that silicon will be fully replaced by 2D semiconductors in the foreseeable future,

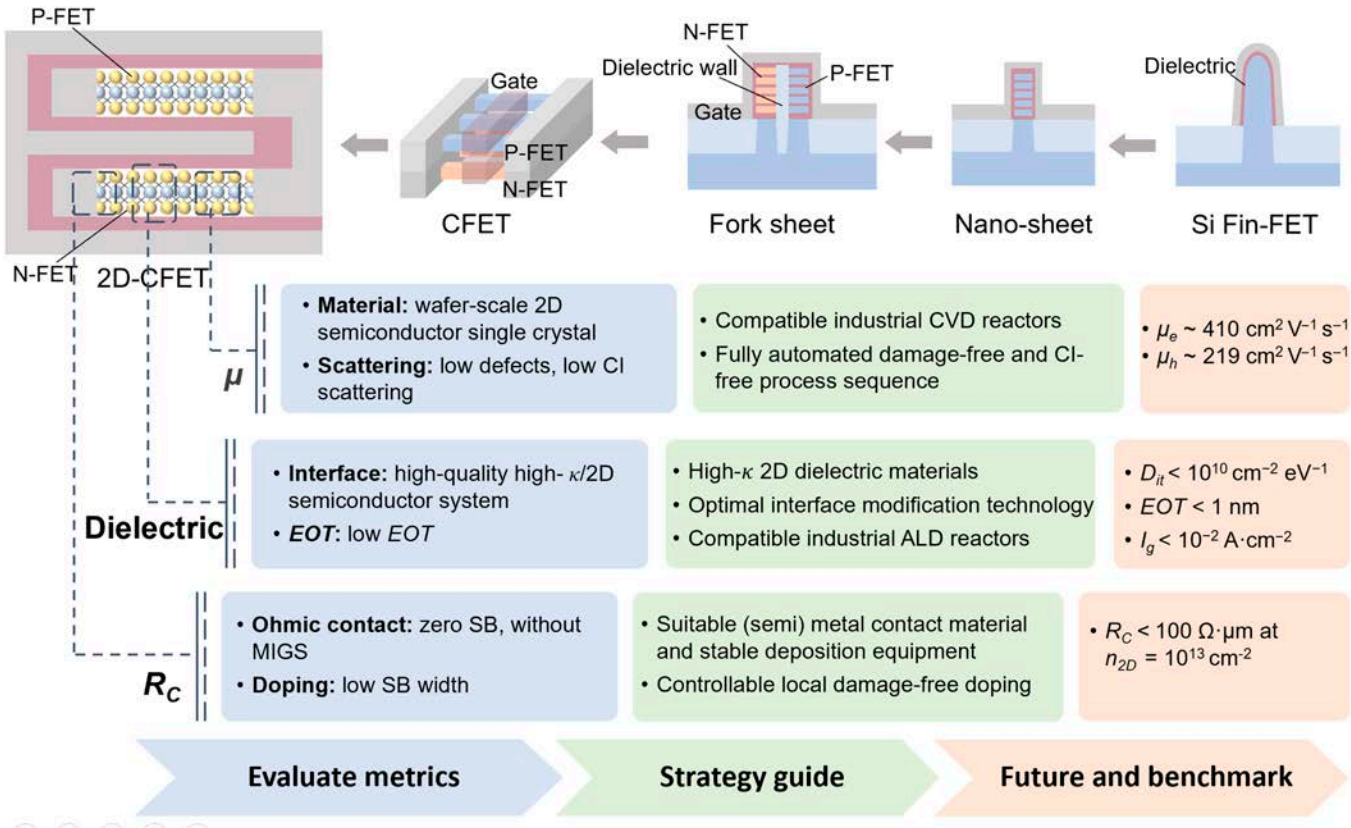


Fig. 7. Schematic visualization of transistor development and 2D-FET technology roadmap. The transistor has been structurally innovated step by step, evolving in accordance with Moore's Law and bringing huge benefits to the semiconductor industry. To bring into production, 2D-FET must overcome a series of challenges from laboratory to manufacturing infrastructure, which is outlined in the diagram.

because of the enormous investment and the immature technology to commercialize 2D transistors. For constant development, some specific "killer application" is necessary. As transferring vdW materials to arbitrary substrates is feasible under room-temperature conditions, monolithic 3D integration of 2D transistors with mainstream semiconductor technologies is a promising way, even being able to substitute the existing amorphous silicon or oxide thin-film transistor technologies. A recent demonstration of fully 3D monolithic, 1270-PPI active-matrix micro-LED displays driven by monolayer MoS_2 transistors offered a persuasive example [69]. Moreover, due to the excellent flexibility, the low integration temperature, and the outstanding optical transparency of 2D semiconductors, flexible electronics are predictable to become another essential application scenario for 2D transistors. In addition, many potential applications of 2D transistors in sensing, nonvolatile memory, and neuromorphic computing are expected to be achieved soon. Though 2D transistor technology is young, it is very appealing to bring 2D transistors into production by combining continuous process optimization and application exploration.

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Data Availability

All data used in the analysis within this paper and other finding of this study are available from the corresponding author upon reasonable request

References

1. Moore GE. Cramming more components onto integrated circuits. *Electronics*. 1965;38:114.
2. Dennard RH, Gaensslen FH, Hwa-Nien YU, Leo Rideout V, Bassous E, Leblanc AR. Design of ion-implanted MOSFETs with very small physical dimensions. *Proc IEEE*. 1999;87:668.

3. Li B, Sullivan TD, Lee TC, Badami D. Reliability challenges for copper interconnects. *Microelectron Reliab*. 2004;44:365.
4. Welser J, Hoyt JL, Takagi S-I, Gibbons JF. Strain dependence of the performance enhancement in strained-Si n-MOSFETs. Paper presented at: Technical Digest-International Electron Devices Meeting; 1994; San Francisco, CA.
5. Jovanovic V, Biasotto C, Nanver LK, Moers J, Grutzmacher D, Gerharz J, Mussler G, Van Der Cingel J, Zhang JJ, Bauer G, et al. n-Channel MOSFETs fabricated on SiGe dots for strain-enhanced mobility. *IEEE Electron Device Lett*. 2010;31:1083–1085.
6. Vogel EM. Technology and metrology of new electronic materials and devices. *Nanosci Technol*. 2009;2:166.
7. Yan RH, Ourmazd A, Lee KF. Scaling the Si MOSFET: From bulk to SOI to bulk. *IEEE Trans. Electron Devices*. 1992;39:1704–1710.
8. Iwai H. Roadmap for 22 nm and beyond (invited paper). *Microelectron Eng*. 2009;86:1520–1528.
9. International Roadmap for Devices and Systems. *International Roadmap for Devices and Systems™ 2021 Update: More Moore*. USA: IEEE; 2021.
10. Zhou J, Lin J, Huang X, Zhou Y, Chen Y, Xia J, Wang H, Xie Y, Yu H, Lei J, et al. A library of atomically thin metal chalcogenides. *Nature*. 2018;556:355–359.
11. Chhowalla M, Shin HS, Eda G, Li LJ, Loh KP, Zhang H. The chemistry of two-dimensional layered transition metal dichalcogenide nanosheets. *Nat Chem*. 2013;5:263–275.
12. Lemme MC, Akinwande D, Huyghebaert C, Stampfer C. 2D materials for future heterogeneous electronics. *Nat Commun*. 2022;13:1392.
13. Liu Y, Duan X, Shin HJ, Park S, Huang Y, Duan X. Promises and prospects of two-dimensional transistors. *Nature*. 2021;591:43–53.
14. Das S, Sebastian A, Pop E, McClellan CJ, Franklin AD, Grasser T, Knobloch T, Illarionov Y, Penumatcha AV, Appenzeller J, et al. Transistors based on two-dimensional materials for future integrated circuits. *Nat Electron*. 2021;4:786–799.
15. Akinwande D, Huyghebaert C, Wang CH, Serna MI, Goossens S, Li LJ, Wong HSP, Koppens FHL. Graphene and two-dimensional materials for silicon technology. *Nature*. 2019;573:507–518.
16. Wang S, Liu X, Zhou P. The road for 2D semiconductors in the silicon age. *Adv Mater*. 2022;34:2106886.
17. Zhu K, Wen C, Aljarb AA, Xue F, Xu X, Tung V, Zhang X, Alshareef HN, Lanza M. The development of integrated circuits based on two-dimensional materials. *Nat Electron*. 2021;4:775–785.
18. Wang Y, Chhowalla M. Making clean electrical contacts on 2D transition metal dichalcogenides. *Nat Rev Phys*. 2022;4:101.
19. Wang QH, Kalantar-Zadeh K, Kis A, Coleman JN, Strano MS. Electronics and optoelectronics of two-dimensional transition metal dichalcogenides. *Nat Nanotechnol*. 2012;7:699–712.
20. Thomas S. An industry view on two-dimensional materials in electronics. *Nat Electron*. 2021;4:856–857.
21. Shrivastava M, Ramgopal Rao V. A roadmap for disruptive applications and heterogeneous integration using two-dimensional materials: State-of-the-art and technological challenges. *Nano Lett*. 2021;21:6359–6381.
22. Chaves A, Azadani JG, Alsalman H, da Costa DR, Frisenda R, Chaves AJ, Song SH, Kim YD, He D, Zhou J, et al. Bandgap engineering of two-dimensional semiconductor materials. *NPJ 2D Mater Appl*. 2020;4:29.
23. Cui F, Feng Q, Hong J, Wang R, Bai Y, Li X, Liu D, Zhou Y, Liang X, He X, et al. *Adv Mater*. 2017;29:1.
24. Yue Y, Feng Y, Chen J, Zhang D, Feng W. Two-dimensional large-scale bandgap-tunable monolayer $MoS_{2(1-x)}Se_2x$/graphene heterostructures for phototransistors. *J Mater Chem C*. 2017;5:5887–5896.
25. Yin W-J, Wen B, Nie G-Z, Wei X-L, Liu L-M. Tunable dipole and carrier mobility for a few layer Janus MoSSe structure. *J Mater Chem C*. 2018;6:1693–1700.
26. Yu ZG, Cai Y, Zhang Y-W. Robust direct bandgap characteristics of one- and two-dimensional ReS_2. *Sci Rep*. 2015;5:13783.
27. Hosseini M, Elahi M, Pourfath M, Esseni D. Strain-induced modulation of electron mobility in single-layer transition metal dichalcogenides MX_2 (M=Mo , W; X=S, Se). *IEEE Trans Electron Devices*. 2015;62:3192–3198.
28. Kalanyan B, Kimes WA, Beams R, Stranick SJ, Garratt E, Kalish I, Davydov AV, Kanjolia RK, Maslar JE. Rapid wafer-scale growth of polycrystalline 2H-MoS_2 by pulsed metalorganic chemical vapor deposition. *Chem Mater*. 2017;29:6279–6288.
29. Li T, Guo W, Ma L, Li W, Yu Z, Han Z, Gao S, Liu L, Fan D, Wang Z, et al. Epitaxial growth of wafer-scale molybdenum disulfide semiconductor single crystals on sapphire. *Nat Nanotechnol*. 2021;16:1201–1207.
30. Li MY, Shi Y, Cheng CC, Lu LS, Lin YC, Tang HL, Tsai ML, Chu CW, Wei KH, He JH, et al. Epitaxial growth of a monolayer WSe_2-MoS_2 lateral p-n junction with an atomically sharp interface. *Science*. 2015;349:524–528.
31. Wang H, Yu L, Lee YH, Shi Y, Hsu A, Chin ML, Li LJ, Dubey M, Kong J, Palacios T. Integrated circuits based on bilayer MoS_2 transistors. *Nano Lett*. 2012;12:4674–4680.
32. Wan Y, Li E, Yu Z, Huang JK, Li MY, Chou AS, Te Lee Y, Lee CJ, Hsu HC, Zhan Q, et al. Low-defect-density WS_2 by hydroxide vapor phase deposition. *Nat Commun*. 2022;13:4149.
33. Yu Z, Ong ZY, Li S, Bin Xu J, Zhang G, Zhang YW, Shi Y, Wang X. Analyzing the carrier mobility in transition-metal dichalcogenide MoS_2 field-effect transistors. *Adv Funct Mater*. 2017;27:1604093.
34. Yu Z, Pan Y, Shen Y, Wang Z, Ong ZY, Xu T, Xin R, Pan L, Wang B, Sun L, et al. Towards intrinsic charge transport in monolayer molybdenum disulfide by defect and interface engineering. *Nat Commun*. 2014;5:5290.
35. Kaasbjerg K, Thygesen KS, Jacobsen KW. Phonon-limited mobility in n-type single-layer MoS_2 from first principles. *Phys Rev B*. 2012;85:115317.
36. Laikhtman B, Solomon PM. Remote phonon scattering in field-effect transistors with a high κ insulating layer. *J Appl Phys*. 2008;103:014501.
37. Fischetti MV, Neumayer DA, Cartier EA. Effective electron mobility in Si inversion layers in metal–oxide–semiconductor systems with a high-κ insulator: The role of remote phonon scattering. *J Appl Phys*. 2001;90:4587.
38. Zhao Y, Qiao J, Yu Z, Yu P, Xu K, Lau SP, Zhou W, Liu Z, Wang X, Ji W, et al. High-electron-mobility and air-stable 2D layered $PtSe_2$ FETs. *Adv Mater*. 2017;29:1604230.
39. Yu Z, Ong ZY, Pan Y, Cui Y, Xin R, Shi Y, Wang B, Wu Y, Chen T, Zhang YW, et al. Realization of room-temperature phonon-limited carrier transport in monolayer MoS_2 by dielectric and carrier screening. *Adv Mater*. 2016;28:547–552.

40. Radisavljevic B, Kis A. Mobility engineering and a metal–insulator transition in monolayer MoS_2. *Nat Mater*. 2013;12:815–820.
41. Liu Y, Wu H, Cheng HC, Yang S, Zhu E, He Q, Ding M, Li D, Guo J, Weiss NO, et al. Toward barrier free contact to molybdenum disulfide using graphene electrodes. *Nano Lett*. 2015;15:3030–3034.
42. Baugher BWH, Churchill HOH, Yang Y, Jarillo-Herrero P. Intrinsic electronic transport properties of high-quality monolayer and bilayer MoS_2. *Nano Lett*. 2013;13:4212–4216.
43. Qiu H, Xu T, Wang Z, Ren W, Nan H, Ni Z, Chen Q, Yuan S, Miao F, Song F, et al. Hopping transport through defect-induced localized states in molybdenum disulphide. *Nat Commun*. 2013;4:2642.
44. Ma N, Jena D. Charge scattering and mobility in atomically thin semiconductors. *Phys Rev X*. 2014;4:011043.
45. Ong Z-Y, Fischetti MV. Mobility enhancement and temperature dependence in top-gated single-layer MoS_2. *Phys Rev B*. 2013;88:165316.
46. Maldague PF. Many-body corrections to the polarizability of the two-dimensional electron gas. *Surf Sci*. 1978;73:296–302.
47. Cui X, Lee GH, Kim YD, Arefe G, Huang PY, Lee CH, Chenet DA, Zhang X, Wang L, Ye F, et al. Multi-terminal transport measurements of MoS_2 using a van der Waals heterostructure device platform. *Nat Nanotechnol*. 2015;10:534–540.
48. Xu S, Wu Z, Lu H, Han Y, Long G, Chen X, Han T, Ye W, Wu Y, Lin J, et al. Universal low-temperature Ohmic contacts for quantum transport in transition metal dichalcogenides. *2D Mater*. 2016;3:021007.
49. Chee SS, Seo D, Kim H, Jang H, Lee S, Moon SP, Lee KH, Kim SW, Choi H, Ham MH. Lowering the Schottky barrier height by graphene/Ag electrodes for high-mobility MoS_2 field-effect transistors. *Adv Mater*. 2019;31:1804422.
50. Han A, Aljarb A, Liu S, Li P, Ma C, Xue F, Lopatin S, Yang CW, Huang JK, Wan Y, et al. Growth of 2H stacked WSe_2 bilayers on sapphire. *Nanoscale Horiz*. 2019;4:1434–1442.
51. Yu H, Liao M, Zhao W, Liu G, Zhou XJ, Wei Z, Xu X, Liu K, Hu Z, Deng K, et al. Wafer-scale growth and transfer of highly-oriented monolayer MoS_2 continuous films. *ACS Nano*. 2017;11:12001–12007.
52. Song JG, Hee Ryu G, Kim Y, Je Woo W, Yong Ko K, Kim Y, Lee C, Oh IK, Park J, Lee Z, et al. Catalytic chemical vapor deposition of large-area uniform two-dimensional molybdenum disulfide using sodium chloride. *Nanotechnology*. 2017;28:465103.
53. Jeon W, Cho Y, Jo S, Ahn JH, Jeong SJ. Wafer-scale synthesis of reliable high-mobility molybdenum disulfide thin films via inhibitor-utilizing atomic layer deposition. *Adv Mater*. 2017;29:1703031.
54. Zhang J, Wang JH, Chen P, Sun Y, Wu S, Jia ZY, Lu XB, Yu H, Chen W, Zhu JQ, et al. Observation of strong interlayer coupling in MoS_2/WS_2 heterostructures. *Adv Mater*. 2016;1950–1956.
55. Shi Y, Li H, Li LJ. Recent advances in controlled synthesis of two-dimensional transition metal dichalcogenides via vapour deposition techniques. *Chem Soc Rev*. 2015;44:2744–2756.
56. Chen W, Zhao J, Zhang J, Gu L, Yang Z, Li X, Yu H, Zhu X, Yang R, Shi D, et al. Oxygen-assisted chemical vapor deposition growth of large single-crystal and high-quality monolayer MoS_2. *J Am Chem Soc*. 2015;137:15632–15635.
57. Kang K, Xie S, Huang L, Han Y, Huang PY, Mak KF, Kim CJ, Muller D, Park J. High-mobility three-atom-thick semiconducting films with wafer-scale homogeneity. *Nature*. 2015;520:656–660.
58. Docherty CJ, Parkinson P, Joyce HJ, Chiu MH, Chen CH, Lee MY, Li LJ, Herz LM, Johnston MB. Ultrafast transient terahertz conductivity of monolayer MoS_2 and WSe_2 grown by chemical vapor deposition. *ACS Nano*. 2014;8:11147–11153.
59. Chen CH, Wu CL, Pu J, Chiu MH, Kumar P, Takenobu T, Li LJ. Hole mobility enhancement and *p* -doping in monolayer WSe_2 by gold decoration. *2D Mater*. 2014;1:034001.
60. Chang YH, Zhang W, Zhu Y, Han Y, Pu J, Chang JK, Hsu WT, Huang JK, Hsu CL, Chiu MH, et al. Monolayer $MoSe_2$ grown by chemical vapor deposition for fast photodetection. *ACS Nano*. 2014;8:8582–8590.
61. Wang X, Gong Y, Shi G, Chow WL, Keyshar K, Ye G, Vajtai R, Lou J, Liu Z, Ringe E, et al. Chemical vapor deposition growth of crystalline monolayer $MoSe_2$. *ACS Nano*. 2014;8:5125–5131.
62. Pu J, Yomogida Y, Liu KK, Li LJ, Iwasa Y, Takenobu T. Highly flexible MoS_2 thin-film transistors with ion gel dielectrics. *Nano Lett*. 2012;12:4013–4017.
63. Zhou J, Lin J, Sims H, Jiang C, Cong C, Brehm JA, Zhang Z, Niu L, Chen Y, Zhou Y, et al. *Adv Mater*. 2020;32:1.
64. Liu KK, Zhang W, Lee YH, Lin YC, Chang MT, Su CY, Chang CS, Li H, Shi Y, Zhang H, et al. Growth of large-area and highly crystalline MoS2 thin layers on insulating substrates. *Nano Lett*. 2012;12:1538–1544.
65. Huang J-K, Pu J, Hsu C-L, Chiu M-H, Juang Z-Y, Chang Y-H, Chang W-H, Iwasa Y, Takenobu T, Li L-J. Large-area synthesis of highly crystalline WSe_2 monolayers and device applications. *ACS Nano*. 2014;8:923–930.
66. Lee Y-H, Zhang X-Q, Zhang W, Chang M-T, Te Lin C, Di Chang K, Yu Y-C, Wang JT-W, Chang C-S, Li L-J, et al. Synthesis of large-area MoS_2 atomic layers with chemical vapor deposition. *Adv Mater*. 2012;24:2320–2325.
67. Liu L, Li T, Ma L, Li W, Gao S, Sun W, Dong R, Zou X, Fan D, Shao L, et al. Uniform nucleation and epitaxy of bilayer molybdenum disulfide on sapphire. *Nature*. 2022;605:69–75.
68. Cheng CC, Chung YY, Li UY, Lin CT, Li CF, Chen JH, Lai TY, Li KS, Shieh JM, Su SK, et al. First demonstration of 40-nm channel length top-gate WS2 pFET using channel area-selective CVD growth directly on SiOx/Si substrate. *Dig Tech Pap - Symp VLSI Technol*. 2019;2019-June:T244.
69. Meng W, Xu F, Yu Z, Tao T, Shao L, Liu L, Li T, Wen K, Wang J, He L, et al. Three-dimensional monolithic micro-LED display driven by atomically thin transistor matrix. *Nat Nanotechnol*. 2021;16:1231–1236.
70. Wang J, Xu X, Cheng T, Gu L, Qiao R, Liang Z, Ding D, Hong H, Zheng P, Zhang Z, et al. Dual-coupling-guided epitaxial growth of wafer-scale single-crystal WS_2 monolayer on vicinal *a*-plane sapphire. *Nat Nanotechnol*. 2022;17:33–38.
71. Bian R, Li C, Liu Q, Cao G, Fu Q, Meng P, Zhou J, Liu F, Liu Z. Recent progress in the synthesis of novel two-dimensional van der Waals materials. *Nat Sci Rev*. 2022;9:nwab164.
72. Tang B, Che B, Xu M, Ang ZP, Di J, Gao H-J, Yang H, Zhou J, Liu Z. Recent advances in synthesis and study of 2D twisted transition metal dichalcogenide bilayers. *Small Struct*. 2021;2:2000153.

73. Wang Q, Li N, Tang J, Zhu J, Zhang Q, Jia Q, Lu Y, Wei Z, Yu H, Zhao Y, et al. Wafer-scale highly oriented monolayer MoS_2 with large domain sizes. *Nano Lett*. 2020;20:7193–7199.
74. Xiao Z, Guojia F, Jiawei W, Xun H, Haoning W, Nishuang L, Hao L, Xingzhong Z. Improved subthreshold swing and gate-bias stressing stability of p-type Cu_2O thin-film transistors using a HfO_2 high-κ gate dielectric grown on a SiO_2/Si substrate by pulsed laser ablation. *Electron Devices IEEE Trans*. 2003;2011:58.
75. Usha C, Vimala P. An electrostatic analytical modeling of high-k stacked gate-all-around heterojunction tunnel FETs considering the depletion regions. *AEU Int J Electron Commun*. 2019;110:152877.
76. Higashi S, Abe D, Hiroshima Y, Miyashita K, Kawamura T, Inoue S, Shimoda T. High-quality SiO_2/Si interface formation and its application to fabrication of low-temperature-processed polycrystalline Si thin-film transistor. *Japanese J Appl Physics, Part 1 Regul Pap Short Notes Rev Pap*. 2002;41:3646.
77. Ogawa A, Iwamoto K, Ota H, Morita Y, Ikeda M, Nabatame T, Toriumi A. 0.6 nm-EOT high-k gate stacks with $HfSiO_x$ interfacial layer grown by solid-phase reaction between HfO_2 and Si substrate. *Microelectron Eng*. 2007;84:1861–1864.
78. Huang B, Zheng M, Zhao Y, Wu J, Thong JTL. Atomic layer deposition of high-quality Al_2O_3 thin films on MoS_2 with water plasma treatment. *ACS Appl Mater Interfaces*. 2019;11:35438–35443.
79. Schwartzberg AM, Olynick D. Complex materials by atomic layer deposition. *Adv Mater*. 2015;27:5778–5784.
80. Azcatl A, McDonnell S, Santosh KC, Peng X, Dong H, Qin X, Addou R, Mordi GI, Lu N, Kim J, et al. MoS_2 functionalization for ultra-thin atomic layer deposited dielectrics. *Appl Phys Lett*. 2014;104:111601.
81. Cheng L, Qin X, Lucero AT, Azcatl A, Huang J, Wallace RM, Cho K, Kim J. Atomic layer deposition of a high-*k* dielectric on MoS_2 using trimethylaluminum and ozone. *ACS Appl Mater Interfaces*. 2014;6:11834–11838.
82. McDonnell SJ, Wallace RM. UV-ozone functionalization of 2D materials. *JOM*. 2019;71:224–237.
83. Xiao M, Qiu C, Zhang Z, Peng L-M. Atomic-layer-deposition growth of an ultrathin HfO_2 film on graphene. *ACS Appl Mater Interfaces*. 2017;9:34050–34056.
84. Choi MS, Lee M, Ngo TD, Hone J, Yoo WJ. Chemical dopant-free doping by annealing and electron beam irradiation on 2D materials. *Adv Electron Mater*. 2021;7:2100449.
85. Zou X, Wang J, Chiu CH, Wu Y, Xiao X, Jiang C, Wu WW, Mai L, Chen T, Li J, et al. Interface engineering for high-performance top-gated MoS_2 field-effect transistors. *Adv Mater*. 2014;26:6255–6261.
86. Kim S, Nah J, Jo I, Shahrjerdi D, Colombo L, Yao Z, Tutuc E, Banerjee SK. Realization of a high mobility dual-gated graphene field-effect transistor with Al_2O_3 dielectric. *Appl Phys Lett*. 2009;94:062107.
87. Son S, Yu S, Choi M, Kim D, Choi C. Improved high temperature integration of Al_2O_3 on MoS_2 by using a metal oxide buffer layer. *Appl Phys Lett*. 2015;106:021601.
88. Takahashi N, Nagashio K. Buffer layer engineering on graphene via various oxidation methods for atomic layer deposition. *Appl Phys Express*. 2016;9:125101.
89. Xu J, Wen M, Zhao X, Liu L, Song X, Lai PT, Tang WM. Effects of HfO_2 encapsulation on electrical performances of few-layered MoS_2 transistor with ALD HfO_2 as back-gate dielectric. *Nanotechnology*. 2018;29:345201.
90. Xiang L, Zhang H, Dong G, Zhong D, Han J, Liang X, Zhang Z, Peng LM, Hu Y. Low-power carbon nanotube-based integrated circuits that can be transferred to biological surfaces. *Nat Electron*. 2018;1:237–247.
91. Sekitani T, Yokota T, Kuribara K, Kaltenbrunner M, Fukushima T, Inoue Y, Sekino M, Isoyama T, Abe Y, Onodera H, et al. Ultraflexible organic amplifier with biocompatible gel electrodes. *Nat Commun*. 2016;7:Article 11425.
92. Liu Y, Guo J, Zhu E, Liao L, Lee SJ, Ding M, Shakir I, Gambin V, Huang Y, Duan X. Approaching the Schottky-Mott limit in van der Waals metal-semiconductor junctions. *Nature*. 2018;557(7707):696–700.
93. Lai S, Byeon S, Jang SK, Lee J, Lee BH, Park JH, Kim YH, Lee S. HfO_2/HfS_2 hybrid heterostructure fabricated *via* controllable chemical conversion of two-dimensional HfS_2. *Nanoscale*. 2018;10(39):18758–18766.
94. Li T, Tu T, Sun Y, Fu H, Yu J, Xing L, Wang Z, Wang H, Jia R, Wu J, et al. A native oxide high-κ gate dielectric for two-dimensional electronics. *Nat Electron*. 2020;3:473–478.
95. Wang X, Tabakman SM, Dai H. Atomic layer deposition of metal oxides on pristine and functionalized graphene. *J Am Chem Soc*. 2008;130(26):8152–8153.
96. Li W, Zhou J, Cai S, Yu Z, Zhang J, Fang N, Li T, Wu Y, Chen T, Xie X, et al. Uniform and ultrathin high-κ gate dielectrics for two-dimensional electronic devices. *Nat Electron*. 2019;2:563–571.
97. Yu Z, Ning H, Cheng CC, Li W, Liu L, Meng W, Luo Z, Li T, Cai S, Wang P, et al. Reliability of ultrathin high-κ dielectrics on chemical-vapor deposited 2D semiconductors. Paper presented at: 66th Annual IEEE International Electron Devices Meeting, IEDM; 2020 Dec 12–18; Virtual, San Francisco.
98. Liu K, Jin B, Han W, Chen X, Gong P, Huang L, Zhao Y, Li L, Yang S, Hu X, et al. A wafer-scale van der Waals dielectric made from an inorganic molecular crystal film. *Nat Electron*. 2021;4:906–913.
99. Vu QA, Fan S, Lee SH, Joo MK, Yu WJ, Lee YH. Near-zero hysteresis and near-ideal subthreshold swing in h-BN encapsulated single-layer MoS_2 field-effect transistors. *2D Mater*. 2018;5:Article 031001.
100. Kim TW, Ra HS, Ahn J, Jang J, Taniguchi T, Watanabe K, Shim JW, Lee YT, Hwang DK. Frequency doubler and universal logic gate based on two-dimensional transition metal dichalcogenide transistors with low power consumption. *ACS Appl Mater Interfaces*. 2021;13(6):7470–7475.
101. Illarionov YY, Banshchikov AG, Polyushkin DK, Wachter S, Knobloch T, Thesberg M, Mennel L, Paur M, Stöger-Pollach M, Steiger-Thirsfeld A, et al. Ultrathin calcium fluoride insulators for two-dimensional field-effect transistors. *Nat Electron*. 2019;2:230–235.
102. Wen C, Banshchikov AG, Illarionov YY, Frammelsberger W, Knobloch T, Hui F, Sokolov NS, Grasser T, Lanza M. Dielectric properties of ultrathin CaF_2 ionic crystals. *Adv Mater*. 2020;32(4):Article 2002525.
103. Huang JK, Wan Y, Shi J, Zhang J, Wang Z, Wang W, Yang N, Liu Y, Lin CH, Guan X, et al. High-κ perovskite membranes as insulators for two-dimensional transistors. *Nature*. 2022;605:262–267.
104. Robertson J. High dielectric constant oxides. *Eur Phys J Appl Phys*. 2004;28:265–291.
105. Krivokapic Z, Rana U, Galatage R, Razavieh A, Aziz A, Liu J, Shi J, Kim HJ, Sporer R, Serrao C, et al. 14 nm Ferroelectric

FinFET technology with steep subthreshold slope for ultra low power applications. *Tech Dig - Int Electron Devices Meet IEDM*. 2018;15.1.1.
106. Sood A, Xiong F, Chen S, Cheaito R, Lian F, Asheghi M, Cui Y, Donadio D, Goodson KE, Pop E. *Nano Lett*. 2019;19:2434.
107. Lai GT, Peng HK, Chen YF, Teng SC, Chou CP, Kao YC, Wu PJ, Wu YH. Improved contact resistivity and transconductance for sub-10 nm FinFET technology by laser-induced contact silicide. *IEEE Trans Nanotechnol*. 2021;20:761–764.
108. Cohen ML. Schottky and Bardeen limits for Schottky barriers. *J Vac Sci Technol*. 1979;16(5):1135.
109. Bardeen J. Surface states and rectification at a metal semi-conductor contact. *Phys Rev*. 1947;71(10):717–727.
110. Shen PC, Su C, Lin Y, Chou AS, Cheng CC, Park JH, Chiu MH, Lu AY, Tang HL, Tavakoli MM, et al. Ultralow contact resistance between semimetal and monolayer semiconductors. *Nature*. 2021;593:211–217.
111. Wager JF, Robertson J. Metal-induced gap states modeling of metal-Ge contacts with and without a silicon nitride ultrathin interfacial layer. *J Appl Phys*. 2011;109(9):Article 094501.
112. Mönch W. Barrier heights of real Schottky contacts explained by metal-induced gap states and lateral inhomogeneities. *J Vac Sci Technol B Microelectron Nanometer Struct*. 1999;17:1867–1876.
113. Sajjad M, Yang X, Altermatt P, Singh N, Schwingenschlögl U, De Wolf S. Metal-induced gap states in passivating metal/silicon contacts. *Appl Phys Lett*. 2019;114(7):Article 071601.
114. Zhang M, Knoch J, Zhao QT, Lenk S, Breuer U, Mantl S, Schottky barrier height modulation using dopant segregation in Schottky-barrier SOI-MOSFETs. Paper presented at: Proceedings of 35th European Solid-State Device Research Conference; 2005 Sept 16; Grenoble, France.
115. Connelly D, Faulkner C, Grupp DE, Harris JS. A new route to zero-barrier metal source/drain MOSFETs. *IEEE Trans Nanotechnol*. 2004;3(1):98–104.
116. Kaneko A, Yagishita A, Yahashi K, Kubota T, Omura M, Matsuo K, Mizushima I, Okano K, Kawasaki H, Izumida T, et al. High-performance FinFET with dopant-segregated Schottky source/drain. *Tech Dig - Int Electron Devices Meet IEDM*. 2006;6.
117. Song S, Sim Y, Kim SY, Kim JH, Oh I, Na W, Lee DH, Wang J, Yan S, Liu Y, et al. Wafer-scale production of patterned transition metal ditelluride layers for two-dimensional metal-semiconductor contacts at the Schottky-Mott limit. *Nat Electron*. 2020;3(4):207–215.
118. Shen T, Ren JC, Liu X, Li S, Liu W. van der Waals stacking induced transition from Schottky to ohmic contacts: 2D metals on multilayer InSe. *J Am Chem Soc*. 2019;141(7):3110–3115.
119. Lv C, Yan W, Shieh TH, Zhao Y, Wu G, Zhao Y, Lv Y, Zhang D, Chen Y, Arora SK, et al. Electrical contact barriers between a three-dimensional metal and layered SnS_2. *Mater Interfaces*. 2020;12(13):15830–15836.
120. LaGasse SW, Dhakras P, Watanabe K, Taniguchi T, Lee JU. Gate-tunable graphene–WSe_2 heterojunctions at the Schottky–Mott limit. *Adv Mater*. 2019;31:2.
121. Xie L, Liao M, Wang S, Yu H, Du L, Tang J, Zhao J, Zhang J, Chen P, Lu X, et al. Graphene-contacted ultrashort channel monolayer MoS_2 transistors. *Adv Mater*. 2017;29(37):Article 1702522.
122. Kim GS, Kim SH, Park J, Han KH, Kim J, Yu HY. Schottky barrier height engineering for electrical contacts of multilayered MoS_2 transistors with reduction of metal-induced gap states. *ACS Nano*. 2018;12(6):6292–6300.
123. Kim C, Moon I, Lee D, Choi MS, Ahmed F, Nam S, Cho Y, Shin HJ, Park S, Yoo WJ. Fermi level pinning at electrical metal contacts of monolayer molybdenum dichalcogenides. *ACS Nano*. 2017;11(2):1588–1596.
124. Das S, Chen HY, Penumatcha AV, Appenzeller J. High performance multilayer MoS_2 transistors with scandium contacts. *Nano Lett*. 2013;13(1):100–105.
125. Cui X, Shih EM, Jauregui LA, Chae SH, Kim YD, Li B, Seo D, Pistunova K, Yin J, Park JH, et al. Low-temperature ohmic contact to monolayer MoS_2 by van der Waals bonded Co/h-BN electrodes. *Nano Lett*. 2017;17:4781–4786.
126. Gong C, Colombo L, Wallace RM, Cho K. the unusual mechanism of partial Fermi level pinning at metal–MoS_2 interfaces. *Nano Lett*. 2014;14(4):1714–1720.
127. Hemanjaneyulu K, Kumar J, Shrivastava M. MoS_2 doping using potassium iodide for reliable contacts and efficient FET operation. *IEEE Trans Electron Devices*. 2019;66:3224–3228.
128. Kim B-K, Choi D-H, Kim H, Watanabe K, Taniguchi T, Rho H, Kim J-J, Bae M-H, Genuine ohmic van der Waals contact between indium and MoS2. arXiv. 3 May 2019. https://doi.org/10.48550/arXiv.1904.10295.
129. Yang L, Majumdar K, Liu H, Du Y, Wu H, Hatzistergos M, Hung PY, Tieckelmann R, Tsai W, Hobbs C, et al. Chloride molecular doping technique on 2D Materials: WS_2 and MoS_2. *Nano Lett*. 2014;14:6275–6280.
130. Gao Z, Zhou Z, Tománek D. Degenerately doped transition metal dichalcogenides as ohmic homojunction contacts to transition metal dichalcogenide semiconductors. *ACS Nano*. 2019;13(5):5103–5111.
131. McClellan CJ, Yalon E, Smithe KKH, Suryavanshi SV, Pop E. Effective n-type doping of monolayer MoS_2 by AlO_x. *Device Res Conf - Conf Dig DRC* 2017;4329:1.
132. Suh J, Park TE, Lin DY, Fu D, Park J, Jung HJ, Chen Y, Ko C, Jang C, Sun Y, et al. Doping against the native propensity of MoS_2: Degenerate hole doping by cation substitution. *Nano Lett*. 2014;14(12):6976–6982.
133. McClellan CJ, Yalon E, Smithe KKH, Suryavanshi SV, Pop E. High current density in monolayer MoS_2 doped by AlO_x. *ACS Nano*. 2021;15(1):1587–1596.
134. Das S, Appenzeller J. Where does the current flow in two-dimensional layered systems? *Nano Lett*. 2013;13(7):3396–3402.
135. Kappera R, Voiry D, Yalcin SE, Branch B, Gupta G, Mohite AD, Chhowalla M. Phase-engineered low-resistance contacts for ultrathin MoS_2 transistors. *Nat Mater*. 2014;13(12):1128–1134.
136. Song S, Keum DH, Cho S, Perello D, Kim Y, Lee YH. Room temperature semiconductor-metal transition of $MoTe_2$ thin films engineered by strain. *Nano Lett*. 2016;16(1):188–193.
137. Cho S, Kim S, Kim JH, Zhao J, Seok J, Keum DH, Baik J, Choe DH, Chang KJ, Suenaga K, et al. Phase patterning for ohmic homojunction contact in $MoTe_2$. *Science*. 2015;349(6248):625–628.
138. Zhu J, Wang Z, Yu H, Li N, Zhang J, Meng J, Liao M, Zhao J, Lu X, Du L, et al. Argon plasma induced phase transition in monolayer MoS_2. *J Am Chem Soc*. 2017;139(30):10216–10219.
139. Wu R, Tao Q, Li J, Li W, Chen Y, Lu Z, Shu Z, Zhao B, Ma H, Zhang Z, et al. Bilayer tungsten diselenide transistors with on-state currents exceeding 1.5 milliamperes per micrometre. *Nat Electron*. 2022;5:497–504.

140. Lee S, Tang A, Aloni S, Philip Wong HS. Statistical study on the Schottky barrier reduction of tunneling contacts to CVD synthesized MoS_2. *Nano Lett*. 2016;16(1):276–281.
141. Jang J, Kim Y, Chee SS, Kim H, Whang D, Kim GH, Yun SJ. Clean interface contact using a ZnO interlayer for low-contact-resistance MoS_2 transistors. *Appl ACS Mater Interfaces*. 2020;12(4):5031–5039.
142. Wang J, Yao Q, Huang CW, Zou X, Liao L, Chen S, Fan Z, Zhang K, Wu W, Xiao X, et al. High mobility MoS_2 transistor with low Schottky barrier contact by using atomic thick h-BN as a tunneling layer. *Adv Mater*. 2016;28(37):8302–8308.
143. Andrews K, Bowman A, Rijal U, Chen PY, Zhou Z. Improved contacts and device performance in MoS_2 transistors using a 2D semiconductor interlayer. *ACS Nano*. 2020;14(5):6232–6241.
144. Yu L, Lee YH, Ling X, Santos EJG, Shin YC, Lin Y, Dubey M, Kaxiras E, Kong J, Wang H, et al. Graphene/MoS_2 hybrid technology for large-scale two-dimensional electronics. *Nano Lett*. 2014;14(6):3055–3063.
145. Kwak JY, Hwang J, Calderon B, Alsalman H, Munoz N, Schutter B, Spencer MG. Electrical characteristics of multilayer MoS_2 FET's with MoS_2/graphene heterojunction contacts. *Nano Lett*. 2014;14(8):4511–4516.
146. Wang Y, Kim JC, Li Y, Ma KY, Hong S, Kim M, Shin HS, Jeong HY, Chhowalla M. P-type electrical contacts for two-dimensional transition metal dichalcogenides. *Nature*. 2022;610:61–66.
147. Wang Y, Kim JC, Wu RJ, Martinez J, Song X, Yang J, Zhao F, Mkhoyan A, Jeong HY, Chhowalla M. Van der Waals contacts between three-dimensional metals and two-dimensional semiconductors. *Nature*. 2019;568:(7750)70–74.
148. Chou AS, Wu T, Cheng CC, Zhan SS, Ni IC, Wang SY, Chang YC, Liew SL, Chen E, Chang WH, et al. Antimony semimetal contact with enhanced thermal stability for high performance 2D electronics. *Tech Dig - Int Electron Devices Meet IEDM*. 2021;2021-Decem:7.2.1.
149. Somvanshi D, Kallatt S, Venkatesh C, Nair S, Gupta G, Anthony JK, Karmakar D, Majumdar K. Nature of carrier injection in metal/2D-semiconductor interface and its implications for the limits of contact resistance. *Phys Rev B*. 2017;96:205423.
150. Cho M, Aoulaiche M, Degraeve R, Kaczer B, Franco J, Kauerauf T, Roussel P, Ragnarsson LÅ, Tseng J, Hoffmann TY, et al. Paper presented at: Proceedings of the International Reliability Physics Symposium; 2010 May 2–6; Anaheim, CA.
151. Kuo C-S, Hsu J-F, Huang S-W, Lee LS, Tsai M-J, Hwu J-G. High-k Al_2O_3 gate dielectrics prepared by oxidation of aluminum film in nitric acid followed by high-temperature annealing. *IEEE Trans Electron Devices*. 2004;51:854–858.
152. Allain A, Kis A. Electron and hole mobilities in single-layer WSe_2. *ACS Nano*. 2014;8:7180–7185.
153. Wang Y, Yang RX, Quhe R, Zhong H, Cong L, Ye M, Ni Z, Song Z, Yang J, Shi J, et al. Does p-type ohmic contact exist in WSe_2–metal interfaces? *Nanoscale*. 2016;8:1179–1191.
154. Chiang CC, Lan HY, Pang CS, Appenzeller J, Chen Z. Air-stable P-doping in record high-performance monolayer WSe_2 devices. *IEEE Electron Device Lett*. 2022;43:319–322.
155. Movva HCP, Rai A, Kang S, Kim K, Fallahazad B, Taniguchi T, Watanabe K, Tutuc E, Banerjee SK. High-mobility holes in dual-gated WSe_2 field-effect transistors. *ACS Nano*. 2015;9:10402–10410.
156. Somvanshi D, Ber E, Bailey CS, Pop E, Yalon E. Improved current density and contact resistance in bilayer $MoSe_2$ field effect transistors by AlO_x capping. *ACS Appl Mater Interfaces*. 2020;12:36355–36361.
157. Li Y, Zhang K, Wang F, Feng Y, Li Y, Han Y, Tang D, Zhang B. Scalable synthesis of highly crystalline $MoSe_2$ and its ambipolar behavior. *ACS Appl Mater Interfaces*. 2017;9:36009–36016.
158. Quereda J, Ghiasi TS, You JS, van den Brink J, van Wees BJ, van der Wal CH. Symmetry regimes for circular photocurrents in monolayer $MoSe_2$. *Nat Commun*. 2018;9:3346.
159. Sebastian A, Pendurthi R, Choudhury TH, Redwing JM, Das S. Benchmarking monolayer MoS_2 and WS_2 field-effect transistors. *Nat Commun*. 2021;12:Article 693.
160. Choi J-H, Park Y-J, Min H-S. Electron mobility behavior in extremely thin SOI MOSFET's. *IEEE Electron Device Lett*. 1995;16:527–529.
161. Wong HSP, Franks DJ, Solomon PM. Device design considerations for double-gate, ground-plane, and single-gated ultra-thin SOI MOSFET's at the 25 nm channel length generation. *Tech Dig IEEE Int Electron Devices Meet*. 1998;407–410.
162. Esseni D, Mastrapasqua M, Celler GK, Fiegna C, Selmi L, Sangiorgi E. An experimental study of mobility enhancement in ultrathin SOI transistors operated in double-gate mode. *IEEE Trans Electron Devices*. 2003;50:802–808.
163. Uchida K, Watanabe H, Kinoshita A, Koga J, Numata T, Takagi S. Experimental study on carrier transport mechanism in ultrathin-body SOI nand p-MOSFETs with SOI thickness less than 5 nm. *Digest Int Electron Devices Meet*. 2002;47–50.
164. Esseni D, Mastrapasqua M, Celler GK, Baumann FH, Fiegn C, Selmi L, Sangiorgi E. Low field mobility of ultra-thin SOI N- and P-MOSFETs: Measurements and implications on the performance of ultra-short MOSFETs. *Tech Dig - Int Electron Devices Meet*. 2000;671.
165. Yue D, Kim C, Lee KY, Yoo WJ. Ohmic contact in 2D semiconductors via the formation of a benzyl viologen interlayer. *Adv Funct Mater*. 2019;29(7):Article 1807338.
166. Sanne A, Ghosh R, Rai A, Yogeesh MN, Shin SH, Sharma A, Jarvis K, Mathew L, Rao R, Akinwande D, et al. Radio frequency transistors and circuits based on CVD moS_2. *Nano Lett*. 2015;15(8):5039–5045.
167. Zhu Y, Li Y, Arefe G, Burke RA, Tan C, Hao Y, Liu X, Liu X, Yoo WJ, Dubey M, et al. Monolayer molybdenum disulfide transistors with single-atom-thick gates. *Nano Lett*. 2018;18(6):3807–3813.
168. Smithe KKH, Suryavanshi SV, Muñoz Rojo M, Tedjarati AD, Pop E. Low variability in synthetic monolayer MoS2 devices. *ACS Nano*. 2017;11(8):8456–8463.
169. Chou AS, Cheng CC, Liew SL, Ho PH, Wang SY, Chang YC, Chang CK, Su YC, Da Huang Z, Fu FY, et al. High on-state current in chemical vapor deposited monolayer MoS_2 nFETs with Sn ohmic contacts. *IEEE Electron Device Lett*. 2021;42(2):272–275.
170. Yalon E, McClellan CJ, Smithe KKH, Muñoz Rojo M, Xu RL, Suryavanshi SV, Gabourie AJ, Neumann CM, Xiong F, Farimani AB, et al. Energy dissipation in monolayer MoS2 electronics. *Nano Lett*. 2017;17(6):3429–3433.
171. Rai A, Valsaraj A, Movva HCP, Roy A, Ghosh R, Sonde S, Kang S, Chang J, Trivedi T, Dey R, et al. Air stable doping and intrinsic mobility enhancement in monolayer molybdenum

disulfide by amorphous titanium suboxide encapsulation. *Nano Lett*. 2015;15(7):4329–4336.
172. Zheng X, Calò A, Albisetti E, Liu X, Alharbi ASM, Arefe G, Liu X, Spieser M, Yoo WJ, Taniguchi T, et al. Patterning metal contacts on monolayer MoS_2 with vanishing Schottky barriers using thermal nanolithography. *Nat Electron*. 2019;2:17–25.
173. Smithe KKH, English CD, Suryavanshi SV, Pop E. Intrinsic electrical transport and performance projections of synthetic monolayer MoS_2 devices. *2D Mater*. 2017;4:Article 011009.
174. Guimarães MHD, Gao H, Han Y, Kang K, Xie S, Kim CJ, Muller DA, Ralph DC, Park J. Atomically thin ohmic edge contacts between two-dimensional materials. *ACS Nano*. 2016;10(6):6392–6399.
175. Liu W, Kang J, Sarkar D, Khatami Y, Jena D, Banerjee K. Role of metal contacts in designing high-performance monolayer n-type WSe_2 field effect transistors. *Nano Lett*. 2013;13(5):1983–1990.
176. Fang H, Chuang S, Chang TC, Takei K, Takahashi T, Javey A. High-performance single layered WSe_2 p-FETs with chemically doped contacts. *Nano Lett*. 2012;12(7):3788–3792.
177. Lin YC, Jariwala B, Bersch BM, Xu K, Nie Y, Wang B, Eichfeld SM, Zhang X, Choudhury TH, Pan Y, et al. Realizing large-scale, electronic-grade two-dimensional semiconductors. *ACS Nano*. 2018;12(2):965–975.
178. Fang H, Tosun M, Seol G, Chang TC, Takei K, Guo J, Javey A. Degenerate n-doping of few-layer transition metal dichalcogenides by potassium. *Nano Lett*. 2013;13(5):1991–1995.
179. Pang CS, Hung TYT, Khosravi A, Addou R, Wang Q, Kim MJ, Wallace RM, Chen Z. Atomically controlled tunable doping in high-performance WSe_2 devices. *Adv Electron Mater*. 2020;6(8):Article 1901304.
180. Das S, Appenzeller J. WSe2 field effect transistors with enhanced ambipolar characteristics. *Appl Phys Lett*. 2013;103(10):Article 103501.
181. Nourbakhsh A, Zubair A, Dresselhaus MS, Palacios T. Transport properties of a MoS_2/WSe_2 heterojunction transistor and its potential for application. *Nano Lett*. 2016;16(2):1359–1366.
182. Sharma D, Motayed A, Shah PB, Amani M, Georgieva M, Glen Birdwell A, Dubey M, Li Q, Davydov AV. Transfer characteristics and low-frequency noise in single- and multi-layer MoS_2 field-effect transistors. *Appl Phys Lett*. 2015;107(16):Article 162102.
183. Najmaei S, Liu Z, Zhou W, Zou X, Shi G, Lei S, Yakobson BI, Idrobo JC, Ajayan PM, Lou J. Vapour phase growth and grain boundary structure of molybdenum disulphide atomic layers. *Nat Mater*. 2013;12(8):754–759.
184. Lin Y, Shen PC, Su C, Chou AS, Wu T, Cheng CC, Park JH, Chiu MH, Lu AY, Tang HL, et al. Contact engineering for high-performance N-type 2D semiconductor transistors. Paper presented at: 2021 IEEE International Electron Devices Meeting, IEDM; 2021 Dec 11–16; San Francisco, CA.
185. O'Brien KP, Dorow CJ, Penumatcha A, Maxey K, Lee S, Naylor CH, Hsiao A, Holybee B, Rogan C, Adams D, et al. Advancing 2D monolayer CMOS through contact, channel and interface engineering. *Tech Dig - Int Electron Devices Meet IEDM* 2021;*2021-Decem*:7.1.1.
186. Li W, Fan D, Shao L, Huang F, Liang L, Li T, Xu Y, Tu X, Wang P, Yu Z, et al. High-performance CVD MoS2 transistors with self-aligned top-gate and Bi contact. Paper presented at: 2021 IEEE International Electron Devices Meeting; 2021 Dec 11–16; San Francisco, CA.
187. Si M, Su CJ, Jiang C, Conrad NJ, Zhou H, Maize KD, Qiu G, Wu CT, Shakouri A, Alam MA, et al. Steep-slope hysteresis-free negative capacitance MoS_2 transistors. *Nat Nanotechnol*. 2018;13(1):24–28.
188. Krasnozhon D, Dutta S, Nyffeler C, Leblebici Y, Kis A. High-frequency, scaled MoS2 transistors. *Tech Dig - Int Electron Devices Meet IEDM*. 2015; *2016-Febru*, 27.4.1.
189. Liu X, Sun G, Chen P, Liu J, Zhang Z, Li J, Ma H, Zhao B, Wu R, Dang W, et al. High-performance asymmetric electrodes photodiode based on Sb/WSe_2 heterostructure. *Nano Res*. 2019;12:339–344.
190. Dorow CJ, O'Brien KP, Naylor CH, Lee S, Penumatcha A, Hsiao A, Tronic T, Christenson M, Maxey K, Zhu H, et al. Advancing monolayer 2D NMOS and PMOS transistor integration from growth to van der Waals interface engineering for ultimate CMOS scaling. *Dig Tech Pap - Symp VLSI Technol*. 2021;*2021-June*:6592.
191. Lin D, Wu X, Cott D, Verreck D, Groven B, Sergeant S, Smets Q, Sutar S, Asselberghs I, Radu I, et al. Dual gate synthetic WS_2 MOSFETs with 120 μS/μm Gm 2.7 μF/cm^2 capacitance and ambipolar channel. *Int. Electron Devices Meet IEDM*. 2020;*2020-Decem*, 3.6.1.
192. Liu X, Hu J, Yue C, Della Fera N, Ling Y, Mao Z, Wei J. High performance field-effect transistor based on multilayer tungsten disulfide. *ACS Nano*. 2014;8(10):10396–10402.
193. Larentis S, Fallahazad B, Tutuc E. Field-effect transistors and intrinsic mobility in ultra-thin $MoSe_2$ layers. *Appl Phys Lett*. 2012;101(22):Article 223104.
194. Li J, Yang X, Liu Y, Huang B, Wu R, Zhang Z, Zhao B, Ma H, Dang W, Wei Z, et al. General synthesis of two-dimensional van der Waals heterostructure arrays. *Nature*. 2020;579(7799):368–374.