Graph Theory-Based Sneak Circuit Time-Domain Analysis and Trigger of CLLC Resonant Converter With Parasitic Parameters

Chengsong WEI, Xiaoquan ZHU, Ke JIN, and Yue WU

***Abstract*—The sneak circuits caused by internal parasitic parameters can lead to unexpected phenomena and affect the efficiency and reliability of CLLC resonant converter. Therefore, the characteristic analysis, trigger mechanism and suppression method of CLLC converter sneak circuit based on graph theory are proposed in this paper. The complete current based sneak circuit model and accurate CLLC time domain model are established. Then, the possible sneak circuit phenomena are described in detail to explain their negative effects on the converter operating characteristics, the trigger mechanism of sneak operating modes is put forward, and the suppression conditions are derived. By optimizing the parameter design and modulation parameters of CLLC converter, the unexpected sneak circuits can be avoided. Finally, the correctness of theoretical analysis is verified by experiment results, and the proposed suppression method avoids unnecessary power loss and suppresses the waveform oscillations.**

***Index Terms*—CLLC converter, graph theory, parasitic parameters, sneak circuit, time-domain analysis.**

I. Introduction

With the rapid development of electric vehicles (EVs), energy storage systems, and new energy resources, bidirectional dc-dc converters have attracted more and more attention [1], [2]. Bidirectional resonant dc converter has been widely used in these applications as the key device [3]−[5] because the LC resonance process makes both the primary and secondary side currents low-distortion sinusoids, so the switching loss can be kept small while transmitting high power. CLLC converter, as one of the best bidirectional dc converters, is a hot research topic in recent years. However, the dynamic nature of parasitic parameters can lead to waveform oscillations during converter operation [6]. This leads to unexpected sneak circuit phenomena, which will reduce the efficiency and reliability of CLLC converter. Hence, there is a requirement to implement sneak-circuit modeling, analysis and suppression of CLLC converter with parasitic parameters.

Currently, the design of CLLC is mainly based on fundamental harmonic approximation (FHA) analysis method, and the parasitic parameters of switching devices are ignored during the design process, which will lead to unfavorable effects [7]. Thus, time domain analysis method is an effective way to study CLLC resonant converter with parasitic parameters [8]. The current research articles mainly focus on the effect of parasitic parameters on switching performance [9], [10], electromagnetic interference [11], [12], and converter characterization of power converters [13]. Furthermore, considering operation modes with parasitic capacitances, the zero voltage switching (ZVS) behavior is discussed in [14], and the axis and center symmetric (ACS) method was proposed based on currents decomposition to achieve “Sync-ZVS”. Considering the modes that include parasitic capacitances, the ZVS behavior is discussed in references [15], [16]. However, parasitic parameters and its dynamic characteristics can lead to unexpected operating modes and cause nonlinear behavior of the components, such as oscillations in voltage and current, which are detrimental to the converter operating modes but are rarely discussed in existing work.

To further distinguish the difference between sneak and normal operation modes, the sneak circuit analysis method was proposed in [17]. Sneak circuit analysis has two steps: one is sneak path analysis, which identifies the sneak current paths appearing in the converter. And the other is sneak mode analysis, which predicts sneak circuit phenomena [18]. For the sneak path analysis, the existing methods include grid combination analysis [19] and graph-theoretic analysis [20], [21]. However, there is no literature on the sneak operating modes analysis of CLLC resonant converters. Therefore, it is necessary to analyze the sneak circuit phenomena of CLLC converter and build its complete time domain model to get the trigger conditions of the unexpected sneak circuit.

For sneak mode analysis, the existing research articles mainly focus on conventional pulse width modulation (PWM) dc-dc converters such as boost [22] and flyback converters [23]. They all have discontinuous conduction modes, so there are current discontinuity intervals in these PWM dc converters. For the CLLC resonant converter, it also has current discontinuity

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intervals due to uncontrolled parasitic diodes on the secondary side, while other discontinuity intervals still exist. In the previous analysis, CLLC converter was considered to stop operating during discontinuous current intervals [24]. However, when parasitic elements are considered, currents flow inside the parasitic elements [25] and present sneak operating modes, which will severely affect the converter operating features, such as unstable output characteristics, lower efficiency and higher switching stress [26]. Nevertheless, there are few studies on the sneak circuits analysis when considering the dynamic characteristics of parasitic capacitance in CLLC converter. Therefore, it is necessary to enhance the mechanism analysis of sneak circuits and provide a comprehensive summary of the possible sneak circuit phenomena in CLLC converter.

The trigger mechanism is a prerequisite for suppressing the sneak circuit phenomenon without changing the topology structure. There are four main types of trigger mechanisms and suppression methods: (1) Parameter design: Avoid the appearance of sneak circuits through reasonable parameter design, so that the converter works in the normal operating mode. (2) Topology improvement: The sneak circuit path can be cut off by changing the converter topology based on the characteristics of sneak circuit path. Although this method can eliminate the hazards of sneak circuits, changing the converter topology may create new sneak circuit paths or affect the converter performance. (3) Modulation optimization: The triggering of sneak circuit phenomenon is also related to the control method. Literature [23] devised an optimized duty cycle to suppress the sneak circuit phenomenon. This method can suppress the sneak circuit without changing circuit structure. (4) Switching device selection optimization: Literature [27] reduced the switching loss of SiC MOSFET with the help of existing parasitic components. The influence of parasitic parameters on switched-capacitor converters performance has been investigated in [28], and corresponding design methods have been proposed.

The selection of suitable sneak circuit elimination method should consider the converter actual situation. For converters with sneak circuits that have clear trigger conditions, parametric design, modulation optimization, and optimal selection of switching devices method can be selected. While, for converters with unclear sneak circuit trigger conditions, the topology improvement method would be a better choice.

However, the detailed study of trigger mechanism and suppression method of sneak circuit phenomenon in CLLC resonant converter requires accurate modeling, so the FHA analysis method is not applicable. To address the above problems, this paper adopts a graph-theory based method for analyzing, triggering and suppressing the CLLC sneak circuit phenomenon when considering parasitic parameters. The CLLC resonant converter is accurately modeled and analyzed in the time domain, and the method to suppress the appearance of sneak circuits is proposed. The contributions of this article are given as follows.

1) On the basis of graph theory, a path classification method based on resonant inductor currents is proposed and a complete system of sneak modality applicable to resonant converters is obtained.

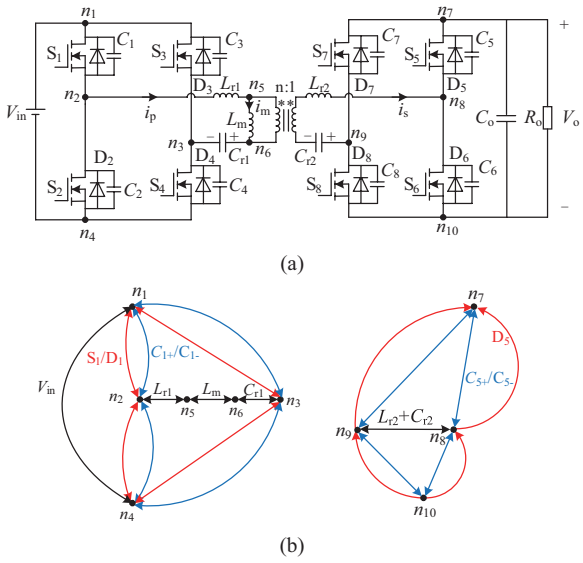

Fig. 1. CLLC with parasitic parameters. (a) Topology. (b) Directed graph of CLLC.

2) Through the time-domain modeling of CLLC converter, the sneak circuit phenomenon is analyzed in detail, and the negative effects of sneak circuit on system operation features and the sneak phenomenon are explained.

3) The trigger mechanism of the sneak modality of CLLC converter is investigated and listed in the form of a time series, which reveals the influence of the converter parameters as well as the modulation parameters on the converter operating state, and the suppression conditions are deduced to improve the efficiency as well as the reliability of CLLC converter.

In contrast to previous studies, the sneak modality of CLLC resonant converter is comprehensively modeled, analyzed, and suppressed in this paper to improve the system efficiency and reliability.

II. The Sneak Circuit Paths Graph Analysis of CLLC Based on Current Direction and Switch State

A. Graph-Theoretic Modeling of CLLC Converter With Parasitic Parameters

The CLLC resonant converter topology considering parasitic parameters is shown in Fig. 1(a). V_{in} and V_o are the input and output voltages, respectively. C_o is the output filter capacitor. R_o is load resistance. The turns ratio of transformer is n:1. L_{r1} and L_{r2} are the primary and secondary side resonant inductors. C_{r1} and C_{r2} are the primary and secondary side resonant capacitors. L_m is the transformer excitation inductance. There are eight MOSFETs S_1–S_8 in CLLC converter, as well as anti-parallel diodes D_1–D_8. Considering the parasitic capacitance of semiconductors, they are equivalent to the parasitic capacitance C_{oss} in parallel with the MOSFETs. C_1–C_8 are connected in parallel with switches S_1–S_8.

The topology of CLLC is modeled as the directed graph in Fig. 1(b). The current and voltage directions labeled in Fig. 1(a)

are defined as positive directions. The direction from node n_1 to node n_2 is the charging direction of capacitor C_1. The capacitor charging direction is defined as the positive direction, denoted as C_{1+}. The edge from n_2 to n_1 is defined as the discharge direction and is denoted as C_{1-}. Similarly, the charging and discharging directions of C_2–C_8 are defined in the same way. According to the graph theory, the connection matrices are established for both the primary and secondary sides of CLLC converter, as shown in (1) and (2).

$$\begin{bmatrix} 1 & \mathrm{S}_1+C_{1+} & \mathrm{S}_3+C_{3+} & V_{\mathrm{in}} & 0 & 0 \\ \mathrm{D}_1+C_{1-} & 1 & 0 & \mathrm{S}_2+C_{2+} & L_{\mathrm{r}1+} & 0 \\ \mathrm{D}_3+C_{3-} & 0 & 1 & \mathrm{S}_4+C_{4+} & 0 & C_{\mathrm{r}1-} \\ V_{\mathrm{in}} & \mathrm{D}_2+C_{2-} & \mathrm{D}_4+C_{4-} & 1 & 0 & 0 \\ 0 & L_{\mathrm{r}1-} & 0 & 0 & 1 & L_{\mathrm{m}+} \\ 0 & 0 & C_{\mathrm{r}1+} & 0 & L_{\mathrm{m}-} & 1 \end{bmatrix} \tag{1}$$

$$\begin{bmatrix} 1 & C_{5+} & C_{7+} & V_{\mathrm{o}} \\ \mathrm{D}_5+C_{5-} & 1 & L_{\mathrm{r}2-}+C_{\mathrm{r}2-} & C_{6+} \\ \mathrm{D}_7+C_{7-} & L_{\mathrm{r}2+}+C_{\mathrm{r}2+} & 1 & C_{8+} \\ V_{\mathrm{o}} & \mathrm{D}_6+C_{6-} & \mathrm{D}_8+C_{8-} & 1 \end{bmatrix} \tag{2}$$

When modeling the directed graph of CLLC, it is worth noting that the bidirectional CLLC converter operates in forward direction with S_1 and S_4 conduct synchronously on the primary side, S_2 and S_3 conduct complementary to S_1 and S_4, and the secondary side achieves current rectification by using the parasitic diode of MOSFETs. At the same time, to simplify the calculation of current path, L_{m} and the primary side winding of transformer are combined into L_{m} in the directed graph and connection matrix. The primary side current of the transformer is determined by its secondary side current.

Therefore, all circuit paths in CLLC converter can be found by the determinants of connection matrices (1) and (2). And feasible current paths can be selected based on the basic rules and modulation method of the circuit.

B. Current Analysis Based on Current Direction and Switch State

In practice, the current path between primary and secondary sides of CLLC converter is determined by i_{p} and i_{s}. In normal operation, each mode of CLLC is mainly decided by the switching state (ON or OFF) and current direction.

According to the proposed method, all possible combinations of switching states and the corresponding normal circuits are listed in Table I. Sneak current circuits on primary and secondary sides are classified according to the direction of the current as shown in Table II. According to (1) and (2), the parasitic parameters can cause CLLC converter to generate different sneak circuits during actual operation. This may lead to unexpected operating modes during current conversion [22]. By connecting the primary and secondary side current paths, the complete sneak circuit paths of CLLC converter can be obtained. The complete sneak circuit operating mode during power conversion consists of charging and discharging

TABLE I
NORMAL CIRCUIT BASED ON CURRENT DIRECTION AND SWITCH STATE

Primary Side		
$\mathrm{S}_1\mathrm{S}_2\mathrm{S}_3\mathrm{S}_4$	$i_{\mathrm{p}}>0$	$i_{\mathrm{p}}<0$
0000	$\mathrm{D}_2L_{\mathrm{r}1+}L_{\mathrm{m}+}C_{\mathrm{r}1+}\mathrm{D}_3V_{\mathrm{in}}$	$\mathrm{D}_1L_{\mathrm{r}1-}L_{\mathrm{m}-}C_{\mathrm{r}1-}\mathrm{D}_4V_{\mathrm{in}}$
1001	$V_{\mathrm{in}}\mathrm{S}_1L_{\mathrm{r}1+}L_{\mathrm{m}+}C_{\mathrm{r}1+}\mathrm{S}_4$	$\mathrm{D}_1L_{\mathrm{r}1-}L_{\mathrm{m}-}C_{\mathrm{r}1-}\mathrm{D}_4V_{\mathrm{in}}$
0110	$\mathrm{D}_2L_{\mathrm{r}1-}L_{\mathrm{m}-}C_{\mathrm{r}1-}\mathrm{D}_3V_{\mathrm{in}}$	$V_{\mathrm{in}}\mathrm{S}_2L_{\mathrm{r}1-}L_{\mathrm{m}-}C_{\mathrm{r}1-}\mathrm{S}_3$
Secondary side		
$\mathrm{S}_5\mathrm{S}_6\mathrm{S}_7\mathrm{S}_8$	$i_{\mathrm{s}}>0$	$i_{\mathrm{s}}<0$
0000	$\mathrm{D}_5\mathrm{D}_8L_{\mathrm{r}2+}C_{\mathrm{r}2+}V_{\mathrm{o}}$	$\mathrm{D}_6\mathrm{D}_7L_{\mathrm{r}2-}C_{\mathrm{r}2-}V_{\mathrm{o}}$

TABLE II
SNEAK CIRCUIT BASED ON CURRENT DIRECTION AND SWITCH STATE

Primary Side		
$\mathrm{S}_1\mathrm{S}_2\mathrm{S}_3\mathrm{S}_4$	$i_{\mathrm{p}}>0$	$i_{\mathrm{p}}<0$
0000	$C_{1+}L_{\mathrm{r}1+}L_{\mathrm{m}+}C_{\mathrm{r}1+}C_{3-}C_{4+}L_{\mathrm{r}1+}$ $L_{\mathrm{m}+}C_{\mathrm{r}1+}C_{2-}$ $C_{1+}L_{\mathrm{r}1+}L_{\mathrm{m}+}C_{\mathrm{r}1+}\mathrm{D}_3$ $C_{4+}L_{\mathrm{r}1+}L_{\mathrm{m}+}C_{\mathrm{r}1+}\mathrm{D}_2$ $C_{1+}L_{\mathrm{r}1+}L_{\mathrm{m}+}C_{\mathrm{r}1+}C_{4+}V_{\mathrm{in}}$ $C_{2-}L_{\mathrm{r}1+}L_{\mathrm{m}+}C_{\mathrm{r}1+}C_{3-}V_{\mathrm{in}}$	$C_{3+}L_{\mathrm{r}1-}L_{\mathrm{m}-}C_{\mathrm{r}1-}C_{1-}$ $C_{2+}L_{\mathrm{r}1-}L_{\mathrm{m}-}C_{\mathrm{r}1-}C_{4-}$ $C_{3+}L_{\mathrm{r}1-}L_{\mathrm{m}-}C_{\mathrm{r}1-}\mathrm{D}_1$ $C_{2+}L_{\mathrm{r}1-}L_{\mathrm{m}-}C_{\mathrm{r}1-}\mathrm{D}_4$ $C_{2+}L_{\mathrm{r}1-}L_{\mathrm{m}-}C_{\mathrm{r}1-}C_{3+}V_{\mathrm{in}}$ $C_{1-}L_{\mathrm{r}1-}L_{\mathrm{m}-}C_{\mathrm{r}1-}C_{4-}V_{\mathrm{in}}$
1001	$\mathrm{S}_1L_{\mathrm{r}1+}L_{\mathrm{m}+}C_{\mathrm{r}1+}C_{3-}$ $\mathrm{S}_4L_{\mathrm{r}1+}L_{\mathrm{m}+}C_{\mathrm{r}1+}C_{2-}$	---
0110	---	$\mathrm{S}_3L_{\mathrm{r}1-}L_{\mathrm{m}-}C_{\mathrm{r}1-}C_{1-}$; $\mathrm{S}_2L_{\mathrm{r}1-}L_{\mathrm{m}-}C_{\mathrm{r}1-}C_{4-}$
Secondary side		
$\mathrm{S}_5\mathrm{S}_6\mathrm{S}_7\mathrm{S}_8$	$i_{\mathrm{s}}>0$	$i_{\mathrm{s}}<0$
0000	$C_{7+}C_{5-}L_{\mathrm{r}2+}C_{\mathrm{r}2+}$ $C_{6+}C_{8-}L_{\mathrm{r}2+}C_{\mathrm{r}2+}$ $C_{7+}\mathrm{D}_5L_{\mathrm{r}2+}C_{\mathrm{r}2+}$ $C_{6+}\mathrm{D}_8L_{\mathrm{r}2+}C_{\mathrm{r}2+}$ $C_{6+}C_{7+}L_{\mathrm{r}2+}C_{\mathrm{r}2+}V_{\mathrm{o}}$ $C_{5-}C_{8-}L_{\mathrm{r}2+}C_{\mathrm{r}2+}V_{\mathrm{o}}$	$C_{7-}C_{5+}L_{\mathrm{r}2-}C_{\mathrm{r}2-}$ $C_{6-}C_{8+}L_{\mathrm{r}2-}C_{\mathrm{r}2-}$ $C_{5+}\mathrm{D}_7L_{\mathrm{r}2-}C_{\mathrm{r}2-}$ $C_{8+}\mathrm{D}_6L_{\mathrm{r}2-}C_{\mathrm{r}2-}$ $C_{5+}C_{8+}L_{\mathrm{r}2+}C_{\mathrm{r}2+}V_{\mathrm{o}}$ $C_{6-}C_{7-}L_{\mathrm{r}2-}C_{\mathrm{r}2-}V_{\mathrm{o}}$

parasitic capacitors on the same bridge arm. Since the CLLC converter adopts a symmetrical operation mode, only the positive half-cycle sneak operation mode is analyzed. The other half-cycle of the sneak circuit is symmetrical. The corresponding sneak circuit modes are shown in Table III. A complete model of the sneak circuit is developed by using the path analysis method based on current direction to characterize the dynamics of parasitic capacitors in CLLC converter, where the dynamic voltage of the parasitic capacitors excites the sneak circuit and degrades the performance of converter.

III. SNEAK MODALITY ANALYSIS

In order to avoid the appearance of unexpected sneak modality, their trigger conditions need to be determined. Therefore, an unabridged time-domain model of CLLC is required. The converter modulation method affects the trigger conditions of sneak circuits, and since the quasi-resonant state can be regarded as a special state of the under-resonant state, it will be analyzed in two categories: under-resonant modulation and over-resonant modulation.

Before theoretical analysis, the following assumptions are made:

1) The parasitic capacitances C_1–C_8 of MOSFETs are equal and their values are C_{oss};

TABLE III
SNEAK MODALITY OF CLLC CONVERTER

Modality	Switch state	Current direction	The paths of primary side	The paths of secondary side
Normal modality 1	---	$i_p<0$, $i_s>0$	$D_1L_{r1}.L_m.C_{r1}.D_4V_{in}$	$D_8C_{r2}+L_{r2}+D_5V_o$
Normal modality 2	S_1S_4	$i_p>0$, $i_s>0$	$V_{in}S_1L_{r1}+L_{m+}C_{r1}+S_4$	$D_8C_{r2}+L_{r2}+D_5V_o$
Sneak modality 1	S_1S_4	$i_p>0$, $i_s<0$	$V_{in}S_1L_{r1}+L_{m+}C_{r1}+S_4$	$C_7.C_5+L_{r2}.C_{r2}.C_6.C_8+L_{r2}.C_{r2}.$
Sneak modality 2	S_1S_4	$i_p>0$, $i_s<0$	$V_{in}S_1L_{r1}+L_{m+}C_{r1}+S_4$	$D_6D_7L_{r2}.C_{r2}.V_o$
Sneak modality 3	S_1S_4	$i_p>0$, $i_s>0$	$V_{in}S_1L_{r1}+L_{m+}C_{r1}+S_4$	$C_7.C_5+L_{r2}+C_{r2}+C_6+C_8.L_{r2}+C_{r2}+$
Sneak modality 4	---	$i_p>0$, $i_s<0$	$C_1+L_{r1}+L_{m+}C_{r1}+C_3.;C_4+L_{r1}+L_{m+}C_{r1}+C_2.$	$C_7.C_5+L_{r2}.C_{r2}.C_6.C_8+L_{r2}.C_{r2}.$
Sneak modality 5	---	$i_p>0$, $i_s<0$	$D_2L_{r1}+L_{m+}C_{r1}+D_3V_{in}$	$C_7.C_5+L_{r2}.C_{r2}.C_6.C_8+L_{r2}.C_{r2}.$
Sneak modality 6	---	$i_p>0$, $i_s<0$	$D_2L_{r1}+L_{m+}C_{r1}+D_3V_{in}$	$D_6D_7L_{r2}.C_{r2}.V_o$
Sneak modality 7	---	$i_p>0$ and $i_p<0$, $i_s<0$	$C_1+L_{r1}+L_{m+}C_{r1}+C_3.;C_4+L_{r1}+L_{m+}C_{r1}+C_2.;C_3+L_{r1}.L_m.C_{r1}.C_1.;C_2+L_{r1}.L_m.C_{r1}.C_4.$	$D_6D_7L_{r2}.C_{r2}.V_o$
Sneak modality 8	---	$i_p>0$, $i_s>0$	$C_1+L_{r1}+L_{m+}C_{r1}+C_3.;C_4+L_{r1}+L_{m+}C_{r1}+C_2.$	$D_8C_{r2}+L_{r2}+D_5V_o$
Sneak modality 9	---	$i_p>0$, $i_s>0$	$D_2L_{r1}+L_{m+}C_{r1}+D_3V_{in}$	$D_8C_{r2}+L_{r2}+D_5V_o$

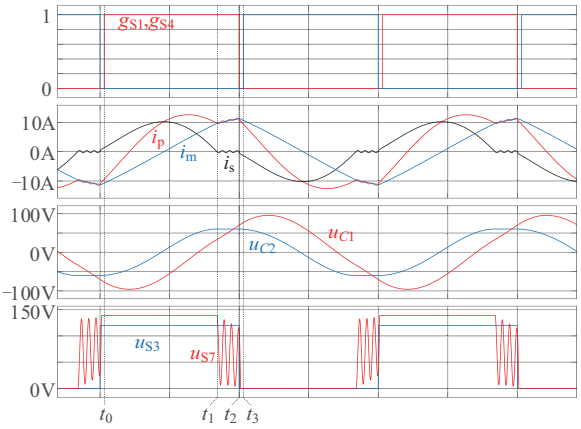

Fig. 2. Voltage and current waveforms of CLLC converter for under-resonant operation.

2) The value of the parasitic capacitance C_{oss} is much smaller than the value of resonant capacitance C_r;

3) If the transformer ratio is n:1 then $n^2C_{r1}=C_{r2}$, $L_{r1}=n^2L_{r2}$. In designing, $L_{r1}=n^2L_{r2}=L_r$, $C_{r1}=C_{r2}/n^2=C_r$.

A. Under-Resonant Modulation Time-Domain Modeling

The under-resonant operation waveforms of CLLC are shown in Fig. 2. Based on Table III, the possible current paths in under-resonant operation state are normal modality 1 to normal modality 2 and sneak modality 1 to sneak modality 7. To ensure the completeness of CLLC converter time-domain model, the time-domain modeling is required for normal modalities 1 and 2. Sneak modalities 4 and 5 end instantaneously, so they can be ignored when performing the time-domain analysis. Sneak modality 2 is triggered by sneak modalities 1 and 3, thus the time-domain modeling of sneak modalities 1 and 3 are required. Sneak modality 7 is triggered by sneak modality 6, so a time domain model of sneak modality 6 is needed. Therefore, the time-domain analysis is divided into three parts for discussion, as described in the following.

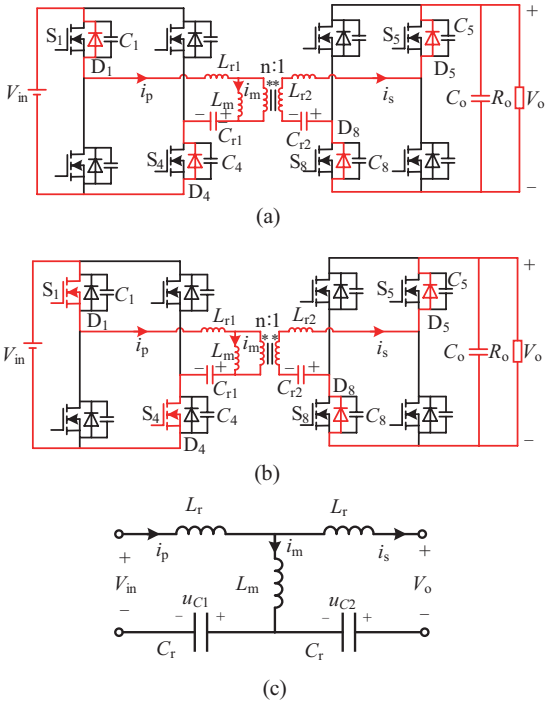

Fig. 3. (a) Current path diagram of normal modality 1. (b) Current path diagram of normal modality 2. (c) The corresponding equivalent circuit.

1) Normal Modality 1 and Normal Modality 2

The circuit diagrams of normal modalities 1 and 2, and their equivalent circuits are shown in Fig. 3. Based on the equivalent circuit, the voltage and current relationship expressions can be derived in (3).

$$\begin{cases} V_{in}=L_r\dfrac{di_p(t)}{dt}+u_{C1}(t)+L_m\dfrac{di_m(t)}{dt},L_m\dfrac{di_m(t)}{dt}=L_r\dfrac{di_s(t)}{dt}+u_{C2}(t)+V_o \\ i_p(t)=i_s(t)+i_m(t),i_p(t)=C_r\dfrac{du_{C1}(t)}{dt},i_s(t)=C_r\dfrac{du_{C2}(t)}{dt} \end{cases} \tag{3}$$

Solving (3) by using the differential operator method yields (4)–(7).

$$u_{C1}(t)=A_1\cos(\omega_{A1}t)+A_2\sin(\omega_{A1}t)+A_3\cos(\omega_{A2}t)+A_4\sin(\omega_{A2}t)+V_{in} \tag{4}$$

$$u_{C2}(t)=A_1\cos(\omega_{A1}t)+A_2\sin(\omega_{A1}t)-A_3\cos(\omega_{A2}t)-A_4\sin(\omega_{A2}t)-V_o \tag{5}$$

TABLE IV
FACTOR EXPRESSIONS

A	*B*	*J*	*K*
$A_1=\frac{1}{2}[u_{C1}(t_0)+u_{C2}(t_0)-V_{in}+V_o]$	$B_1=\frac{C_{oss}L_m[u_{C1}(t_1)+u_{C2}(t_1)-V_{in}+V_o]}{C_r(L_m+L_r)}$	$J_1=\frac{1}{2}[u_{C1}(t_2)+u_{C2}(t_2)+V_{in}-V_o]$	$K_1=\frac{1}{2}[u_{C1}(t_1)+u_{C2}(t_1)+V_{in}+V_o]$
$A_2=[i_p(t_0)+i_s(t_0)]/(2C_r\omega_{A1})$	$B_2=C_{oss}i_p(t_1)/(C_r^2\omega_{B1})$	$J_2=i_p(t_2)/(2C_r\omega_{J1})$	$K_2=[i_p(t_1)+i_s(t_1)]/(2C_r\omega_{K1})$
$A_3=\frac{1}{2}[u_{C1}(t_0)-u_{C2}(t_0)-V_{in}-V_o]$	$B_3=u_{C1}(t_1)-V_{in}-\frac{C_{oss}L_m}{C_r(L_m+L_r)}[u_{C2}(t_1)+V_o]$	$J_3=\frac{1}{2}[u_{C1}(t_2)-u_{C2}(t_2)+V_{in}+V_o]$	$K_3=\frac{1}{2}[u_{C1}(t_1)-u_{C2}(t_1)+V_{in}-V_o]$
$A_4=[i_p(t_0)-i_s(t_0)]/(2C_r\omega_{A2})$	$B_4=i_p(t_1)/(C_r\omega_{B2})$	$J_4=i_p(t_2)/(2C_r\omega_{J2})$	$K_3=[i_p(t_1)-i_s(t_1)]/(2C_r\omega_{K2})$
$\omega_{A1}=1/\sqrt{L_rC_r}$	$\omega_{B1}=1/\sqrt{(L_r+2L_m)L_rC_{oss}/(L_r+L_m)}$	$\omega_{J1}=1/\sqrt{L_rC_r}$	$\omega_{K1}=1/\sqrt{L_rC_r}$
$\omega_{A2}=1/\sqrt{(L_r+2L_m)C_r}$	$\omega_{B2}=1/\sqrt{(L_r+L_m)(C_r+C_{oss})}$	$\omega_{J2}=1/\sqrt{(L_r+2L_m)C_r}$	$\omega_{K2}=1/\sqrt{(L_r+2L_m)C_r}$

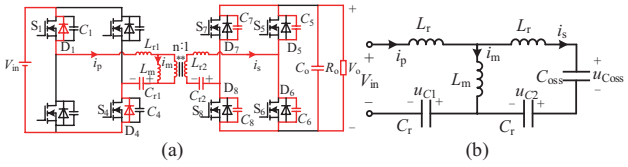

Fig. 4. (a) Current path diagram of sneak modality 1 and 3. (b) The corresponding equivalent circuit.

$$i_p(t)=-C_r\omega_{A1}A_1\sin(\omega_{A1}t)+C_r\omega_{A1}A_2\cos(\omega_{A1}t)-C_r\omega_{A2}A_3\sin(\omega_{A2}t)+C_r\omega_{A2}A_4\cos(\omega_{A2}t) \quad (6)$$

$$i_s(t)=-C_r\omega_{A1}A_1\sin(\omega_{A1}t)+C_r\omega_{A1}A_2\cos(\omega_{A1}t)+C_r\omega_{A2}A_3\sin(\omega_{A2}t)-C_r\omega_{A2}A_4\cos(\omega_{A2}t) \quad (7)$$

where ω_{A1}, ω_{A2} and A_1–A_4 are listed in Table IV. A_1–A_4 can be derived from (8).

$$u_{C1}(t_0)=u_{C1}(t_0),\frac{du_{C1}(t_0)}{dt}=\frac{i_p(t_0)}{C_r},u_{C2}(t_0)=u_{C2}(t_0),\frac{du_{C2}(t_0)}{dt}=\frac{i_s(t_0)}{C_r} \quad (8)$$

where $i_s(t_0)=i_p(t_0)-i_m(t_0)$, due to current $i_p(t_0)$ is approximately equal to the current $i_m(t_0)$, which means $i_s(t_0)=0$.

2) Sneak Modality 1 and Sneak Modality 3

Although the current direction on secondary side of sneak modalities 1 and modality 3 is different, they both have the same current path diagram and equivalent circuits, as shown in Fig. 4.

According to the equivalent circuit in Fig. 4(b), the state equations can be derived in (9). The total capacitance value of C_r in series with C_{oss} is C_{oss}, due to C_{oss}<<C_r. Therefore, $u_{Coss}(t)+u_{C2}(t)=u_2(t)$.

$$\begin{cases}V_{in}=L_r\frac{di_p(t)}{dt}+u_{C1}(t)+L_m\frac{di_m(t)}{dt},L_m\frac{di_m(t)}{dt}=L_r\frac{di_s(t)}{dt}+u_2(t)\\ i_p(t)=i_s(t)+i_m(t),i_p(t)=C_r\frac{du_{C1}(t)}{dt},i_s(t)=C_{oss}\frac{du_2(t)}{dt}\end{cases} \quad (9)$$

Solving (9) by using the differential operator method yields (10)–(13).

$$u_{C1}(t)=B_1\cos(\omega_{B1}t)+B_2\sin(\omega_{B1}t)+B_3\cos(\omega_{B2}t)+B_4\sin(\omega_{B2}t)+V_{in} \quad (10)$$

$$u_2(t)=\frac{(L_r+L_m)}{L_m}\frac{C_r}{C_{oss}}[B_1\cos(\omega_{B1}t)+B_2\sin(\omega_{B1}t)]-\frac{L_r+L_m}{L_m}[B_3\cos(\omega_{B2}t)+B_4\sin(\omega_{B2}t)] \quad (11)$$

$$i_s(t)=\frac{L_r+L_m}{L_m}C_r\omega_{B1}[-B_1\sin(\omega_{B1}t)+B_2\cos(\omega_{B1}t)]-\frac{L_r+L_m}{L_m}C_{oss}\omega_{B2}[-B_3\sin(\omega_{B2}t)+B_4\cos(\omega_{B2}t)] \quad (12)$$

$$i_p(t)=C_r\omega_{B1}[-B_1\sin(\omega_{B1}t)+B_2\cos(\omega_{B1}t)]+C_r\omega_{B2}[-B_3\sin(\omega_{B2}t)+B_4\cos(\omega_{B2}t)] \quad (13)$$

where ω_{B1}, ω_{B2} and B_1–B_4 are listed in Table IV. B_1–B_4 can be calculated by (14).

$$u_{C1}(t_1)=u_{C1}(t_1),\frac{du_{C1}(t_1)}{dt}=\frac{i_p(t_1)}{C_r},u_2(t_1)=u_{C2}(t_1)+V_o,\frac{du_2(t_1)}{dt}=\frac{i_s(t_1)}{C_{oss}} \quad (14)$$

where $i_s(t_1)=i_p(t_1)$–$i_m(t_1)$, due to current $i_p(t_1)$ is approximately equal to the current $i_m(t_1)$, which means $i_s(t_1)=0$. Sneak modality 2 is a situation that should be avoided, so there is no need to model it in the time domain.

3) Sneak Modality 6

The current path circuit diagram and equivalent circuit of Sneak modality 6 are shown in Fig. 5. Based on Fig. 5(b), the voltage and current relationship expressions can be derived in the followings.

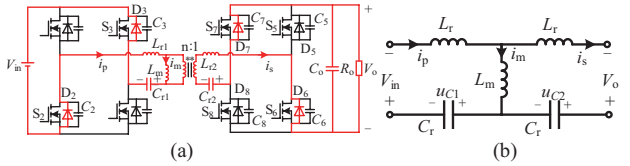

Fig. 5. (a) Current path diagram of sneak modality 6. (b) The equivalent circuit of sneak modality 6.

$$\begin{cases} -V_{in} = L_r \dfrac{di_p(t)}{dt} + u_{C1}(t) + L_m \dfrac{di_m(t)}{dt}, L_m \dfrac{di_m(t)}{dt} = L_r \dfrac{di_s(t)}{dt} + u_{C2}(t) - V_o \\ i_p(t) = i_s(t) + i_m(t), i_p(t) = C_r \dfrac{du_{C1}(t)}{dt}, i_s(t) = C_r \dfrac{du_{C2}(t)}{dt} \end{cases} \tag{15}$$

$$u_{C1}(t) = J_1 \cos(\omega_{J1} t) + J_2 \sin(\omega_{J1} t) + J_3 \cos(\omega_{J2} t) + J_4 \sin(\omega_{J2} t) - V_{in} \tag{16}$$

$$u_{C2}(t) = J_1 \cos(\omega_{J1} t) + J_2 \sin(\omega_{J1} t) - J_3 \cos(\omega_{J2} t) - J_4 \sin(\omega_{J2} t) + V_o \tag{17}$$

$$i_p(t) = -J_1 \omega_{J1} C_r \sin(\omega_{J1} t) + J_2 \omega_{J1} C_r \cos(\omega_{J1} t) - J_3 \omega_{J2} C_r \sin(\omega_{J2} t) + J_4 \omega_{J2} C_r \cos(\omega_{J2} t) \tag{18}$$

where ω_{J1}, ω_{J2} and J_1–J_4 are listed in Table IV. J_1–J_4 can be derived by solving (19).

$$u_{C1}(t_2) = u_{C1}(t_2), \frac{du_{C1}(t_2)}{dt} = \frac{i_p(t_2)}{C_r}, u_{C2}(t_2) = u_{C2}(t_2), \frac{du_{C2}(t_2)}{dt} = \frac{i_s(t_2)}{C_r} \tag{19}$$

Due to the current $i_p(t_2)$ is approximately equal to the current $i_m(t_2)$, which indicates $i_s(t_2) = i_p(t_2) - i_m(t_2) = 0$.

B. Over-Resonant Modulation Time-Domain Modeling

According to Table III, the possible current paths in over-resonant operating state are normal modality 1 to normal modality 2 and sneak modality 5 to sneak modality 9. The circuits of normal modalities 1 and 2 in over-resonant state are the same as the circuits in under-resonant state. Sneak modalities 5 and 8 end instantaneously, and they can be ignored when performing the time-domain analysis. Sneak modality 7 is triggered jointly by sneak modalities 6 and 9, and thus sneak modalities 6 and 9 need to be modeled in the time domain. The equivalent circuit of sneak modality 6 at over-resonance is the same as that of the under-resonant state, except that the initial value of time entry is different for the calculation and solution. The time-domain analysis of sneak modality 9 at over-resonance is described in the following. The voltage and current waveforms during the over-resonant operating condition are shown in Fig. 6. The current path diagram and equivalent circuit of sneak modality 9 are shown in Fig. 7.

Based on Fig. 7(b), the voltage and current relationship expressions are obtained in the following.

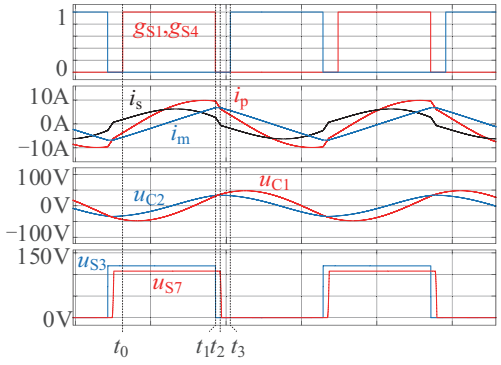

Fig. 6. Voltage and current waveforms of CLLC converter for over -resonant operation state.

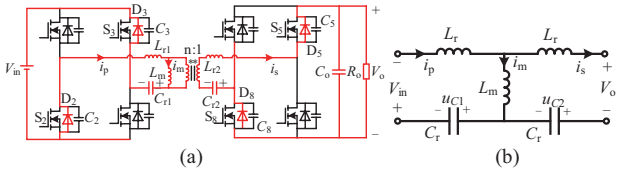

Fig. 7. (a) Current path diagram of Sneak modality 9. (b) The equivalent circuit of sneak modality 9.

$$\begin{cases} -V_{in} = L_r \dfrac{di_p(t)}{dt} + u_{C1}(t) + L_m \dfrac{di_m(t)}{dt}, L_m \dfrac{di_m(t)}{dt} = L_r \dfrac{di_s(t)}{dt} + u_{C2}(t) + V_o \\ i_p(t) = i_s(t) + i_m(t), i_p(t) = C_r \dfrac{du_{C1}(t)}{dt}, i_s(t) = C_r \dfrac{du_{C2}(t)}{dt} \end{cases} \tag{20}$$

$$u_{C1}(t) = K_1 \cos(\omega_{K1} t) + K_2 \sin(\omega_{K1} t) + K_3 \cos(\omega_{K2} t) + K_4 \sin(\omega_{K2} t) - V_{in} \tag{21}$$

$$u_{C2}(t) = K_1 \cos(\omega_{K1} t) + K_2 \sin(\omega_{K1} t) + K_3 \cos(\omega_{K2} t) - K_4 \sin(\omega_{K2} t) - V_o \tag{22}$$

$$i_p(t) = -K_1 \omega_{K1} C_r \sin(\omega_{K1} t) + K_2 \omega_{K1} C_r \cos(\omega_{K1} t) - K_3 \omega_{K2} C_r \sin(\omega_{K2} t) + K_4 \omega_{K2} C_r \cos(\omega_{K2} t) \tag{23}$$

where ω_{K1}, ω_{K2} and substituting the initial values yields K_1–K_4, are au listed in Table IV.

IV. Sneak Circuit Phenomenon and Trigger Mechanisms and Suppression

According to the combination and trigger form of these sneak operation modes, there are four sneak circuit phenomena in CLLC resonant converter, which are listed in Table V.

A. Sneak Circuit Phenomenon 1

During under-resonant operation, the normal modality between t_1–t_2 is the alternating operation of sneak modalities 1 and 3. And the appearance of sneak modality 2 will be triggered when the parasitic capacitance voltage u_{S7} of switch S_7 is equal to zero. At this time, the current flows through parasitic diode during the non-power transfer duration,

TABLE V
SNEAK CIRCUIT PHENOMENON

Phenomena	Mode
Sneak circuit phenomena 1	Normal modality 1→Normal modality 2→ Sneak modality 1→Sneak modality 2→ Sneak modality 3→Sneak modality 1→ Sneak modality 2→Sneak modality 3……
Sneak circuit phenomena 2	Normal modality 1→Normal modality 2→ Sneak modality 1→Sneak modality 3→ Sneak modality 4→Sneak modality 5→ Sneak modality 6→Sneak modality 7
Sneak circuit phenomena 3	Normal modality 1→Normal modality 2→ Sneak modality 1→Sneak modality 2→Sneak modality 3→Sneak modality 4→Sneak modality 5→ Sneak modality 6→Sneak modality 7
Sneak circuit phenomena 4	Normal modality 1→Normal modality 2→ Sneak modality 8→Sneak modality 9→Sneak modality 5→Sneak modality 6→Sneak modality 7

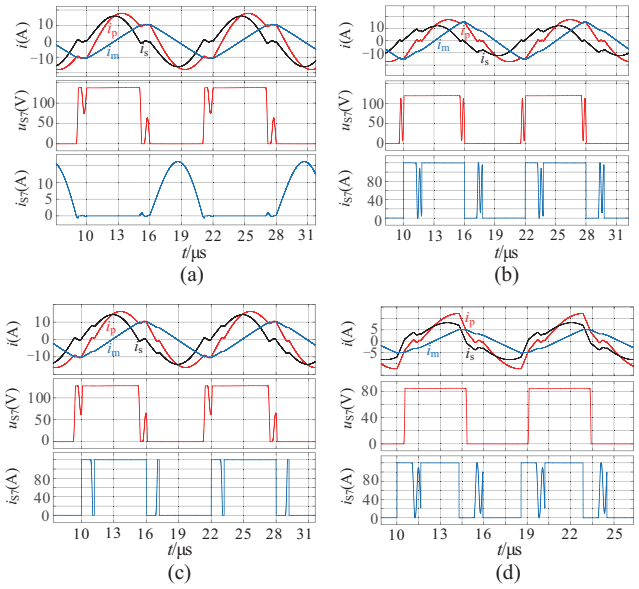

Fig. 8. Key waveforms of these four sneak circuit phenomena. (a) Sneak circuit phenomenon 1. (b) Sneak circuit phenomenon 2. (c) Sneak circuit phenomenon 3. (d) Sneak circuit phenomenon 4.

generates a non-essential power loss. Thus, the appearance of sneak modality 2 reduces the efficiency of CLLC converter. The key operation waveforms when sneak modality 2 is triggered are shown in Fig. 8(a).

Based on the time-domain model established in Section III-A and (12), since ω_{B1}>>ω_{B2}, $i_s(t)$ can be derived as (24), u_{S7} can be solved as shown in (25).

$$i_s(t)=\frac{L_r+L_m}{L_m}C_r\omega_{B1}\left[-B_1\sin(\omega_{B1}t)+B_2\cos(\omega_{B1}t)\right] \quad (24)$$

$$u_{S7}(t)=\frac{1}{C_{oss}}\int\frac{i_s}{2}\mathrm{d}t=\frac{1}{2}\frac{L_r+L_m}{L_m}\frac{C_r}{C_{oss}}[B_1\cos(\omega_{B1}t)+B_2\sin(\omega_{B1}t)]+E \quad (25)$$

$$2u_{S7}=\left[u_{C1}(t_1)+u_{C2}(t_1)-V_{in}+V_o\right]\cos(\omega_{B1}t)+2E \quad (26)$$

$$2E=V_o-u_{C2}(t_1)+V_{in}-u_{C1}(t_1) \quad (27)$$

$$u_{S7\min}=E-U_{S7} \quad (28)$$

$$C_r>\frac{P_o}{2V_o^2f_r} \quad (29)$$

Resonant capacitance needs to satisfy (29) when designing the CLLC converter in order to avoid the sneak circuit phenomenon 1. The influence of C_{oss} on u_{S7} is ignored in the derivation, but the value of C_{oss} is proportional to the oscillation amplitude of u_{S7}. Thus, the selection of switches with smaller parasitic capacitance helps to avoid the sneak modality 2.

B. Sneak Circuit Phenomenon 2

Due to sneak modality 7 is triggered, sneak circuit phenomenon 2 occurs during t_2–t_3 period in the under-resonant state. When i_p= 0, the primary side switch is fully closed, then sneak modality 7 is triggered, at this time the ZVS of primary side switch is disabled. The key waveforms in sneak circuit phenomenon 2 is shown in Fig. 8(b).

To achieve reliable ZVS on the primary side of CLLC converter, it is necessary to ensure that the switches change phase before i_p crosses zero. Therefore, the timing of i_p crosses zero needs to be analyzed. The maximum and minimum value of t_{dead} can be found according to (18) and (30). $u_{C1}(t_2)=u_{C1}(t_1)+I_m(T_s-T_r)/(2C_r)$, $u_{C2}(t_2)=u_{C2}(t_1)$, where T_s is the switch period and T_r is the resonant period.

$$i_p(t_2)=I_m,\ i_p(t_3)=0,\ t_{dead\_max}=t_3-t_2,\ t_{dead\_min}=8C_{oss}L_m.f_r \quad (30)$$

where I_m is the peak value of the excitation inductor current, f_r is the resonant frequency.

$$I_m=\frac{V_o}{4L_m.f_r} \quad (31)$$

C. Sneak Circuit Phenomenon 3

Due to sneak modality 2 is triggered simultaneously with sneak modality 7, then sneak circuit phenomenon 3 occurs. And it is the worst operation case of CLLC converter, resulting in large power loss. The trigger conditions of sneak modalities 2 and 7 have been analyzed in Section III and will not be repeated here. The key operation waveforms during this phenomenon are shown in Fig. 8(c).

D. Sneak Circuit Phenomenon 4

When CLLC converter operates in the over-resonant state, sneak circuit phenomenon 4 is triggered by sneak modality 7, where modality 7 is co-triggered by both sneak modalities 6 and 9 jointly. Currently, the ZVS of primary-side switches in

TABLE VI
PARAMETERS OF CLLC RESONANT CONVERTER

Parameters	Values	Parameters	Values
V_{in}	110−130 V	C_{r1}	300 nF
V_o	110−130 V	C_{r2}	300 nF
$L_{r1}+L_\sigma$	8.44 μH	Switches 1−8	IPW60R037CSFD
$L_{r2}+L_\sigma$	8.44 μH	f_r	100 kHz
P_o	1000 W	C_o	100 μF
L_m	29.54 μH	n	1:1

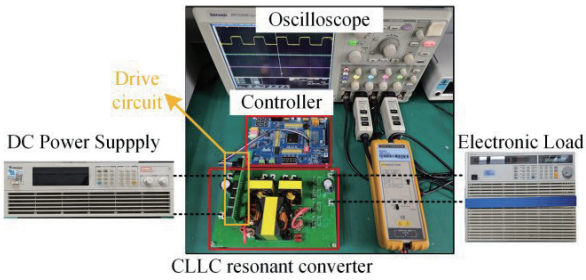

Fig. 9. CLLC resonant converter hardware platform.

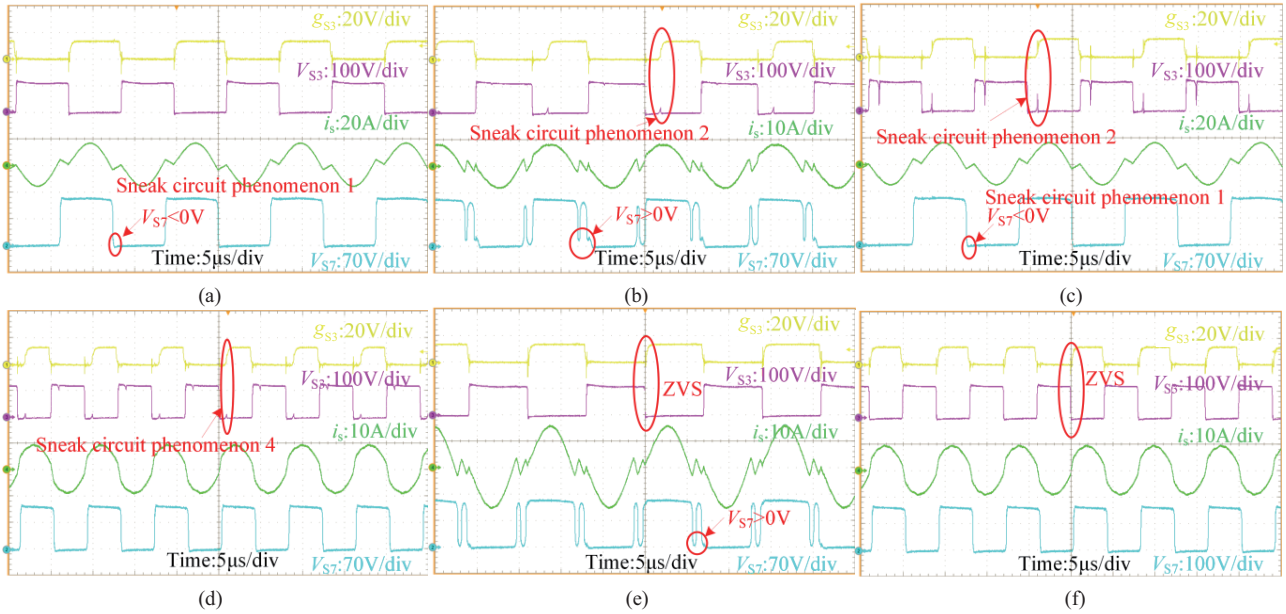

Fig. 10. Experimental waveforms of CLLC resonant converter under different conditions. (a) Sneak circuit phenomenon 1. (b) Sneak circuit phenomenon 2. (c) Sneak circuit phenomenon 3. (d) Sneak circuit phenomenon 4. (e) Under-resonant waveform. (f) Over-resonant operating waveform.

CLLC converter fails. To avoid the appearance of sneak circuit phenomenon 4, the dead time must be less than the operating time of sneak modalities 9 and 6. The key waveforms at this stage are presented in Fig. 8(d). Define the operation time of sneak modalities 9 and 6 as Δt_1 and Δt_2, respectively. Then, Δt_1 can be calculated according to (23).

$$i_p(t_1)=i_p(t_1),\quad i_p(t_2)=I_m,\quad \Delta t_1=t_2-t_1 \tag{32}$$

where $I_m=V_{in}/(4L_m f_s)$, f_s is the switching frequency.

Based on (18), Δt_2 can be calculated as

$$i_p(t_2)=I_m,\quad i_p(t_3)=0,\quad \Delta t_2=t_3-t_2 \tag{33}$$

From (32) and (33), the maximum value of dead time can be calculated by

$$t_{dead\_max}=\Delta t_1+\Delta t_2 \tag{34}$$

In order to ensure reliable ZVS on the primary side switches, the minimum value of t_{dead} is

$$t_{dead\_min}=8C_{oss}L_m f_s \tag{35}$$

V. EXPERIMENTAL VERIFICATION

In this section, a CLLC resonant converter prototype with the rated power of 1 kW is built for experimental verification. The detailed power circuit specifications are listed in Table VI, and the hardware platform is outlined in Fig. 9.

In order to verify the trigger conditions for the occurrence of sneak circuits, four types of sneak circuit phenomena are triggered under different conditions in the experiment, and the measured experimental waveforms are shown in Fig. 10 (a)–(d), the normal operation waveforms are shown in Fig. 10 (e)–(f).

By using the parameters in Table VI with a dead time set to 300 ns, and the load resistance is 14.4 Ω in the converter. As shown in Fig. 10(a), the sneak circuit phenomenon 1-modality 2 occurs. During the oscillation of current i_s around 0 A, the parasitic capacitance of switches S_5–S_8 is continuously charged and discharged. When the voltage across C_5–C_8 is reduced to 0 V, the parasitic diodes D_5–D_8 become conductive, resulting in unnecessary losses.

The converter adopts the parameters in Table VII, and the

TABLE VII
THE OPTIMIZED PARAMETERS OF CLLC RESONANT CONVERTER

Parameters	Values	Parameters	Values
V_{in}	110–130 V	C_{r1}	600 nF
V_o	110–130 V	C_{r2}	600 nF
$L_{r1}+L_\sigma$	5.3 μH	Switches 1–8	IPW60R037CSFD
$L_{r2}+L_\sigma$	5.3 μH	f_r	90 kHz
P_o	1000 W	C_o	100 μF
L_m	29.54 μH	n	1:1

load resistance is 28.8 Ω. By using the theoretical calculations in Section IV, sneak modality 7 appears when t_{dead} = 2.27 μs. And the deadtime is set to 2.1 μs in the experiment. As shown in Fig. 10(b), the CLLC converter operates in sneak circuit phenomena 2-modality 7. Due to the large dead time set for the primary side switches, the current i_p oscillates around 0 A, continuously charging and discharging S_1–S_4. If the switches turn on when the drain-source voltage is not 0 V, the switches transition from ZVS to hard switching, resulting in increased switching losses. Under sneak circuit phenomenon 2, although the current i_s oscillating around 0 A, continuously charging and discharging S_5–S_8, the voltage across C_5–C_8 does not reach 0 V. Consequently, the parasitic diodes D_5–D_8 do not conduct.

By adopting the parameters in Table VI, the deadtime is set to 1.44 μs and the load resistance is 14.4 Ω. Sneak circuit phenomenon 2 appears when t_{dead} = 0.8 μs. As shown in Fig. 10(c), CLLC converter operates in sneak circuit phenomena 3. It includes sneak modality 2 and modality 7. The primary-side switch ZVS fails and the secondary-side D_5–D_8 conduct in the non-power-transfer phase.

As shown in Fig. 10(d), By adopting the parameters in Table VI, CLLC converter operates in the over-resonance mode. By applying the theoretical calculations in Section IV and the load resistance is 18 Ω, sneak modality 7 appears when t_{dead} = 1.17 μs, and experimentally sneak modality 7 appears at t_{dead} = 1.14 μs. When the sneak circuit phenomenon 4 occurs, the sneak modality 7 appears and the primary side switch ZVS fails.

The above four phenomena of sneak circuits will lead to lower efficiency of the CLLC converter, so the parameters of the converter are optimized and designed according to the method in Section IV. The parameters shown in Table VII are satisfied (29). Fig. 10(e) shows the normal operating waveforms for the under-resonant operating state. The converter adopts the parameters in Table VII, and the deadtime is set to 300 ns. The S_5–S_8 are continuously charged and discharged during the oscillation of current i_s around 0 A. The voltage across C_5–C_8 does not drop to 0 V and D_5–D_8 are not conducted. Primary side switches S_1–S_4 operate in the ZVS state. Neither sneak phenomenon 1 nor sneak phenomenon 2 exists, i.e., sneak phenomenon 3 does not exist.

Fig. 10(f) shows the normal operating waveforms for the over-resonant operating state. The converter adopts the parameters in Table VI, and the deadtime is set to 300 ns. Primary side switches S_1–S_4 operate in the ZVS state. Sneak phenomenon 4 does not exist.

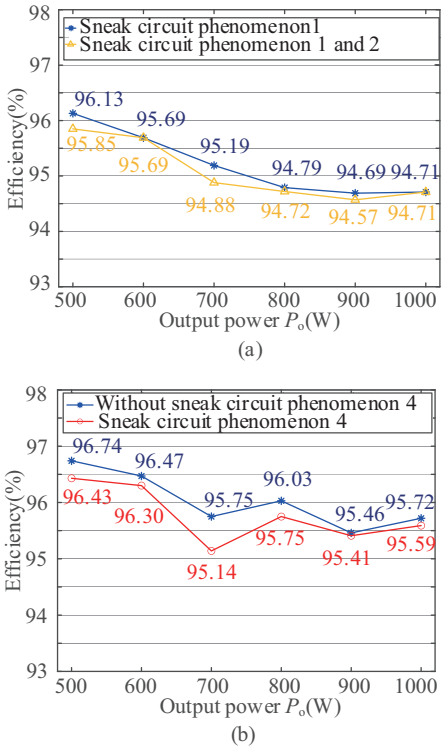

Fig. 11. Efficiency curve of CLLC resonant converter.

Fig. 11 shows the efficiency curve of the CLLC converter with Table VI parameters. The converter adopts the parameters in Table VI, and it operates in the under-resonant state, the dead time of the converter is set to t_{dead1} = 300 ns (blue line) and t_{dead2}>1.4 μs (yellow line), respectively. As shown in Fig. 11(a), the blue line is the efficiency curve when sneak circuit phenomenon 1 is present, and the yellow line is the efficiency curve when both sneak circuit phenomenons 1 and 2 are present, i.e., when sneak circuit phenomenon 3 is present. By setting the dead time appropriately, sneak circuit phenomenon 2 can be eliminated and efficiency can be improved.

As shown in Fig. 11(b), the converter adopts the parameters in Table VI, and it operates in the over-resonant state, t_{dead1} = 300 ns (blue line) and t_{dead2} = 1.14 μs (red line), respectively. When the dead time is set too large, it will trigger the sneak circuit phenomenon 4 resulting in the converter primary-side switches fail to realize ZVS, which also leads to the reduction of converter efficiency. By setting the dead time reasonably, the sneak circuit phenomenon 4 can be eliminated and the efficiency can be improved.

VI. CONCLUSION

The graph theory-based sneak circuit particularity analysis, trigger mechanism and suppression method for CLLC resonant converter are studied in this paper. A current-based sneak circuit classification method is proposed, and an accurate sneak circuit analysis is realized by combining the relationship between the primary-side and secondary-side currents. In addition, the CLLC time-domain model considering parasitic

parameters is investigated, nine sneak circuit modalities and four sneak circuit phenomena of CLLC converter are analyzed. The higher-order oscillations of voltage and current are also described in detail. During primary-side current and secondary-side current intermittency, there exists a current that charges and discharges inside the parasitic capacitor. The above sneak modality analysis helps to predict all possible sneak circuit phenomena.

Moreover, the trigger mechanism is introduced by time-domain analysis, and a general method to suppress the sneak circuit phenomenon is proposed to improve the reliability and efficiency of CLLC resonant converter operation by optimizing modulation parameters and the converter parameter design. The proposed suppression method avoids unnecessary power losses in the CLLC converter and effectively suppresses the oscillations of voltage and current waveforms.

Compared with previous research articles, the proposed method provides a more accurate model, a more detailed trigger mechanism and practical suppression method to improve the efficiency as well as the stability of CLLC converter. In addition, this method can be extended and applied to model and analyze other various resonant converters.

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