A Generalized Partial Fault-Tolerant Single-Phase Common-Ground Multilevel Inverter for PV System

Soniya AGRAWAL, Manoranjan SAHOO, Sateesh Kumar KUNCHAM, and Yam Prasad SIWAKOTI

***Abstract*—The common ground multilevel inverter (MLI) is highly appreciated in transformerless photovoltaic (PV) systems, which have improved leakage current performance and reduced filter size. The fault-tolerant (FT) capability is essential in a common ground inverter to enhance the reliability of the system. This paper highlights a FT strategy for single-phase common ground MLI under different open switch fault conditions. The proposed circuit can self-balance the voltage across the switched capacitor (SC) in normal and switch open circuit (OC) fault conditions. Moreover, the employed modulation scheme enables the SCs to be connected in series or parallel to obtain a wide range of output voltages with reduced input voltage. Further, the circuit can be extended for higher voltage levels by adding SC cells. A detailed Markov reliability and cost function assessment highlights the merits of the proposed inverter over counter topologies. Finally, the inverter's operational feasibility and effectiveness are validated through 500 W prototype experimentally.**

***Index Terms*—Common ground, fault-tolerant, multilevel inverter, reliability, switched capacitor.**

I. Introduction

THE global move toward clean and sustainable energy is evident by widespread adoption of photovoltaic (PV) systems in industries, homes, and power generation stations. Inverters play a crucial role in PV-based power conversion systems. Transformerless inverters (TLIs) are compact, low-cost solutions for grid-connected PV systems [1]. However, removing transformers from inverters introduces leakage current issues due to the PV panel's parasitic capacitance. The traditional transformerless three-level (3L) H-bridge inverter with boost converter has less component count, but it is able to supply a 3L output which in turn requires higher size of filter to obtain a sinusoidal waveform. Consequently, boost with seven-level (7L) H-bridge inverter was presented in the literature [2] to increase the output voltage levels. But it comes with an increased number of switches, DC sources, gate driver circuitry, and passive components. Further, the conventional H-bridge based inverters are suffering from the issue of leakage current due to PV parasitic capacitance. This results in electromagnetic compatibility (EMC) problems, low power quality, and shorter system lifespan. Thus, the above-said topologies cannot be used directly for the PV applications as per the German VDE 0126-1-1 standard (i.e., common mode leakage current should be less than 100 mA). Also, the use of front-end boost converters is more susceptible to instability especially at higher duty ratios, and involve complex inductor design.

To address the above said issues literature proposes that minimizing leakage current in TLIs by forming a common ground connection between the load-neutral and PV-negative terminals is the most effective solution [3]–[5]. As there is a chance of the failure of a switch in a solar-powered inverter due to sudden load changes, overheating, or manufacturing defects, it results in the shutdown of the entire system. However, the continuity of supply is essential for critical off-grid solar applications like lighting in remote areas, water pumping, power supply for security surveillance, and medical emergency systems. Therefore, a FT system is an important aspect in the above applications to retain the continuous supply of electric power. For instance, an off-grid solar-based water pumping system in remote areas is driven by an inverter [6]. If a switch fault occurs in the inverter, the water pumping will stop, disrupting essential day-to-day activities. With a FT inverter, the system would continue to supply water even in the event of a switch failure, ensuring uninterrupted operation. Therefore, recent research has emphasized the development of multilevel inverters (MLIs) with integrated FT capabilities. Based on the availability of voltage at the load during post-fault period, the inverter can be named as partial FT or complete FT topology. A complete FT hybrid cascaded H-bridge (CHB) MLI [7] is presented, utilizing cross-coupled CHB for fault tolerance. However, this topology has a higher switch count and demands a greater number of independent DC sources. To address this, [8] proposes a FT 7L CHB inverter with fewer switches. In several cases, complete FT operation is not practically possible due to the requirement of uneven voltage sources and the non-availability of redundant paths.

To address that, in [9], a 7L inverter was adapted for partial fault tolerance with a greater number of DC sources. The

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inverter in [10], [11] employs three DC sources and a high switch count. Also, using an H-bridge at the output stage for polarity generation results in high total standing voltage (TSV). In [12], a resilient FT five-level (5L) inverter is discussed. While the topology has fewer switching devices, the use of clamping diodes increases conduction losses in the system. The topology in [13] offers fault tolerance with fewer switches for 5L output voltage under most faults but is limited to buck mode operation. In [14], [15], FT 5L inverters for single and multiple-switch faults are described. Madhukar Rao A.,et al. introduce a partial FT inverter using a tap-changing transformer to preserve power rating, raising system costs [16].

Moreover, the explored FT inverter topologies face challenges in direct application to PV systems due to parasitic capacitance-induced leakage current. Thus, they cannot be used directly for the PV applications. To address this, additional common-mode filters or transformers are needed, increasing system size, cost, complexity, and power losses. CG-based inverters can mitigate leakage current, but achieving both FT and multilevel operation is challenging due to the limited number of redundant states. A FT operation in MLI with a CG is an important aspect of a PV system, however, it has not been adequately explored in the literature. Therefore, the authors are driven to explore the development of a novel CG based FT MLI with inherent voltage boosting for standalone PV applications. Further, the key attributes of the suggested inverter are as follows:

- Manages single or multiple switch faults with the least or no modification in pulse width modulation (PWM) scheme.
- Eliminating the leakage current with a single source and handling faults while giving generalized multilevel output voltages.
- Three-time inherent voltage boosting.
- Self-balanced voltage across switched capacitors (SCs) (C_1 and C_2) pre- and post-fault operation.
- Markov reliability, component comparison, and cost function (CF) analysis indicate the proposed topology's suitability for standalone PV systems.

The rest of the paper is organized as follows: Section II covers the topology description and operation of the proposed inverter, modulation and fault tolerance scheme. Section III analyzes inverter's reliability. Section IV deals with simulation and hardware validation. Section V details the voltage current and loss analysis of the proposed inverter. Section VI gives the maximum power point tracking (MPPT) approach for the proposed inverter. Section VII compares the presented topology with its counterparts. Finally, Section VIII concludes the paper.

II. Proposed Generalized Common Ground Fault-Tolerant MLI

A. Topology Description and Mode of Operation

The schematic of the generalized structure for the proposed common ground FT multilevel inverter (CGFTMLI) is illustrated in Fig. 1. The blue-coloured line shows the redundant

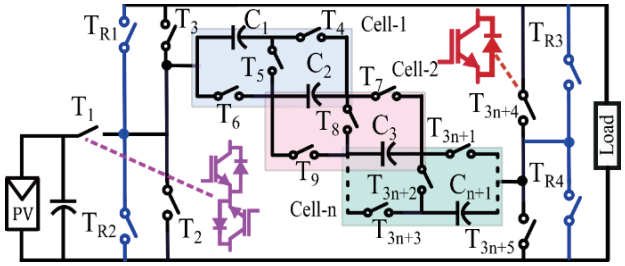

Fig. 1. Schematic of the generalized structure of the proposed CGFTMLI.

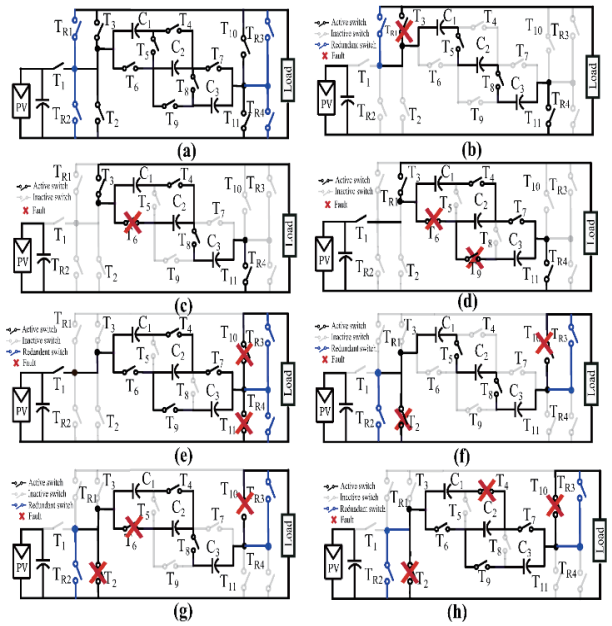

Fig. 2. FT operation of proposed CGFTMLI.

switches added for fault tolerance. The black-coloured line shows the inverter during normal operation. The n number of basic SC cells can be cascaded (as shown in multi-colour cells) to generate the $2n$+3 output voltage levels, which requires an n+1 number of switched capacitors and a $3n$+5 number of switches. Each basic cell can generate a 5L output voltage, and it can be generalized to $2n$+3 output voltage levels.

The 7L inverter is considered for the FT operation analysis with n = 2, SC cells, as shown in Fig. 2(a). It consists of 11 controlled switches (T_1– T_{11}), one input DC link capacitor (C_{in}), and three SCs (C_1, C_2, C_3). The series and parallel configuration of the SC generates 7L voltage with three times input voltage boosting. The main inverter switching table for various switches in different modes of operation (V_1–V_7) during normal operation is given in Table I. It outlines the inverter's various switch conditions during operational modes. In mode M_1, V_{AN} is $+3V_{dc}$ with C_1, C_2, and C_3 discharging in series. In mode M_2, V_{AN} drops to $+2V_{dc}$; C_2 discharges in series and C_3 in parallel. Mode M_3 realizes V_{AN} at $+V_{dc}$, with all capacitors charging in parallel, acting as an additional DC link. In mode M_4, V_{AN} is $0V_{dc}$, allowing load current to freewheel through T_{10} and T_{11}, with capacitors charging in parallel. Mode M_5 drops V_{AN} to $-V_{dc}$, discharging all capacitors in parallel. In mode M_6,

TABLE I
SWITCHING STATES OF THE VARIOUS SWITCHES DURING NORMAL INVERTER OPERATION

S.No	Mode	Voltage level	On state switches	C_1, C_2, C_3
1.	M_1	$3V_{dc}$	T_3, T_5, T_8, T_{11}	↓
2.	M_2	$2V_{dc}$	T_3, T_4, T_6, T_8, T_{11}	↓
3.	M_3	V_{dc}	T_1, T_3, T_4, T_6, T_7, T_9, T_{11}	↑
4.	M_4	$0V_{dc}$	T_1, T_4, T_6, T_7, T_9, T_{10}, T_{11}	↑
5.	M_5	$-V_{dc}$	T_2, T_4, T_6, T_7, T_9, T_{10}	↓
6.	M_6	$-2V_{dc}$	T_2, T_4, T_6, T_9, T_{10}	↓
7.	M_7	$-3V_{dc}$	T_2, T_5, T_8, T_{10}	↓

↓ = Discharging, ↑ = Charging

V_{AN} is $-2V_{dc}$, with C_1 and C_2 discharging in parallel and C_3 in series. Finally, mode M_7 achieves $-3V_{dc}$, with all capacitors discharging in series [17].

The switch faults significantly impact the operation of the main inverter, leading to the unavailability of most voltage levels in the event of any switch fault. Four redundant switches (T_{R1}–T_{R4}) have been added to the circuit to tolerate the various switch faults. The FT analysis and corresponding modulation scheme are explained in the following subsections.

B. Fault Tolerant Analysis

The effect of open circuit (OC) switch faults of the proposed inverter has been analyzed in detail for the single switch fault, double and triple switch fault scenarios, and availability of various voltage levels during open fault conditions have been listed in Table II. Additionally, the fast-acting relays associated with each switch will activate in response to a short-circuit fault, converting it into an open-circuit fault [18], [19]. It has to be noted that there are 11 cases possible for single switch fault, C(11,2)=11!/(9!*2!)=55, combination for double switch fault and C(11,3)=11!/(8!*3!)=165 combination for triple switch fault is possible. In Table II, all single-switch fault cases and potential double- and triple-switch fault cases have also been listed, and some of the possible faults and reductant states are illustrated in Fig. 2.

1) Single switch fault: In case of a fault on the switch T3 during the mode M_1, the $3V_{dc}$ voltage level can be generated by activating redundant switch T_{R1} as shown in Fig. 2(b). If the switch fault occurs in switch T_6 in mode M_2, $2V_{dc}$ voltage level can be obtained without any modification in PWM scheme as given in Fig. 2(c).
2) Double switch fault: When fault occurs in switch T_6 and T_9 simultaneously in mode M_3, in this case the capacitor C_1 continues to provide V_{dc} voltage level at the output as in Fig. 2(d). Also, during mode M_4, if fault occur on T_{10} and T_{11} as in Fig. 2(e), the redundant switches T_{R3} and T_{R4} can be switched "ON". Mode M_5, T_2, T_5 fault can be replaced by redundant switches T_{R2} and T_{R3} in Fig. 2(f).
3) Triple switch fault: In the event of simultaneous three switches i.e,. T_2, T_5 and T_{10} failure in mode M_6 as Fig. 2(g) and similarly in case of T_2 and redundant switches to get T_2, T_4 and T_{11} failure in mode M_7 as Fig. 2(h), with redundant switches and alternate path for the $-2V_{dc}$ and $-3V_{dc}$ voltage levels can be obtained. Table II outlines the accessibility of switching states and voltage levels within the proposed topology under various other fault conditions, incorporating redundant switches. Therefore, the suggested CGFTMLI can tolerate failure of single and multiple switches while providing a continuous supply to the load.

C. Fault Tolerant Modulation Scheme

The modulation scheme for the proposed FT inverter is determined by the number of output voltage levels obtained during post-fault. The level-shifted pulse width modulation (LS-PWM) scheme has been adopted for 7L voltage generation. The availability of voltage levels during OC fault and fault tolerant strategy has been shown in Table II. It shows that a 7L output voltage can be obtained if any single, double, or triple fault occurs on switches T_2, T_3, T_{10}, and T_{11} during post-fault operation. In this case, the reference voltage V_{ref} has been taken with an amplitude $A_c = A_{ref}/3$, as shown in Fig. 3(a). Similarly, for faults on the switches T_4, T_5, T_6, T_7 or T_8 5L output voltage is obtained with V_{ref} amplitude $A_c = A_{ref}/2$ as given in Fig. 3(b). In case of a fault on any two series switches (for example, switch T_4 and T_6 simultaneously) a 3L output voltage can be achieved with V_{ref}, having, $A_c = A_{ref}$ shown in Fig. 3(c). The flowchart in Fig. 4 illustrates the procedural steps for implementing the LS–PWM scheme in normal and fault conditions.

D. Self-Voltage Balancing Analysis of the SCs

Table I reveals that all three SCs are charged with the same voltage for an equal amount of time and are discharged simultaneously. Therefore, the proposed inverter has achieved self-voltage balancing of the SC [20]. The voltage across each capacitor is naturally balanced to V_{dc} by the principle of charge-second balance of the capacitor in a fundamental cycle of the output voltage. As per Table I, the capacitors are charged during modes M_3 and M_4, and the capacitors are discharged in all the other modes of operation. Also, in the mode M_4, the load current freewheels. Considering half-wave symmetry to the output voltage (V_{ac}) and current (i_{ac}) with the load across the inverter as Z_L, the average current through capacitors during each mode of operation is given by

$$\begin{aligned} &\langle i_c^{M1} \rangle = 3v_c/Z_L,\ \langle i_c^{M2} \rangle = 2v_c/Z_L,\ \langle i_c^{M3} \rangle = V_{dc}/Z_L,\ \langle i_c^{M4} \rangle = 0, \\ &\langle i_c^{M5} \rangle = 3v_c/Z_L,\ \langle i_c^{M6} \rangle = 2v_c/Z_L,\ \langle i_c^{M7} \rangle = v_c/Z_L \end{aligned} \quad (1)$$

Where v_c is the voltage across each capacitor. Using the above relations, the net charge (Q) delivered/absorbed by capacitors over the fundamental cycle (with time period T) is given by

$$Q = \left\{ \langle i_c^{M1} \rangle + \langle i_c^{M2} \rangle + \langle i_c^{M3} \rangle + \langle i_c^{M4} \rangle - \langle i_c^{M5} \rangle - \langle i_c^{M6} \rangle - \langle i_c^{M7} \rangle \right\} T \quad (2)$$

TABLE II
AVAILABILITY OF VOLTAGE LEVELS DURING OC FAULT WITH FAULT TOLERANT STRATEGY

S.NO.	Faulty switch	Availability of the various voltage levels							Connection of Capacirors		
		M_1	M_2	M_3	M_4	M_5	M_6	M_7	C_1	C_2	C_3
1.	$T_2/T_3/T_{10}/T_{11}/T_2T_3/T_{10}T_{11}/T_2T_3T_{11}/T_2T_3\ T_{11}$	T_{R1}, T_6, T_8, T_{R4}	T_{R1}, T_4, T_7, T_9, T_{R4}	T_1, T_{R1}, T_4, T_5, T_7, T_9, T_{R4}	T_1, T_6, T_8, T_9, T_{R3}, T_{R4}	T_{R2}, T_4, T_5, T_7, T_9, T_{R3}	T_{R2}, T_4, T_7, T_8, T_{R4}	T_{R2}, T_6, T_8, T_R	√	√	√
2.	$T_4/T_4T_2/T_4T_3/\ T_4T_{10}/T_4\ T_{11}$	--	T_{R1}, T_7, T_9, T_{R4}	T_{R1}, T_6, T_8, T_{R4}	T_1, T_6, T_8, T_{10}, T_{R4}	T_{R2}, T_6, T_8, T_9, T_{R3}	T_{R2}, T_7, T_9, T_{R3}	--	--	√	√
3.	$T_5/T_5T_2/T_5T_3/\ T_5T_{10}/T_5T_{11}$	--	T_{R1}, T_7, T_9, T_{R4}	T_{R1}, T_6, T_8, T_{R4}	T_1, T_6, T_8, T_{10}, T_{R4}	T_{R2}, T_6, T_8, T_9, T_{R3}	T_{R2}, T_7, T_9, T_{R3}	--	√	√	√
4.	$T_6/T_6T/T_6T_3/T_6T_{10}/T_6/T_{11}$	--	T_{R1}, T_8, T_5, T_{R4}	T_{R1}, T_4, T_8, T_9T_{R4}	T_1, T_4, T_8, T_9, T_{R3}, T_{R4}	T_{R2}, T_4, T_7, T_9, T_{R3}	T_{R2}, T_8, T_5, T_{R3}	--	√	--	√
5.	$T_7/T_7T_2/\ T_7T_3/\ T_7T_{10}/T_7T_{11}/\ T_7T_3\ T_{11}$	--	T_{R1}, T_8, T_5, T_{R4}	T_{R1}, T_4, T_8, $T_9\ T_{R4}$	T_1, T_4, T_8, T_9, T_{R3}, T_{R4}	T_{R2}, T_4, T_8, T_9, T_{R3}	T_{R2}, T_8, T_5, T_{R3}	--	√	--	√
6.	$T_8/T_8T_2/T_8T_3/\ T_8T_{10}/T_8T_{11}$	--	T_{R1}, T_4, T_6, T_9, T_{R4}	T_{R1}, T_4, T_5, T_{R4}	T_1, T_{R1}, T_6, T_5, T_{R3}, T_{R4}	T_{R2}, T_5, T_6, T_{R3}	T_{R2}, T_4, T_6, T_9, T_{R3}	--	√	√	√
7.	$T_9/T_9T_3/\ T_9T_2T_3/\ T_{10}\ T_9T_3$	--	T_{R1}, T_8, T_5, T_{R4}	T_{R1}, T_4, T_7, T_{R4}	T_1, T_{R1}, T_6, T_5, T_{R3}, T_{R4}	T_{R2}, T_4, T_7, T_{R3}	T_{R2}, T_8, T_5, T_{R3}	--	--	√	√
8.	$T_6T_4/\ T_2T_6T_4/\ T_3T_6T_4/T_{10}T_6T_4$	--	--	T_{R1}, T_8, T_9, T_{R4}	T_1, T_8, T_9, T_{R3}, T_{R4}	T_{R2}, T_6, T_8, T_9, T_{R3}	--	--	--	--	√
Charging state of capacitor's		↓	↓	↑	↑	↑	↓	↓			

√ = Available, -- = Not available

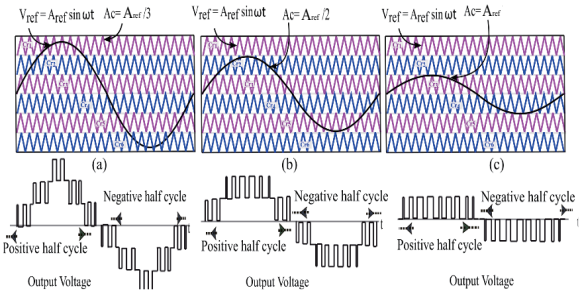

Fig. 3. PWM scheme for the converter (a) 7L, (b) 5L and (c) 3L post-fault voltages.

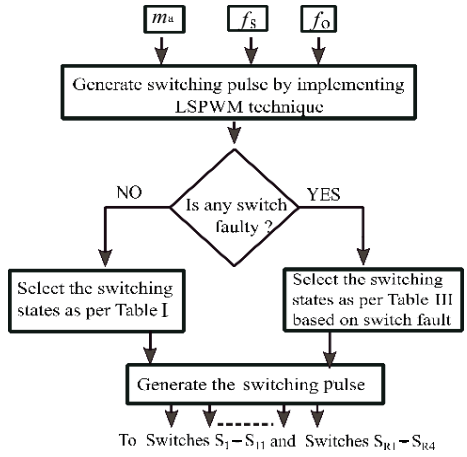

Fig. 4. Flowchart for selection of gate pulses.

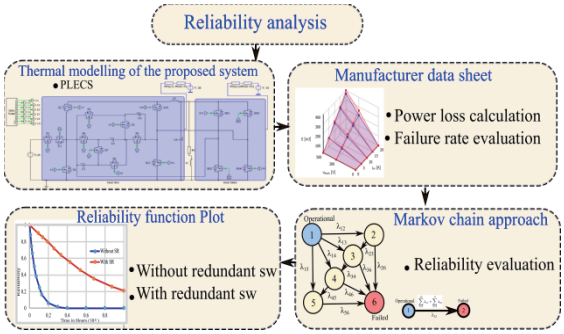

Fig. 5. Process of assessing reliability for the proposed inverter.

The average charge (Q) passing through an ideal capacitor must be zero for a periodic voltage in steady-state conditions. By substituting (1) with $Q = 0$, (2) simplifies to

$$0 = (V_{dc} - v_c)/Z_L \tag{3}$$

This results in $v_c = V_{dc}$, which implies that the capacitor exhibits self-voltage balancing ability without requiring any voltage/current sensors.

III. RELIABILITY ANALYSIS

Predicting reliability in power electronic converters is essential for manufacturers and users. If the converter unexpectedly fails, it can cause significant economic losses. Reliability assessment identifies potential failure modes,

enabling careful maintenance and reducing the risk of sudden breakdowns. The process of reliability assessment for the proposed inverter is summarized in Fig. 5. The power semiconductor devices are the most fragile components of power electronic systems. The main factors causing the aging failure of power devices are thermal stresses which are caused by the means temperature [21]. Initially, thermal modeling of the inverter on the piecewise linear electrical simulation (PLECS) platform evaluates power loss by referencing the manufacturer's data sheet for various components. The failure rates of switches and capacitors are determined using obtained power loss data [22]. Subsequently, the Markov chain reliability assessment derives the reliability function

$$R(t) = e^{-\lambda t} \tag{4}$$

Where, λ is the component's failure rate in failures /10^6 h, which has been calculated as follows:

The failure rate of the components (λ_z) is defined as

$$\lambda_z = \lambda_{\text{zbase}} \prod_{x=1}^{n} \alpha_x \tag{5}$$

Where, λ_{base} is the base failure rate of the component, n is the number of factor (α) affecting the failure rate of the components.

The various factors affecting the failure rate of the components are temperature factor (αT), quality factor (αQ), application factor (αA), capacitance factor (α_{cv}), stress factor (αS), and environment factor (αE). Therefore, the failure rate for switch (S_i) and capacitor (C_i) can be calculated as below:

(a) Failure rate for switch (S_i): As per (5), the failure rate of the switch (S_i) can be calculated as

$$\lambda_{\text{si}} = \lambda_{\text{si,base}} \times \alpha T_{\text{si}} = \times \alpha Q \times \alpha A \times \alpha E \tag{6}$$

For the reliability calculation, the idea switches have been considered, hence $\alpha A = \alpha Q = 1$, and for same environmental condition for all the devices, it gives that $\alpha E = 1$. The base failure rate of the switch ($\lambda_{\text{si,base}}$) is taken as 0. 00074.The αT for the switch and diode is given as

$$\alpha T_{\text{si}} = exp\left[-1925 \times \left(\frac{1}{T_j + 273} - \frac{1}{298}\right)\right] \tag{7}$$

Where T_j is the junction temperature of the switch, which can be calculated as

$$T_j = T_c + \theta_{jc} \tag{8}$$

$$T_c = T_a + \theta_{ca} \times P_{\text{loss}} \tag{9}$$

Where T_c and T_a are the heat sink and ambient temperature, respectively. θ_{jc} and θ_{ca} are junction to case and case to ambient thermal impedances. The values of T_a, θ_{jc} and θ_{ca} are assumed as 25 °C, 0.45 °C/W and 62 °C/W, respectively. P_{loss} is the total power loss of the switch obtained from the PLECS real time simulator.

(b) Failure rate for capacitor (C_i):

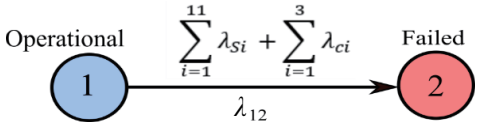

Fig. 6. Markov chain state transition diagram of inverter without redundant switches.

$$\lambda_{\text{ci}} = \lambda_{\text{ci,base}} \times \alpha_{\text{cv}} \times \alpha Q \times \alpha S \times \alpha \text{E} \tag{10}$$

The α_{cv} and αS for the capacitor is given as

$$\alpha_{\text{cv}} = 0.34 \times C^{0.12}, \ \alpha_{\text{S}} = V_{\text{S}}^{2.43} \tag{11}$$

Where V_S is equal to the ratio of operating voltage to rated voltage and C is the capacitance in microfarad.

From the component's failure rate, the overall system's reliability can be evaluated using the Markov chain model. The reliability of the proposed 7L common ground FT inverter has been analyzed using the Markov chain model in two conditions of the inverter, without redundant switches and with redundant switches.

A. Reliability Without Redundant Switches

This section analyzes the failure rate of the inverter without redundant switches. In the event of a failure in any component, the whole system is completely shut down. It is assumed that each component will have two states to evaluate the reliability per the Markov chain process: operational state 1 and failure state 2. Fig. 6 shows the state transition diagram of the converter without redundant switches. It illustrates that the failure of any of the switches, i.e., T_1–T_{11} ($\sum_{i=1}^{11} \lambda_{\text{Si}}$) or any of the capacitors, i.e., C_1–C_3 ($\sum_{i=1}^{3} \lambda_{\text{ci}}$) can lead to overall system failure. The $P_1(t)$ and $P_2(t)$ are occupations of probability in state 1 (operational) and state 2 (failed), respectively. Based on the state transition diagram of the inverter without redundant switches, the state equation can be written as [20]

$$\begin{bmatrix} \dot{P_1}(t) & \dot{P_2}(t) \end{bmatrix} = \begin{bmatrix} P_1(t) & P_2(t) \end{bmatrix} \begin{bmatrix} -\lambda_{12} & \lambda_{12} \\ 0 & 0 \end{bmatrix} \tag{12}$$

Inverter is assumed to be functioning at $t = 0$, hence ,

$$P_1(0) = 1, P_2(0) = 0 \tag{13}$$

After solving the differential (12)

$$P_1(t) = e^{-\lambda_{12} t} \tag{14}$$

Where λ_{12} is the rate when state 1 the inverter makes the transition to state 2, which is defined as

$$\lambda_{12} = \sum_{i=1}^{11} \lambda_{\text{Si}} + \sum_{i=1}^{3} \lambda_{\text{ci}} \tag{15}$$

Substituting the value of λ_{12} in (14) the occupation of probability in state 1, i.e., operational state $P_1(t)$ has been computed as

$$P_1(t) = exp\left[-\left(\sum_{i=1}^{11} \lambda_{\text{Si}} + \sum_{i=1}^{3} \lambda_{\text{ci}}\right) t\right] \tag{16}$$

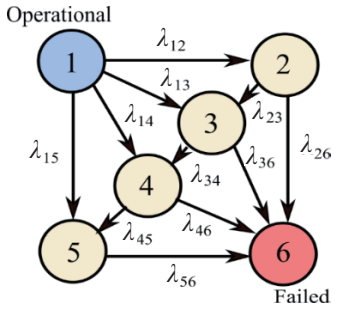

Fig. 7. State transition diagram of inverter with redundant switches.

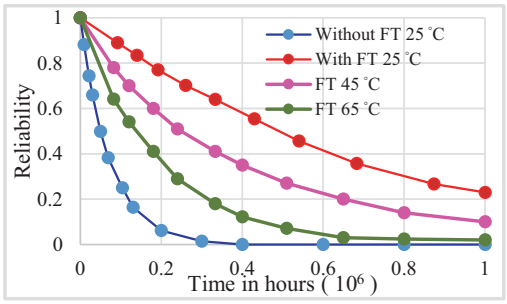

Fig. 8. Reliability curve of the FT inverter at 25 , 45, and 65 °C.

The procedure described in [20] calculates the switches and capacitors' component failure rate (λ). The reliability function of the inverter system without FT mode, is given by

$$R(t) = P_1(t) = e^{-0.13.912t} \tag{17}$$

B. Reliability With Redundant Switches

Markov reliability analysis is also extended to evaluate the enhanced reliability of the suggested fault-tolerance circuit in comparison with base topology. The reliability of the inverter system with redundant switches has been assessed by considering its five different states.

State 1: Converter is in the complete operational state. State 2: One switch failure (1 SW). State 3: Two switches failure (2 SW). State 4: One capacitor failure (1 CAP). State 5: Two capacitors failure (2 CAP). State 6: Complete converter failure. Also, it has to be noted that when any of the components fails, it is replaced with a new switching strategy, according to Table II, at the same time. The replacement time is so short that it can be neglected. The Markov chain diagram of the inverter with the proposed fault tolerant scheme has been shown in Fig. 7. The corresponding occupational probability during fault is given as,

$$A = \begin{bmatrix} -[\lambda_{12,13,14,15}] & \lambda_{12} & \lambda_{13} & \lambda_{14} & \lambda_{15} & 0 \\ 0 & -[\lambda_{23,26}] & \lambda_{23} & 0 & 0 & \lambda_{26} \\ 0 & 0 & -[\lambda_{34,36}] & \lambda_{34} & 0 & \lambda_{36} \\ 0 & 0 & 0 & -[\lambda_{45,46}] & \lambda_{45} & \lambda_{46} \\ 0 & 0 & 0 & 0 & -\lambda_{56} & \lambda_{56} \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{18}$$

The various failure rates are given as follows:

$$\begin{cases} \lambda_{12} = (\lambda_{S1-S12})P_R,\ \lambda_{13} = (\lambda_{2sw})P_R,\ \lambda_{14} = (\lambda_{C1-C3})P_R, \\ \lambda_{15} = (\lambda_{2CAP})P_R,\ \lambda_{23} = (\lambda_{S1-S12} + \lambda_{2sw})P_R, \\ \lambda_{34} = (\lambda_{2sw} + \lambda_{C1-C3})P_R,\ \lambda_{45} = (\lambda_{C1-C3} + \lambda_{2CAP})P_R, \\ \lambda_{26} = (\lambda_{S1-S12} + \lambda_{2sw})(1 - P_R),\ \lambda_{36} = (\lambda_{2sw} + \lambda_{C1-C3})(1 - P_R), \\ \lambda_{46} = (\lambda_{2CAP} + \lambda_{C1-C3})(1 - P_R),\ \lambda_{56} = (\lambda_{2CAP})(1 - P_R) \end{cases} \tag{19}$$

Where P_R is the probability of the satisfactory operation of the redundant switches, here, it is assumed $P_R = 0.9$.

After substituting various component failure rates in (7), the occupational probability function can be written as follows:

$$[P_1'(t)P_2'(t)P_3'(t)P_4'(t)P_5'(t)P_6'(t)] = [P_1(t)P_2(t)P_3(t)P_4(t)P_5(t)P_6(t)] \times A \tag{20}$$

$$P_1(t) = e^{-13.912t} \tag{21}$$

$$P_2(t) = 55.25\,(e^{-0.1307t} - e^{-0.13912t}) \tag{22}$$

$$P_3(t) = 2.467\,e^{-0.062t} - 95.13\,e^{-0.131t} + 92.66\,e^{-0.139t} \tag{23}$$

$$P_4(t) = 2.344\,e^{-0.02786t} - 4.3438\,e^{-0.0624t} + 56.24\,e^{-0.10307t} - 54.24\,e^{0.1391t} \tag{24}$$

$$P_5(t) = 0.1990\,e^{-0.0053t} - 0.4031\,e^{-0.02786t} + 329\,e^{-0.0624t} - 2.03\,e^{-0.1307t} + 1.90448\,e^{-0.13912t} \tag{25}$$

The reliability function is

$$R(t) = P_1(t) + P_2(t) + P_3(t) + P_4(t) + P_5(t) \tag{26}$$

$$R(t) = 0.1990\,e^{-0.53t} + 1.940\,e^{-02.786t} + 1.547\,e^{-06.24t} + 14.33\,e^{-013.07t} - 13.92552\,e^{-13.91t} \tag{27}$$

Fig. 8 illustrates the reliability over the operational time of the proposed inverter in both without and with a FT scheme at 25 °C, based on (17) and (25), respectively. The reliability curve at 45 °C and 65 °C ambient temperature with a FT scheme has also been shown to enhance the value of the proposed converter for various engineering applications. The FT inverter maintains higher reliability over time compared to the non-FT inverter at all temperatures due to the modified reference signal and the presence of redundant switches (T_{R1}–T_{R4}). As the temperature increases, the reliability of the FT inverter decreases, but it still performs better than the non-FT inverter. Thus, the proposed converter can work under single or multiple switch failure with improved reliability at varying ambient temperatures.

IV. Simulation and Hardware Validation

The performance of the proposed FT 7L inverter was validated using Matlab/Simulink and a 500 W hardware prototype shown in Fig. 9. System parameters for both hardware and simulation are provided in Table III. Open circuit (OC) switch faults were

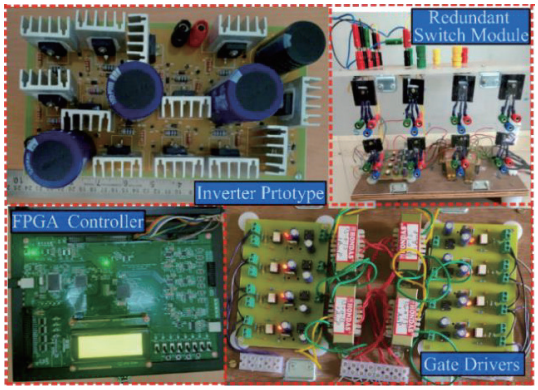

Fig. 9. Hardware setup of the proposed fault tolerant inverter.

TABLE III
PARAMETERS FOR SIMULATION AND HARDWARE VALIDATION

Parameters	Value /Part number
Input voltage (V_{dc})	110 V
Output voltage (v_{ac})	– 230 V (RMS)
Switching frequency (f_{sw})	5 kHz
Output frequency (f_{ref})	50 Hz
Filter capacitor (C_{flt})	5 µF
Filter inductor (L_{flt})	1 mH
Load parameter (R-L load)	500 W
Input capacitor (C_{in})	1000 µF, Electrolytic, TDK Elect. B43547
Switched capacitors (C_1, C_2, C_3)	1600 µF, Electrolytic, EPCOS B43544
Power switches	MOSFET IRFP460LCPBF
FPGA controller	SPARTAN6 XC6SLX4

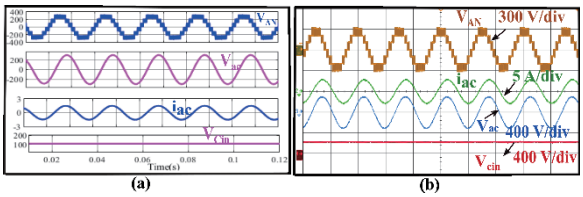

Fig. 10. Healthy inverter output level voltage (V_{AN}), filtered voltage (V_{ac}) and current (i_{ac}) and input voltage (V_{dc}). (a) Simulation. (b) Experimental result.

categorized into three groups for analysis: single switch fault, double switch fault, and triple switch fault, with detailed analysis for each group presented.

A. Healthy 7L Inverter

The Fig.10 shows the simulation and hardware results for the 7L inverter in healthy condition. It is observed that the phase voltage V_{AN} is nearly 326 V i.e., and top voltage level is almost thrice the inverter input voltage V_{dc}. The RMS voltage and current values at the output are 230 V and 2.1 A, respectively. Fig.11 shows that C_1, C_2, C_3 voltages are self-balanced during operation and maintaining the constant voltage across it.

B. Single Switch Fault

1) Fault on Switch T_2

Table II displays the fault tolerance analysis for different

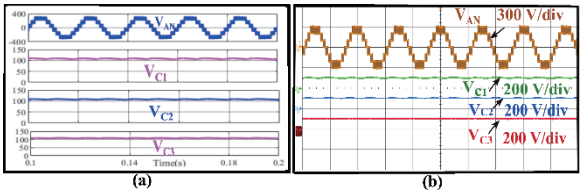

Fig. 11. Healthy inverter output level voltage V_{AN} and capacitor C_1, C_2 and C_3 voltages. (a) Simulation. (b) Experimental result.

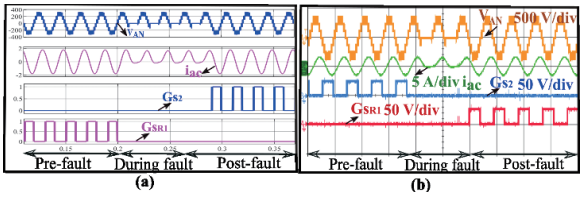

Fig. 12. Fault on switch T_2. (a) Simulation. (b) Experimental result.

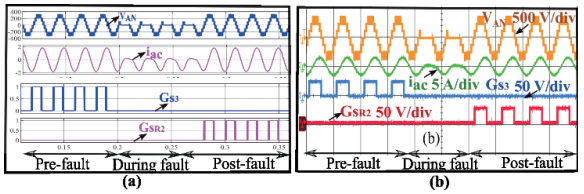

Fig. 13. Fault on switch T_3. (a) Simulation. (b) Experimental result.

switches in the proposed inverter. It indicates in case of a malfunction of switch T_2, the inverter can generate the full range of 7L voltages using redundant switches, similar to its healthy condition. Fig. 12 displays the simulation and practical waveforms for the switch T_2 fault condition. The simulation and hardware results indicate that when a fault occurs in switch T_2 at t = 0.2 s by withdrawing gate pulses G_{T2}, the output waveform exhibits only positive level voltage before the filter (V_{AN}) and discontinues current (i_{ac}) supply to the load. After clearing the fault at t = 0.6 s, switch T_2 is replaced with redundant switches T_{R1}, receiving gate pulse G_{TR1}. The inverter consistently produces a 7L output voltage and supplies the load during the post-fault state. The consistent number of on-state switches in both pre-fault and post-fault states indicates unchanged efficiency in both conditions.

2) Fault on Switch T_3

The simulation and experimental waveform for the switch T_3 fault condition are shown in Fig.13. It can be observed from the simulation and hardware results that when the fault occurs in switch T_3 at t = 0.2 s by with drawing gate pulses G_{T3} from it, the output waveform during the post-fault state, i.e., after clearing the fault at t = 0.26 s, the inverter switch T_3 has been replaced with the redundant switches T_{R2}, and the gate pulse G_{TR2} is given to it. The inverter continues to generate 7L output voltage and supply to the load, as in healthy cases, pre-fault and post-fault efficiencies remain the same. The faults in switches T_{10} and T_{11} can be analyzed like those in switches T_2 and T_3.

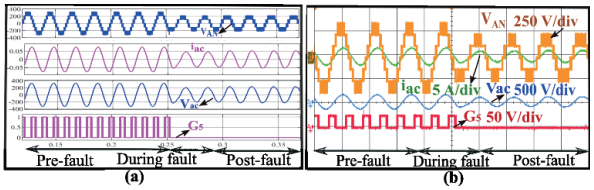

Fig. 14. Fault on switch T_5. (a) Simulation. (b) Experimental result.

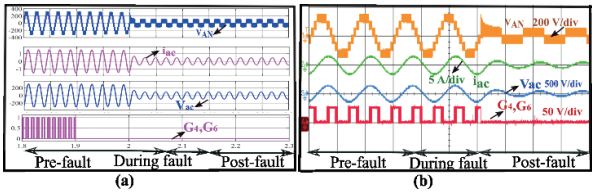

Fig. 15. Fault on switches T_4 and T_6 simultaneous. (a) Simulation. (b) Experimental result.

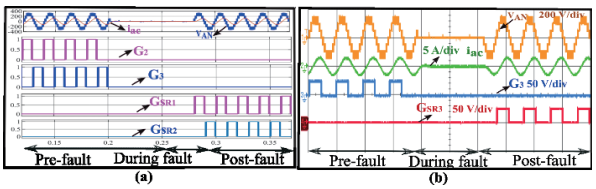

Fig. 16. Fault on switches T_2 and T_3 simultaneous. (a) Simulation. (b) Experimental result.

3) Fault on Switch T_5

Switch T_5 is an essential for charging C_2, and voltage level $\pm 3V_{dc}$ is not possible to generate at the output. Notably, applying a modified reference signal, as shown in Fig. 2(b), results in a 5L output voltage ($\pm 2V_{dc}$, $\pm V_{dc}$, 0) during post-fault operation. If T_5 experiences a fault, the output voltage level changes from seven to five levels, as illustrated in the simulation and experimental results shown in Fig. 14. Despite a slight reduction in power output, the inverter continues to supply power to the load.

C. Double Switch Fault

Fault on switch T_4 and T_6 simultaneously: The inverter circuit operation reveals that the switch T_4 and T_6 are essential for charging C_1 and C_2. When a fault occurs in switch T_4 and T_6 at the time $t = 1.9$ s by removing the gate pulse (G_4 and G_6), the inverter will shut down based on the discharge time of the three SCs. The PWM reference signal needs to be modified as in Fig. 2(c).

To maintain the continuity to supply sinusoidal voltage (V_{ac}) and current (i_{ac}) of load. Three output voltage (V_{AN}) levels, i.e, (0, $\pm V_{dc}$), can be generated with a modified PWM reference signal to continue the supply to the load, as shown in the simulation and hardware results in Fig. 15. Similarly, the simultaneous Fault on switches T_2 and T_3 can be analyzed as shown in the simulation and hardware results in Fig. 16.

D. Triple Switch Fault

Fault on switch T_2, T_3 and T_4 simultaneously: Fig. 17 presents the simulation and experimental results for the scenario in which switches T_2, T_3, and T_4 fail simultaneously. Both simulation and practical outcomes reveal that, by changing the PWM reference signal and replacing switches T_2 and T_3 with the redundant switches T_{R2} and T_{R3} as outlined in Table II, a 5L voltage, i.e., $\pm 2V_{dc}$, $\pm V_{dc}$,0 can be generated at the output.

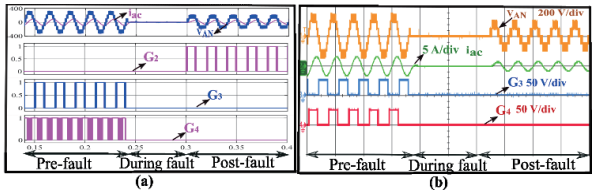

Fig. 17. Fault on switches T_2, T_3 and T_4 simultaneously. (a) Simulation. (b) Experimental result.

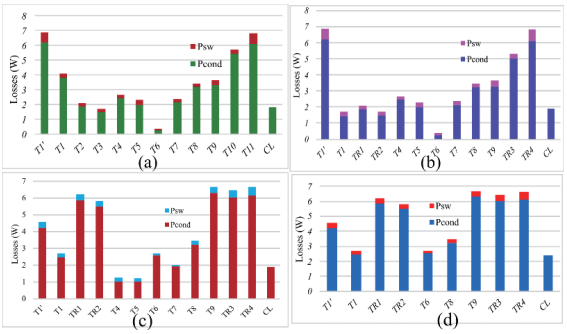

Fig. 18. Conduction (P_{cond}) and switching (P_{sw}) loss distribution of the proposed inverter. (a) 7L healthy. (b) 7L fault. (c) 5L fault. (d) 3L fault.

V. Voltage, Current Stress and Loss Analysis

The detail analysis of voltage and current stress for each switch and capacitor for a 7L operation of the proposed inverter is tabulated in Table IV. From which it can be noticed that switches T_2, T_3, T_{10}, and T_{11} have voltage stress three times the input voltage, while switches T_1' and T_5 have voltage stress nearly two times the input voltage. In contrast, the remaining switches and all the three capacitors (C_1, C_2 and C_3) have voltage stress almost the same as the input voltage of V_{dc}. The current stress profile of all the involved power switches for the proposed inverter has also been listed in Table IV, which revealed that four power switches of T_1, T_1', T_{10}, and T_{11} are tolerating the maximum current stress equal to around $4I_{max}$ whereas switch T_4, T_9 and capacitor C_1 has current of $2I_{max}$, all other switches and capacitors are having current stress almost equal to the peak output current I_{max}, i.e..

The conduction (P_{cond}) and switching (P_{sw}) loss distribution for the proposed inverter for healthy and all the fault conditions has been shown in Fig. 18. It can be observed that during healthy condition and 7L voltage post-fault condition, the power loss in the switches T_1, T_{10}, and T_{11} are slightly higher due to higher current and voltage stress. Meanwhile, in 5L and 3L output cases, T_{R1}, T_{R2}, T_{R3}, T_{R4} and T_9 switches have to undergo higher losses than other switches as they have high conduction time during fault. Fig. 19 illustrates the efficiency

TABLE IV
VOLTAGE AND CURRENT STRESS ACROSS THE VARIOUS COMPONENTS OF THE PROPOSED INVERTER

Switch	Voltage stress	Current stress	Switch/Capacitor	Voltage stress	Current stress
T_1	V_{dc}	$4I_{max}$	T_8	V_{dc}	I_{max}
T_1'	$2V_{dc}$	$4I_{max}$	T_9	V_{dc}	$2I_{max}$
T_2, T_{R3}	$3V_{dc}$	I_{max}	T_{10}, T_{R3}	$3V_{dc}$	I_{max}
T_3, T_{R4}	$3V_{dc}$	I_{max}	T_{11}, T_{R4}	$3V_{dc}$	$4I_{max}$
T_4	$2V_{dc}$	$2I_{max}$	C_1	V_{dc}	$2I_{max}$
T_5	V_{dc}	I_{max}	C_2	V_{dc}	I_{max}
T_6	V_{dc}	I_{max}	C_3	V_{dc}	I_{max}
T_7	V_{dc}	I_{max}	I_{max} = Peak load current		

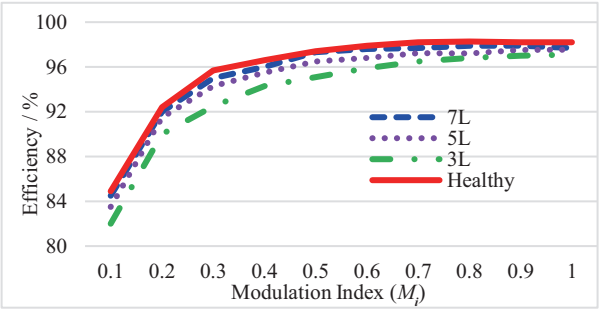

Fig. 19. Efficiency curve for the proposed converter at various switch fault conditions.

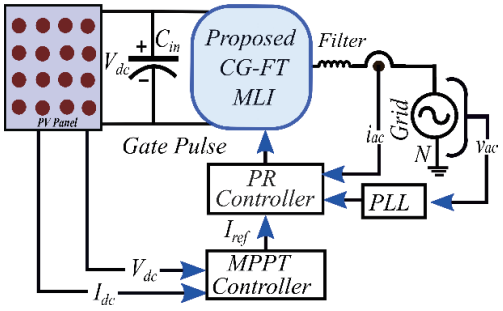

Fig. 20. Structure of the complete MPPT control system.

versus modulation index for the proposed inverter under healthy condition and post-fault output voltages at 7L, 5L, 3L conditions. During the 7L post-fault output, the inverter maintains efficiency comparable to healthy conditions in other it is slightly less.

VI. MPPT Approach for the Proposed Inverter

The block diagram for the complete MPPT control system is shown in Fig. 20 [27], [28]. The PV voltage (V_{dc}) and current (I_{dc}) are measured, and the perturb and observe (P&O) MPPT algorithm is applied to extract the maximum power from the PV system. The MPPT controller generates a I_{ref} signal, which is fed to the PR controller. The PR controller regulates the proposed CG-FT MLI's output voltage during varying environmental conditions and generates the gate pulses for the inverter. To verify operation of the proposed inverter in varying environmental conditions, the system is simulated in Matlab environment. ASM-M12-132-AAA-650 is selected from the Eternal Pride Series manufactured by Adani Solar for evaluating the functionality of the suggested converter and the power rating of the PV panel considered as 1500 W, OC voltage as 45.12 V and short circuit current as 9.36 A. The five PV modules are connected in series, and one module is connected in parallel. Fig. 21 (a) illustrates the step change in temperature from 60 °C to 1 °C. Correspondingly, PV terminal voltage has been changed.

To ensure the constant grid voltage irrespective of temperature changes, the modulation index (M_i) of the inverter is altered from 0.65 to 0.85. Furthermore, Fig. 21(b) illustrates the step change in insolation from 100 W/m^2 to 1000 W/m^2. Correspondingly, the PV current has changed significantly

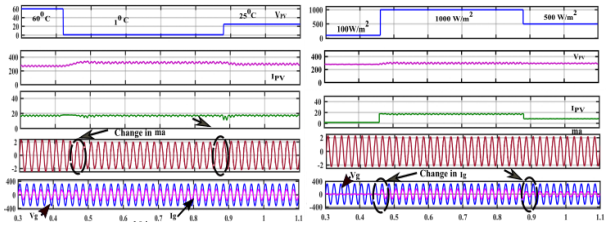

Fig. 21. Simulation results. (a) Step change in temperature. (b) Step change in insolation.

from 2 A to 5 A. As the modulation index is constant, the voltage remains constant. Further, the designed current controller effectively injects the current to the AC grid as per the insolation characteristics of the PV string. As the time required to track the MPPT is significantly longer than the inverter's switching period, it ensures the capacitors have sufficient time to charge before the next tracking cycle. Hence, MPPT has been achieved, and the proposed system is a suitable transformerless PV inverter system that boosts and reduces leakage current for grid-connection applications.

VII. Comparative Analysis

A comparative assessment has been conducted to highlight the uniqueness of the proposed converter in two ways, i.e., 1) Comparative analysis between the proposed inverter with other recent FT topologies. 2) Comparative analysis between the proposed inverter with traditional H-bridge inverter topologies. It is worth noting that the presented work has a common ground feature that distinguishes it from other fault-tolerant

TABLE V
COMPARATIVE ANALYSIS BERTWEEN PROPOSED AND RECENT FT TOPOLOGY

Converter topology	Ref.	N_{sw}	N_D	N_c	N_{SR}	N_{dc}	N_L	G	Control complexity	Leakage current	TSV	CF_{pu} (α=β=1)
FT-TLIs	[11]	8	2	1	4	1	5	1	Moderate	High	8	4.6
	[22]	12	-	3	4	3	7	2	High	High	8.5	11.7
	[13]	6	-	1	4	1	5	1	Moderate	High	8	3.8
	[16]	8	2	-	-	2	5	1	Moderate	High	8	7.2
	[23]	12	-	-	3	3	7	1	Less	High	15	12.8
	[14]	8	-	-	4	2	5	2	Moderate	High	9	8.4
FTCG-TLI	P	12	-	3	4	1	7	3	Less	Zero	7.33	3.7

N_{sw} = No. of switches, N_D = No. of diode, N_c = Capacitors, N_{SR} = Redundant switch, N_{dc} = No. of DC sources, N_L = No. of O/P voltage levels, G= Voltage gain, P = Proposed.

TABLE VI
COMARATIVE ANALYSIS BETWEEN PROPOSED INVERTER WITH TRADITIONAL H-BRIDGE INVERTER TOPOLOGIES

Inverter	Type	N_{sw}	N_d	N_{dc}	N_{Cap}	N_{ind}	N_{total}	Leakage current	Size*	Efficiency/%	CF	Reliability**	V_G
Traditional H-bridge Inverters	Boost +3L voltage	5	1	1	1	1	9	Not addressed	Moderate	98	5	Low	2
	Boost + 7L voltage	15	3	3	3	3	27	Not addressed	High	96	15.4	Low	2
Proposed MLI	7L voltage	12	0	1	3	0	16	Zero	Moderate	97.12	3.7	High	3

N_{sw} = No. of switches, N_d = No. of diodes, N_{dc} = No. of DC sources, N_{Cap} = No. of capacitors, N_{ind} = No. of inductors, N_{total} = Total, V_G = Voltage gain , component count.
*Size of the converter by including filter and component count. **High reliability due to FT operation.

inverters in the literature. Tables V and Table VI summarized the comparative analysis for recent FT and traditional H-bridge topology, respectively. Each attribute is detailed as follows.

A. Comparative Analysis Between the Proposed Inverter With Other Recent FT Topologies

1) Components Count ($N_{sw,}$ N_D, N_{sr}, N_c and N_{dc})

The component count is an essential criterion for selecting any inverter for a given application. Table V compares the proposed inverter with the other FT inverters in recent literature, based on the number of switches (N_{sw}), redundant switches (N_{sr}), diodes (N_D), capacitors (N_c), DC source (N_{dc}) requirements. The proposed converter has fewer component counts than [22] and [23]. However, the other features, such as static, zero leakage current, and self-voltage balancing, make it a unique inverter.

2) Leakage Current Handling Capabilities

The proposed converter has distinguished characteristics of negligible leakage current due to the common ground between source and load. This makes it unique from other 7L FT inverters in the recent literature. These features validate the suitability of the proposed inverter for PV applications.

3) Control Complexity

The proposed FT inverter has self-voltage balancing across SCs and negligible leakage current during pre-fault and post-fault periods. Hence, no extra circuitry or control strategy is needed to balance the capacitor voltages. Hence, the control complexity of the proposed topology is the least among the available FT MLI topologies.

4) TSV and CF

An inverter's capabilities cannot be justified only by its component count. The device rating is also an important parameter for selecting any converter for an application, which affects the cost of the inverter. It can be seen that the proposed topology has the least TSV as compared to other FT inverters. For a fair evaluation of the costs associated with different fault-tolerant multilevel inverters (FTMLIs), a CF detailed in [24]–[26] has been considered.

$$CF = \frac{N_{dc}}{N_L} \times \left[N_{SW} + N_D + N_{SR} + N_C + \left(\frac{\alpha \times TSV_{PU}}{\beta} \right) \right] \quad (28)$$

Here, α and β constants provide flexibility in weighting the significance of device count and TSV. The proposed topology's cost, is influenced by component count. A higher number of DC sources (N_{dc}) complicates voltage compatibility and isolation, impacting cost. The costs rise with more DC sources but decrease with more output voltage levels (N_L). The proposed topology achieves a 7L output with just one DC source, lowering its cost compared to other FT inverters in the literature.

5) Reliability of the Inverter

The previous section extensively analyzed the reliability of

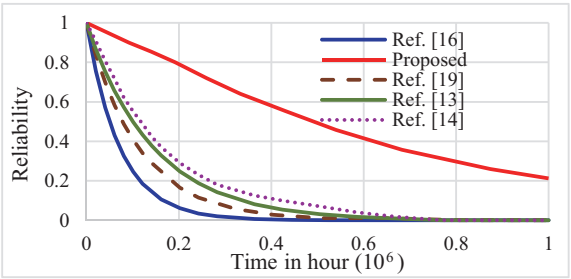

Fig. 22. Reliability curve of proposed inverter and inverters in [13], [14], [22], [16].

the proposed inverter, expressed by the reliability function (19). Comparative reliability calculations were also performed for the topology in references [13], [14], [16], [22]. The reliability plot in Fig. 22 indicates that the proposed inverter surpasses the referenced inverters in reliability. It exhibits tolerance to single and multiple switch faults with minimal modifications to the modulation scheme.

B. Comparative Analysis Between the Proposed Inverter With Traditional H-Bridge Inverter Topologies

To show the compatibility of the proposed inverter with traditional H-bridge inverter, a thorough comparison of the proposed inverter with traditional 3L and 7L H-bridge inverters integrated with a front-end boost converter has been carried out and tabulated in Table VI. It is noticed that the proposed FT inverter has the least CF as compared to the traditional H-bridge inverters by considering different parameters as (19). The traditional H-bridge based 3L inverter shows higher efficiency and lower component count. Also, the 7L H-bridge inverter requires a higher component count to realize the multi-level operation, which results in the lowest efficiency. Moreover, both the above-said topologies suffer from the issue of leakage current due to PV parasitic capacitance. They cannot be used directly for PV applications as per the German VDE 0126-1-1 standard. Further, the proposed inverter has FT capability and high reliability.

VIII. Conclusion

This paper introduces a 7L switched capacitor-based FT inverter with a common ground. This inverter showcases advanced capabilities, such as eliminating leakage current, self-balancing SC voltages, boosting voltage in regular, and FT modes, setting it apart with unique features. The reliability of the converter has been rigorously assessed through a Markov chain approach to reliability analysis.

Integrating redundant switches enhances fault tolerance and significantly elevates the overall reliability of the inverter compared to counterparts lacking such redundancy. The results explicitly confirm its superiority through comprehensive simulation and hardware testing, particularly in photovoltaic system-based inverter applications connected to loads requiring a continuous power supply. This research contributes valuable insights and practical advancements to power electronics and FT systems.

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