A Novel Topology and Modulation Strategy for the High-Gain Hybrid Active Neutral-Point-Clamped Three-Level Inverter

Chuanjing HOU, Desheng JIA, Changwei QIN , and Xiaoyan LI

***Abstract*—The hybrid active neutral-point-clamped (HANPC) three-level inverter (TLI) has the advantage of high efficiency and low cost due to the partial use of SiC devices. However, the magnitude of AC output voltage cannot exceed that of DC input voltage, which limits its application field. This paper puts forward a novel topology and modulation method of the high-gain HANPC TLI. The proposed topology combines the advantages of reduced count of SiC MOSFETs and single-stage boosting ability. To further improve system efficiency, a novel modulation method is designed, in which the SiC MOSFETs and Si IGBTs are operated in high frequency and fundamental frequency, respectively. To realize the function of voltage boosting without affecting the normal ac output voltage, the upper-shoot-through (UST) and lower-shoot-through (LST) states are inserted within the dwell times of small vectors. Moreover, the neutral point (NP) voltage balance is actively controlled by introducing a distribution factor to regulate duty cycle of redundant small vectors, which improve system reliability. Experimental tests verify the performance of the proposed topology and strategy.**

***Index Terms*—Hybrid active neutral-point-clamped (HANPC), neutral point (NP) voltage, quasi-Z-source, silicon carbide (SiC).**

I. Introduction

THE three-level inverter (TLI) has the distinct superiorities of reduced voltage stress of semiconductors, high efficiency, and small instantaneous rate of voltage change (dv/dt) [1], [2]. It has been extensively employed in varieties of industrial fields, such as photovoltaic power system, electric vehicles, and electric drive, etc [3]–[5].

Among a variety of multilevel inverters, the neutral-point-clamped (NPC) TLI is one typical topology that is utilized in medium and high voltage applications [6], [7]. However, it has the drawback of an uneven loss distribution among the semiconductors. To cope with this issue, the active NPC (ANPC) topology and its corresponding modulation scheme have been developed [8]–[10]. In the ANPC topology, the clamping diodes is replaced with the Si IGBTs.

In industrial applications, the efficiency as well as the power density is expected to be as high as possible, which means that the achievement of lower hardware cost [11]. Recently, with the development of SiC devices, a full-SiC active neutral-point-clamped (ANPC) TLI is proposed to enhance efficiency and power density [12]. Moreover, since SiC devices have lower switching loss, full-SiC ANPC TLI can be operated in higher switching frequency, and the filter size is reduced consequently. However, SiC devices are about four times as expensive as Si IGBTs, which greatly increases the system cost.

The Si/SiC hybrid converters is an alternative approach to achieve the tradeoff between performance and cost [13]. The SiC MOSFETs are used to replace part of Si IGBTs to construct hybrid active neutral-point-clamped (HANPC) topology [14]. Additionally, switching actions are shifted from Si IGBTs to SiC MOSFETs by utilizing the inherent redundancy states on each phase. Only the Si IGBTs are operated in fundamental frequency, which mitigates switching loss and improves system efficiency. However, similar to the conventional dc/ac converter, the HANPC TLI faces the problem that the amplitude of ac output voltage cannot exceed that of dc input voltage, which brings about limitations in practical applications. To solve this problem, a dc/dc boost circuit is usually configured to attain the desired voltage level. However, this configuration adds the control complexity [15], [16].

Fortunately, the emergence of quasi-Z-sources allows single-stage inverters to have voltage buck-boost capability, which can extend the output voltage range [17], [18]. Comparing with the two-stage solution, the power conversion stage is reduced, and dead-time of power devices is avoided, which effectively improves system reliability. Among single-stage inverters, the quasi-Z-source inverter maintains the superiority of continuous current and have been widely used in practical applications [19]. Recently, a reduced switch count (RSC) quasi-Z-source TLI has been proposed, which reduces the system cost and increases the output voltage range [20]. However, due to inherent

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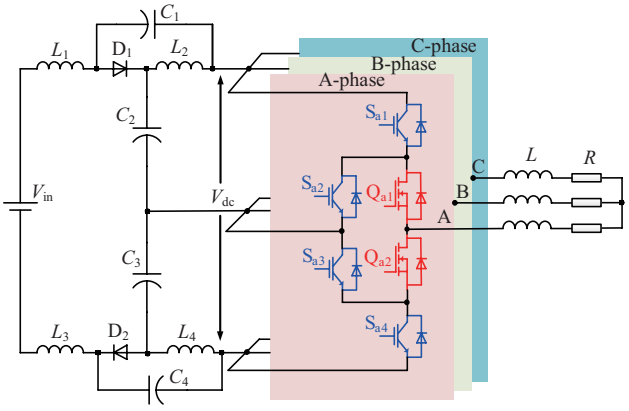

Fig. 1. Topology of the proposed novel high-gain HANPC TLI.

defects of the RSC TLI topology, the medium vector cannot be obtained, and at the same time, the switching state directly jump from [P] to [N] (or [N] to [P]) in one sampling period when designing the switching sequence, adding additional switching losses.

As the above analyses reveal, to further improve the performance and reduce system cost of the inverter, this paper presents a novel high-gain HANPC TLI, which consists of a quasi-Z-source network and a HANPC TLI. The novel high-gain HANPC TLI combines the advantages of quasi-Z-source and HANPC inverter [21]. To realize the normal operation and further improve efficiency of the proposed topology, a novel modulation strategy is also presented.

The major novelties of this paper include the following 4 points:

(1) In the proposed high-gain HANPC TLI, only one-third of the total power devices are SiC MOSFETs, and rest power devices are still Si IGBTs, which greatly reduces the system cost. Due to the combination with a quasi-Z-source, the adverse effect of dead time to the output waveform is avoided.

(2) The proposed novel modulation strategy is composed by low-frequency module and high-frequency module, which are used to drive the Si IGBTs and SiC MOSFETs, respectively. Using the novel modulation strategy, the power losses are further decreased, and system performance is also improved.

(3) The dc voltage boosting operation is realized by inserting an upper-shoot-through (UST), abbreviated as [U] and a lower-shoot-through (LST), abbreviated as [L] in the dwell times of small vectors, which broadens the output voltage range and extents topology application field.

(4) A distribution factor is presented to regulate dwell times of redundant small vectors, which realizes the active control of neutral point (NP) voltage and improves system reliability consequently.

II. Fundamentals of Proposed High-Gain HANPC TLI

In this section, a detailed descriptions of the novel high-gain HANPC TLI topology are presented, which include topology structure and operational principle.

Fig. 1 shows the structure of circuit for high-gain HANPC TLI, which consists of the dc power source, quasi-Z-source network, HANPC TLI, and load. The HANPC TLI comprises four Si IGBTs switches (S_{x1}, S_{x2}, S_{x3}, and S_{x4}) and two SiC MOSFETs switches (Q_{x1} and Q_{x2}) (x = a, b, c) in each phase. The quasi-Z-source network is deployed between the dc source and HANPC TLI. The dc power source voltage and input voltage of the HANPC TLI are indicated to V_{in} and V_{dc}, respectively.

TABLE I
Output States and Output Voltages Corresponding to Switching States of High-Gain HANPC TLI

Output state	Output voltage	Switching states (x = a, b, c)					
		S_{x1}	S_{x2}	S_{x3}	S_{x4}	Q_{x1}	Q_{x2}
[P]	$V_{dc}/2$	1	0	1	0	1	0
[O+]	0	1	0	1	0	0	1
[U]	0	1	0	1	0	1	1
[O−]	0	0	1	0	1	1	0
[N]	$-V_{dc}/2$	0	1	0	1	0	1
[L]	0	0	1	0	1	1	1

All the switching states corresponding output states and voltage levels of the high-gain HANPC TLI are summed up in Table I, where "1" and "0" represent the on and off states of semiconductor devices, respectively. In this way, six different output states can be generated in the proposed high-gain HANPC TLI. Notably, the NPC TLI merely having three output states [P], [N], and [O], the proposed topology contains six output states [P], [N], [O+], [O−], [U] and [L]. With the above characteristics, the high-gain HANPC TLI has the potential to boost input dc voltage and equalize the distribution of switching losses.

As we all know that the switching losses of SiC MOSFET device is about one-third to one-fifth of that of Si IGBTs device with the same power rating [22]. Nevertheless, the SiC MOSFETs is approximately four times more expensive than Si IGBTs. In the proposed topology, only a third of the semiconductors are SiC MOSFETs, and rest of power switches are Si IGBTs, which reduce the system cost, consequently.

By designing a reasonable modulation strategy, the six SiC MOSFETs can operate in high-frequency mode and the twelve Si IGBTs can operate in fundamental frequency mode, which further reduces switching losses, and thus improves system efficiency [23]−[25]. To realize dc input voltage boosting and maintain the reduced switching losses, a new modulation method is presented in Section IV.

III. Comparative Summary and Design Guidelines

A. Comparison of the High-Gain HANPC TLI With Other TLI Based on Impedance Sources or SiC Devices

The detailed comparisons of the high-gain HANPC TLI and the existing TLI based on impedance sources or SiC devices have been conducted, which including Z-source neutral-point clamped (NPC) TLI with two separated impedance networks

TABLE II
COMPARISONS OF DIFFERENT THREE-LEVEL INVERTERS BASED ON IMPEDANCE-SOURCE OR SIC DEVICES

Parameter	ZS NPC3L with 2-LC [26]	ZS 3LT^{2}I [27]	QZS 3LT^{2}I [28]	Full-SiC ANPC TLI [12]	High-gain HANPC TLI
DC sources	2	1	1	1	1
Inductors	4	2	4	0	4
Capacitors	4	4	4	2	4
Diodes	8	2	2	0	2
Si switches	12	12	12	0	12
SiC switches	0	0	0	18	6
Power density	Low	Low	Low	High	High
Total price of power devices (CNY)	304.92	211.32	242.32	1103.73	610.23
Shoot-through duty cycle	$1-m$	$1-m$	$1-m$	0	$1-m$
Boost factor	$1/(1-2d_f)$	$1/(1-2d_f)$	$1/(1-2d_f)$	1	$1/(1-2d_f)$
Voltage gain	$m\cdot B$	$m\cdot B$	$m\cdot B$	m	$m\cdot B$
Input current characteristics	Discontinuous	Discontinuous	Continuous	Continuous	Continuous
Whether dead time is required	No	No	No	Yes	No
Capacitor voltage stress	$\frac{(1-d_f)V_{in}}{2(1-2d_f)}$	$\frac{(1-d_f)V_{in}}{1-2d_f}$	C_1 and C_4: $\frac{d_fV_{in}}{2(1-2d_f)}$, C_2 and C_3: $\frac{(1-d_f)V_{in}}{2(1-2d_f)}$	$\frac{V_{in}}{2}$	C_1 and C_4: $\frac{d_fV_{in}}{2(1-2d_f)}$, C_2 and C_3: $\frac{(1-d_f)V_{in}}{2(1-2d_f)}$
Line voltage	Five-level	Five-level	Five-level	Five-level	Five-level

(ZS NPC3L with 2-LC) [26], Z-source three-level T-type inverter (ZS 3LT2I) [27], quasi-Z-source three-level T-type inverter (QZS 3LT2I) [28] and full-SiC active neutral-point-clamped TLI (Full-SiC ANPC TLI) [12].

Table II summarizes the detailed comparisons of different TLI. Compared with the conventional Z-source inverter, the proposed high-gain HANPC TLI draws a continuous input current, since the inductor is directly connected to the DC power source. When compared to the traditional quasi-Z-source T-type and NPC TLI, the high-gain HANPC TLI boasts higher power density and efficiency. In contrast to the full-SiC ANPC TLI, the proposed high-gain HANPC TLI topology employs only six SiC devices, the system cost can be reduced accordingly. The hybrid ANPC requires much fewer SiC MOSFETs than a full-SiC ANPC inverter while providing a comparable power density [29].

B. Design Criterion and Formulations for Passive Components in the High-Gain HANPC TLI

The design criterion and formulations for passive components in the quasi-Z-source network are elaborated as follows.

Since the high-gain HANPC TLI belongs to one kind of quasi-Z-source inverter in essence, the passive components in the quasi-Z-source network are designed by referring the methodology presented in [20], [30].

The inductances are calculated by

$$L_1 = L_2 = L_3 = L_4 \geqslant \frac{V_{in}^2\cdot(1-d_f)\cdot d_f}{2\cdot P_{out}\cdot f_{sw}\cdot k_L\cdot(1-2d_f)} \tag{1}$$

where V_{in}, d_f, P_{out}, f_{sw}, and k_L are the dc input voltage, shoot-through duty cycle, output power of the inverter, switching frequency, and the current ripple factor of inductors, respectively.

The capacitances are formulated by

$$C_1 = C_4 \geqslant \frac{2\cdot P_{out}}{V_{in}^2\cdot k_{C1,4}\cdot f_{sw}}\cdot(1-2d_f) \tag{2}$$

$$C_2 = C_3 \geqslant \frac{2\cdot P_{out}}{V_{in}^2\cdot k_{C2,3}\cdot f_{sw}}\cdot\frac{1-2d_f}{1-d_f}\cdot d_f \tag{3}$$

where $k_{C1,4}$ is the voltage ripple factor of capacitors C_1 and C_4, while $k_{C2,3}$ is the voltage ripple factor of capacitors C_2 and C_3.

In the designed high-gain HANPC TLI, the current ripple factor of inductors (k_L) is selected as 0.6. $k_{C1,4}$ is selected as 0.0009, while $k_{C2,3}$ are selected as 0.0007. The maximum dc input voltage is 400 V, the maximum output power is 4 kW, and the switching frequency is 10 kHz.

Based on the above parameters, the values of capacitors and inductors can be calculated. The inductance of L_1, L_2, L_3, and L_4 is selected as 1 mH, the capacitance of C_1 and C_4 is chosen as 2350 μF, and the capacitance of C_2 and C_3 is selected as 1410 μF. In the experimental verification, it is noted that C_1 and C_4 are

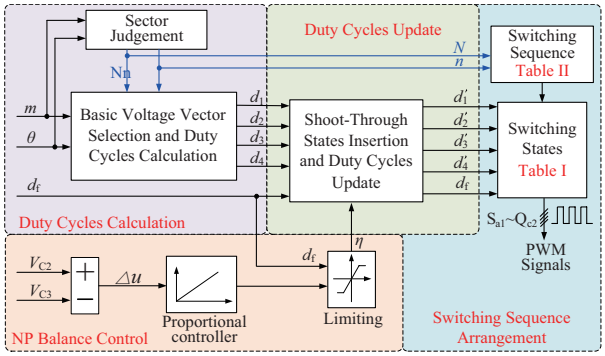

Fig. 2. Overall diagram of the proposed novel modulation method.

built by connecting five 470 μF / 450 V electrolytic capacitors in parallel, while C_2 and C_3 are built by connecting three 470 μF / 450 V electrolytic capacitors in parallel. For the diodes in the quasi-Z-source network, the fast recovery epitaxial diode (FRED) DSEI60-06A is selected.

IV. Proposed Novel Modulation Scheme

The proposed strategy consists of four steps. Firstly, according to the sector and region of the reference voltage vector (V_{ref}), basic vectors are selected, and the corresponding duty cycles are calculated for synthesizing the V_{ref}. For the second part, the capacitor voltages V_{C2} and V_{C3} are actively controlled in balance by introducing the distribution factor (η). For the third part, depending on the η and the set shoot-through duty cycle (d_f), the durations of small vectors are adjusted, which implements the boost function and maintains the normal output waveforms. At last, the switching sequences of SiC MOSFETs and Si IGBTs are designed separately, and the hybrid frequency pulse driving signals are generated. The control diagram is given in Fig. 2. For each part, the design process is elaborated below.

A. Basic Vectors Selection and Duty Cycles Calculation

With the different output states of three phases, the space vector diagram (SVD) of high-gain HANPC TLI is illustrated in Fig. 3, which includes 27 non-shoot-through basic voltage vectors. It should be noted that since quasi-Z-source network is included in the proposed high-gain HANPC TLI, the shoot-through vectors consisting of [U] and [L] states can be generated for voltage boosting operation.

According to the values of m and θ of the V_{ref}, the sector and region number of the V_{ref} location can be determined, where θ and m are the phase angle and modulation index of V_{ref}, respectively. Only the location of V_{ref} is determined, the basic voltage vectors can be selected consequently.

In each sector, the duration calculation of selected vectors still follows the same principles of conventional three-level space vector modulation (3L-SVM) [31], which is also based on "volt-second balancing" formula. As shown in Fig. 4, when V_{ref} is located in the region 5 of sector I (abbreviated as I-5), the "nearest three vectors" (NTV) scheme is utilized. Four basic voltage vectors are chosen according to the NTV principle, i.e., [ONN], [PNN], [PON], [POO], and the duty cycles are noted as d_1, d_2, d_3 and d_4, respectively. The formula that calculates the

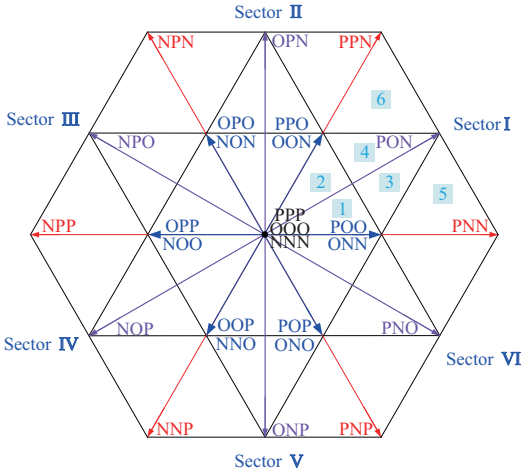

Fig. 3. SVD of high-gain HANPC TLI.

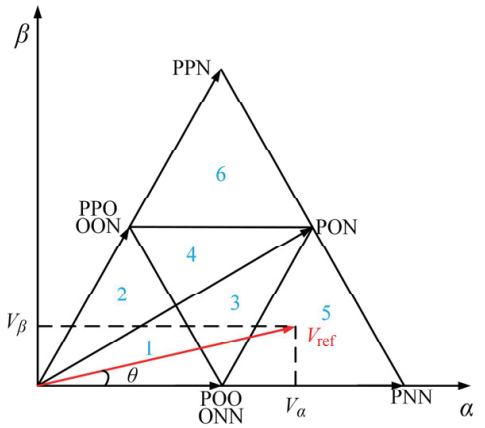

Fig. 4. SVD of the sector I for the high-gain HANPC TLI.

duty cycles are given in (4):

$$\begin{cases} V_{ref}\cos\theta = \dfrac{V_{in}}{3}\cdot d_1 + \dfrac{2V_{in}}{3}\cdot d_2 + \dfrac{\sqrt{3}V_{in}}{3}\cdot\dfrac{\sqrt{3}}{2}\cdot d_3 + \dfrac{V_{in}}{3}\cdot d_4 \\ V_{ref}\sin\theta = \dfrac{\sqrt{3}V_{in}}{3}\cdot\dfrac{1}{2}\cdot d_3 \\ d_1 + d_2 + d_3 + d_4 = 1 \\ d_1 = d_4 \end{cases} \tag{4}$$

The duty cycles of d_1, d_2, d_3 and d_4 can be calculated as:

$$\begin{cases} d_1 = 1 - \dfrac{\sqrt{3}V_{ref}}{V_{in}}\sin\left(\dfrac{\pi}{3}+\theta\right) \\ d_2 = \dfrac{2\cdot\sqrt{3}V_{ref}}{V_{in}}\sin\left(\dfrac{\pi}{3}-\theta\right) - 1 \\ d_3 = \dfrac{2\cdot\sqrt{3}V_{ref}}{V_{in}}\sin\theta \\ d_4 = 1 - \dfrac{\sqrt{3}V_{ref}}{V_{in}}\sin\left(\dfrac{\pi}{3}+\theta\right) \end{cases} \tag{5}$$

Generally, following the principle of conventional 3L-SVM, the switching sequence is designed to [ONN]-[PNN]-[PON]-[POO]-[PON]-[PNN]-[ONN]. It should be noted that the [O] state contains two states, [O_+] and [O_-], which are determined by its neighboring states, [O_+] states are only adjacent to [P] and [U] states, [O_-] states are only adjacent to [N] and [L]. Based on the above principles, the least switching times and switching losses are guaranteed, and the actual switching sequence is designed as [O_+NN]-[PNN]-[PO_N]-[PO_O_]-[PO_N]-[PNN]-[O_+NN].

B. NP Voltage Balance Active Control

A distribution factor is introduced to regulate duty cycles of redundant small vectors, thus realizing the NP voltage balance.

First, the voltages across C_2 and C_3 are sampled, and noted as V_{C2} and V_{C3}, respectively. Next, the difference between V_{C2} and V_{C3} is adjusted by a proportional controller, and η is obtained as:

$$\eta = p \cdot (V_{C2} - V_{C3}) \tag{6}$$

where p is the proportional control factor.

Lastly, the limiting of η is required to prevent voltage distortion, the formula is given in (7).

$$-(1-m-d_f) < \eta < 1-m-d_f \tag{7}$$

C. Shoot-Through States Injection and Duty Cycles Update

In the case of the proposed method, the utilization of [U] and [L] states enable the implementation of boost function. [U] and [L] are injected within the dwell time of small vectors. Additionally, the duration of small vectors is adjusted through modification of the NP voltage distribution factor.

Considering the addition of NP voltage balance control scheme and the injection of [U] and [L] states, the duty cycles of basic voltage vectors are revised as:

$$\begin{cases} d_1' = d_1 - d_f - \eta \\ d_2' = d_2 \\ d_3' = d_3 \\ d_4' = d_4 - d_f + \eta \end{cases} \tag{8}$$

The dwell times of basic voltage vectors can be calculated as:

$$\begin{cases} T_*' = d_*' \cdot T_s \\ T_{UST} = T_{LST} = d_f \cdot \dfrac{T_s}{2} \end{cases} \tag{9}$$

where * represents the segment of the switch sequence (1, 2, 3 and 4) and T_s is the sampling period.

D. Switching Sequences Arrangement and Drive Signals Generation

The design of switching sequences should follow certain principles, which ensure the quality of the output waveforms and as few switching times as possible.

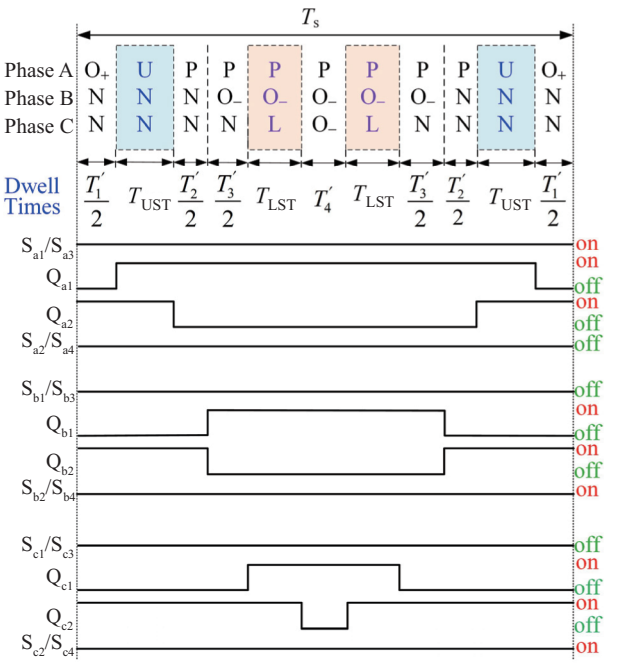

Fig. 5. Switching sequence and switching states in sector I-5.

The [U] and [L] states are inserted, and the boost function is implemented. Simultaneously, the dwell times of the redundant small vectors are adjusted for achieving NP voltage balance. As the above analyses demonstrate, eleven segment switching sequences are arranged, the actual switching sequence (I-5) is designed as [O_+NN]-[UNN]-[PNN]-[PO_N]-[PO_L]-[PO_O_]-[PO_L]-[PO_N]-[PNN]-[UNN]-[O_+NN].

When the V_{ref} is located in I-5, the arranged switching sequence and the switching state of power devices are drawn in Fig. 5. In one sampling period, the output states of each phase change between [P], [O_+] and [U] states or between [N], [O_-] and [L] states, and the switching states of Si IGBTs are always turn-on or turn-off. For example, for phase A, the output states change between [P], [O_+] and [U] states. The Si IGBTs of S_{a1}, S_{a3} are always turn-on, and S_{a2}, S_{a4} are always turn-off in one sampling period. While the switching states of SiC MOSFETs switch turn-on and switch turn-off one time in one sampling period. Thus, the working frequency of SiC MOSFETs is equal to sampling frequency, which is defined as high frequency modulation. Considering the symmetry of SVD, the rules of switching sequences in other sectors are similar to above analysis and will not repeat here.

For phase B and phase C, output states have similar changing law. Table III summarizes the output states of each phase in one fundamental period. Therefore, the working frequency of all Si IGBTs in the proposed high-gain HANPC TLI is equal to fundamental frequency, which is defined as fundamental frequency modulation.

V. Simulation Results

The effectiveness of the proposed topology and scheme is demonstrated by adopting MATLAB software. Since the high-

TABLE III
THE SECTOR AND REGION FOR POSITIVE CYCLE AND NEGATIVE CYCLE IN ONE FUNDAMENTAL PERIOD

Phase	Sector and region	
	Positive cycle [P], [O+], [U]	Negative cycle [L], [O-], [N]
A	I-3, 4, 5, 6 II-3, 5 V-4, 6 VI-3, 4, 5, 6	II-4, 6 III-3, 4, 5, 6 IV-3, 4, 5, 6 V-3, 5
B	I-4, 6 II-3, 4, 5, 6 III-3, 4, 5, 6 IV-3, 5	I-3,5 IV-4, 6 V-3, 4, 5, 6 VI-3, 4, 5, 6
C	III-4, 6 IV-3, 4, 5, 6 V-3, 4, 5, 6 VI-3, 5	I-3, 4, 5, 6 II-3, 4, 5, 6 III-3, 5 VI-4, 6

TABLE IV
PARAMETERS FOR SIMULATION AND EXPERIMENTAL TEST

Parameter	Value
DC Voltage (V_{in})	70 V
AC output frequency (f)	50 Hz
Sampling period (T_s)	100 μs
Sampling frequency (f_{SF})	10 kHz
Inductors (L_1, L_2, L_3, and L_2)	1 mH
DC-link capacitors (C_1 and C_4)	2350 μF
DC-link capacitors (C_2 and C_3)	1410 μF
RL load	R_{load} = 10 Ω/20 Ω L_{load} = 4 mH

gain HANPC TLI is essentially a type of quasi-Z-source TLI, the design of passive components in quasi-Z-source is referred to [20] and [30]. The parameters for both simulation and experimental tests are given in Table IV. The high-gain HANPC TLI can be operated in non-boost and boost modes as required, in non-boost mode, the shoot-through state is not required.

To verify the effect of different gains on the total harmonic distortion (THD) of current at the same power, four different operation conditions are compared and analyzed: (a) $m = 0.8$, $d_f = 0$, (b) $m = 0.7$, $d_f = 0.05$, (c) $m = 0.8$, $d_f = 0.1$, (d) $m = 0.7$, $d_f = 0.15$.

Fig. 6 displays the simulated results in steady state, and the total harmonic distortion of output current (THDi) is also given. The proposed high-gain HANPC TLI belongs to one kind of quasi-Z-source inverter in essence. Due to the injection of the shoot-through state, the input voltage of the HANPC TLI (V_{dc}) is changed to a pulse waveform, while the normal ac output voltage is not affected [30].

Fig. 6 (a) shows the output waveform in non-boost mode. At this time, the system modulation index (m) and the shoot-through d_f are set as 0.8 and 0, respectively. The dc input voltage (V_{in}) is set to be 70 V, and the dc-link voltage (V_{dc}) is equal to the dc input voltage. The voltages of dc-link capacitors C_2 and C_3 are balanced at 35 V, which is half of the dc-link voltage

TABLE V
COMPARISON OF THD AND POWER LOSS OF HIGH-GAIN HANPC TLI FOR DIFFERENT OPERATING CONDITIONS

Parameter	$m = 0.8$ $d_f = 0$	$m = 0.7$ $d_f = 0.05$	$m = 0.8$ $d_f = 0.1$	$m = 0.7$ $d_f = 0.15$
Output Power/W	215	215	335	335
THDi/%	0.80	0.86	0.88	0.89
Total Power Loss/W	1.6	1.764	3.08	3.513

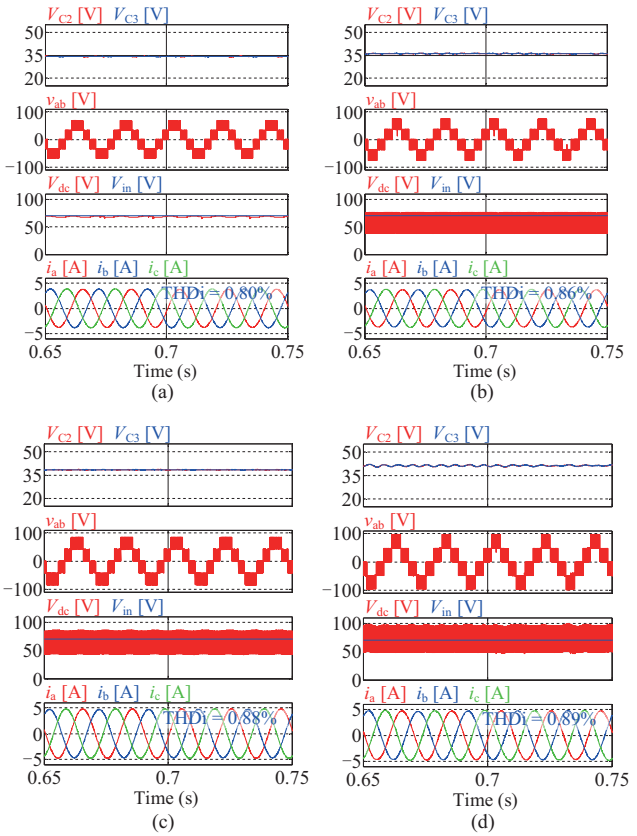

Fig. 6. Simulation results in different operation conditions. (a) $m = 0.8$, $d_f = 0$. (b) $m = 0.7$, $d_f = 0.05$. (c) $m = 0.8$, $d_f = 0.1$. (d) $m = 0.7$, $d_f = 0.15$.

magnitude. The waveform of line voltage (v_{ab}) has five levels, that is, 0, ±35 V, and ±70 V, which validate the correctness of the designed modulation scheme. Moreover, three-phase output currents (i_a, i_b, and i_c) are symmetrical and sinusoidal.

The simulation results in boost mode are shown in Fig. 6 (b)−(d), respectively. It is clearly observed that the dc-link voltage becomes pulse waveform, whose magnitude is higher than the dc input voltage due to the utilization of shoot-through states. It can be concluded that the voltage boosting capability is realized. Table V summarizes the THD of the current and the output power for various operating conditions. Under the condition of keeping the output power constant, the THD of the current shows an upward trend with the increasing of the through duty cycle. However, the quality of the current waveform can still be well guaranteed.

The gate signals of all power switches in phase A of the inverter are demonstrated in Fig. 7. In one fundamental period,

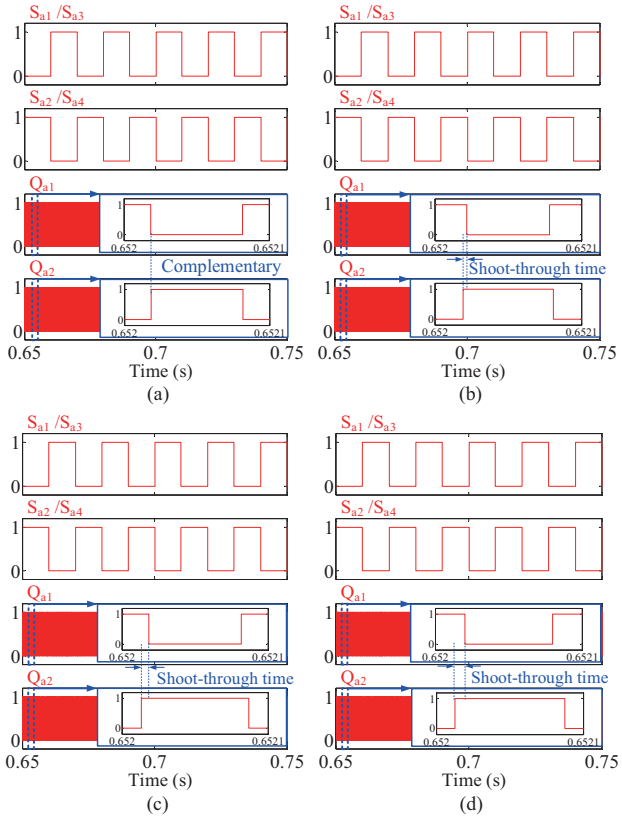

Fig. 7. Drive signals of power switches in different operation conditions. (a) $m = 0.8$, $d_f = 0$. (b) $m = 0.7$, $d_f = 0.05$. (c) $m = 0.8$, $d_f = 0.1$. (d) $m = 0.7$, $d_f = 0.15$.

the Si IGBTs S_{a1}, S_{a2}, S_{a3}, and S_{a4} only switch once. It is easy to see that the switching action is mainly shifted to SiC devices with better switching loss performance. The Si devices operate solely at the fundamental frequency to minimize switching loss. On the other hand, the drive signals of Q_{a1} and Q_{a2} are complementary in the non-boost mode, and in the boost mode, the drive signals of Q_{a1} and Q_{a2} exhibit shoot-through time, and a higher shoot-through duty cycle results in an extended shoot-through duration.

The proposed quasi-Z-source inverter should preferably operate under high modulation condition when voltage boosting (output voltage greater than V_{in} and with shoot-through states inserted) is commanded [32]. In order to verify that the system can operate normally under different m, indices m changes from 0.8 to 0.7, and the dynamic output results are shown in Fig. 8. Obviously, the output current is proportionally decreased with the reduction of m in both boost and non-boost modes, while the voltage boosting capacity is not influenced.

To verify the effectiveness of the NP voltage balance control strategy, an extra 500 Ω resistor is connected in parallel with C_2, Fig. 9 shows the simulated waveforms. Originally, the NP voltage balance control is enabled, V_{C2} and V_{C3} are balanced. The NP voltage balancing control is manually disabled when the simulation time is 0.7 s. Accordingly, V_{C2} and V_{C3} are separated. In both non-boost and boost modes, the effectiveness of the NP voltage balance control is verified. When the load resistance changes in step, simulated waveforms are depicted

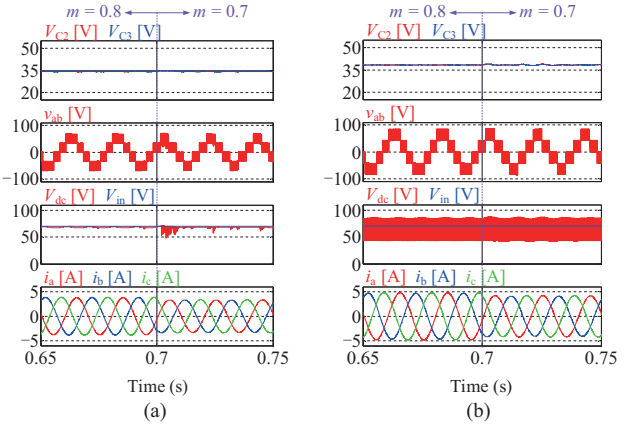

Fig. 8. Simulated waveforms of when the modulation index changes from 0.8 to 0.7. (a) $d_f = 0$. (b) $d_f = 0.1$.

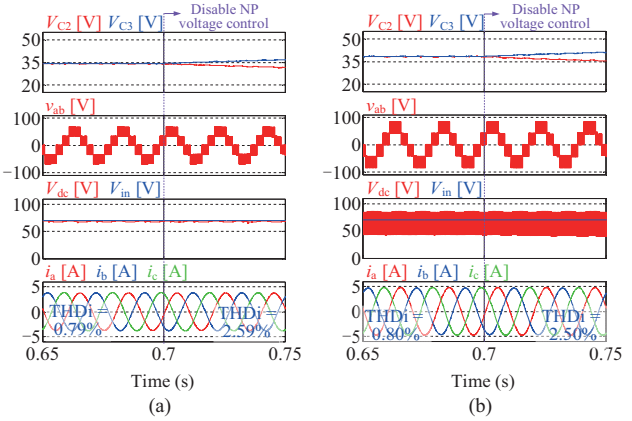

Fig. 9. Simulated waveforms with or without NP voltage balance control. (a) $m = 0.8$, $d_f = 0$. (b) $m = 0.8$, $d_f = 0.1$.

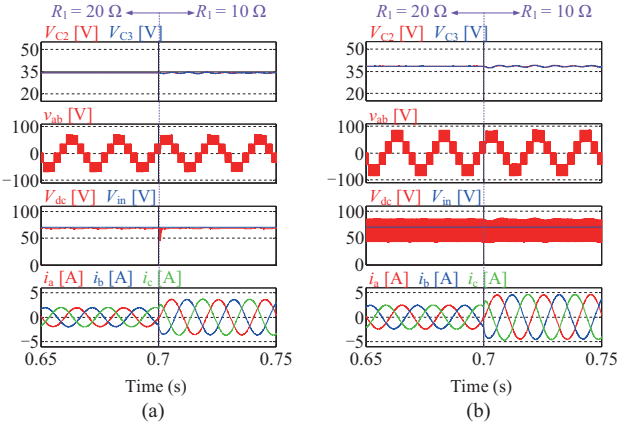

Fig. 10. Simulated waveforms with load changes. (a) $m = 0.8$, $d_f = 0$. (b) $m = 0.8$, $d_f = 0.1$.

in Fig. 10. It is observed that the proposed scheme ensures the stable operation of the high-gain HANPC TLI under both conditions.

Fig. 11 displays the losses of power devices in the high-gain HANPC TLI, which are obtained by adopting MATLAB/

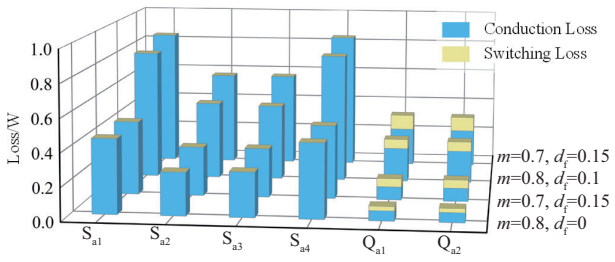

Fig. 11. Loss distribution for high-gain HANPC TLI.

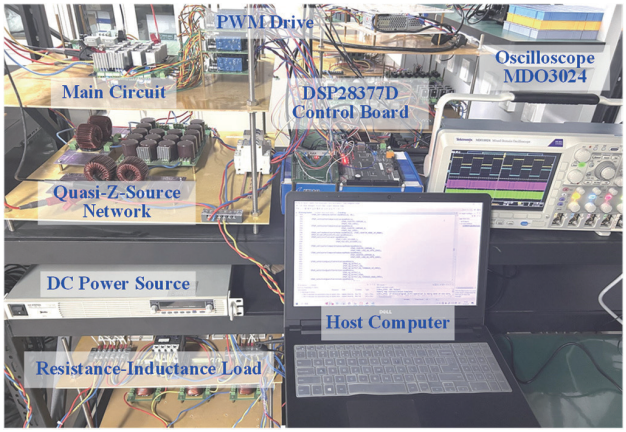

Fig. 12. Photograph of the hardware-based test rig.

Simulink and PLECS Blockset. According to the symmetrical characteristics of the topology, the loss of S_{a1} is identical to that of S_{a4}, and similar conclusions can be obtained for other power switches. It is noted that the losses of power switches include those of the body diodes. It is seen that the conduction losses accounts for the majority of the total power loss. Overall, the losses of power devices are relatively equalized.

Under the condition of consistent output power, it is observed that the increase in the d_f leads to a slight increase in power loss. Further analysis shows that the switching loss shows a significant upward trend when the output power is increased. Based on the above observations, it is reasonable to infer that the power loss is mainly affected by the output power and also modulated to some extent by the d_f.

VI. Experimental Results

To validate the performance of the proposed topology and modulation scheme, an experimental test system of the high-gain HANPC TLI is designed, as shown in Fig. 12.

The digital signal processor of the control board is TMS320 F28377D from Texas Instruments. The IGBT IKW50N65EH5 is adopted for power switches S_{x1}–S_{x4}, while the MOSFET IMW65R027M1H is adopted for power switches Q_{x1}–Q_{x2}.

Fig. 13 shows the operating waveforms of the high-gain HANPC TLI in non-boost mode. At this time, the m and d_f are set as 0.8 and 0, respectively. The capacitor voltages V_{C2} and V_{C3} are maintained at 35 V, i.e., $V_{in}/2$. The line voltage (v_{ab}) is five level waveforms, which comprise 0, ±35 V, and ±70 V. In addition, the load currents (i_a, i_b, and i_c) are symmetrical and sinusoidal, which verified the validity of the proposed modulation method.

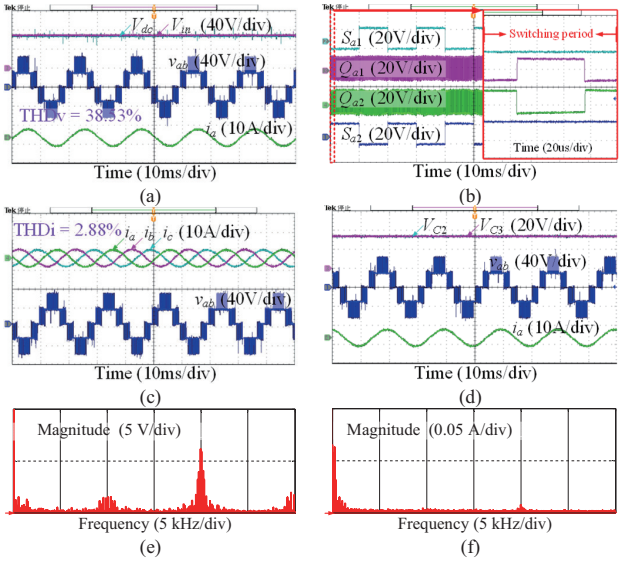

Fig. 13. Experimental results in non-boost mode. (m = 0.8 and d_f = 0). (a) DC power source voltage, input voltage of the HANPC TLI, phase A output currents and line voltage. (b) Drive signals of power switches. (c) Three-phase output currents and line voltage. (d) Voltages across dc-link capacitors, line voltage and phase A output currents. (e) Spectrum of line voltage. (f) Spectrum of output current.

As observed from Fig. 13(b), the drive signals of the power switches are consistent with the simulation results. It can be found that the Si IGBTs S_{x1}, S_{x2}, S_{x3}, and S_{x4} only switch once in one fundamental period. As it can be observed from the enlarged figure, the working frequency of SiC MOSFETs is equivalent to the sampling frequency. Furthermore, Q_{a1} and Q_{a2} are complementary signals that exhibit no shoot-through state. While the SiC MOSFETs Q_{x1} and Q_{x2} operate in high frequency switching of 10 kHz. In this case, the voltages across capacitors C_2 and C_3 are about 35 V, and the NP voltage balance is guaranteed by the proposed method, as shown in Fig. 13(d).

The spectra of v_{ab} and i_a are obtained using MATLAB software, which are provided in Fig. 13(e) and (f), respectively. These spectra show that the main components of v_{ab} and i_a are concentrated at 50 Hz, switching frequency (10 kHz) and multiples of switching frequency.

Fig. 14 displays the experimental waveforms in boost mode, and the d_f is set as 0.1. The V_{dc} is changed to a pulse waveform. It is noticed that the line voltage and current amplitude have increased. In non-boost mode (m = 0.8, d_f = 0), the amplitude of the line voltage is about 64 V. In addition, the load currents (i_a, i_b, and i_c) are symmetrical and sinusoidal, the amplitude of output current is about 3.8 A. In boost mode (m = 0.8, d_f = 0.1), the amplitude of the line voltage is increased to about 80 V and the amplitude of output current is increased to about 4.7 A. Noteworthy, there is some attenuation of voltage and current as it passes through the transducer and oscilloscope display, but the values of voltage and current increase before and after boosting are in accordance with (10).

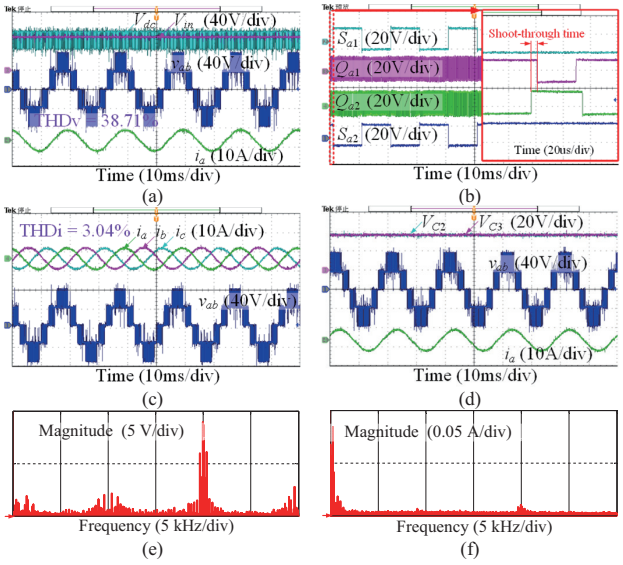

Fig. 14. Experimental results in boost mode. (m = 0.8 and d_f = 0.1). (a) DC power source voltage, input voltage of the HANPC TLI, phase A output currents and line voltage. (b) Drive signals of power switches. (c) Three-phase output currents and line voltage. (d) Voltages across dc-link capacitors, line voltage and phase A output currents. (e) Spectrum of line voltage. (f) Spectrum of output current.

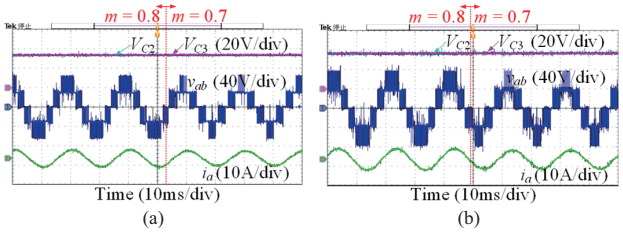

Fig. 15. Experimental waveforms of step change in the modulation index. (a) d_f = 0. (b) d_f = 0.1.

$$V_{dc} = V_{in} / (1 - 2d_f) = BV_{in} \tag{10}$$

Obviously, the boost function is realized. In boost mode, the driving signal of power switches are shown in Fig. 14(b), the injection of the shoot-through state does not add additional switching action, thereby preventing an increase in switching loss. Furthermore, the boost function is accomplished during the shoot-through time. It is noteworthy that within one sampling period, only one of the three phases has a shoot-through time, and the high frequency drive signals for the remaining two phases are similar to Fig. 13(b). Moreover, the voltages across C_2 and C_3 are balanced as well, as shown in Fig. 14(d). The spectra of v_{ab} and i_a are also provided in Fig. 14(e) and (f).

Fig. 15 depicts the experimental waveforms with the variation of the modulation index. Evidently, the magnitude of load current decreases when the modulation index is given as 0.7. Additionally, the excellent output current quality can be guaranteed.

To verify the NP voltage control capability of the proposed method in practical applications, the experimental conditions are configured to be consistent with the simulation conditions.

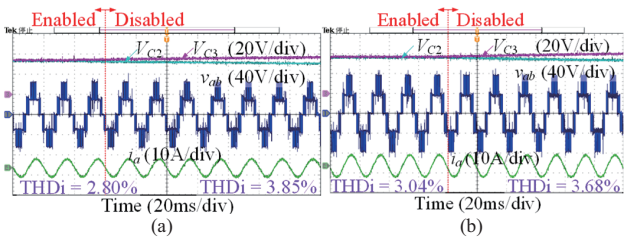

Fig. 16. Dynamic experimental waveforms of the NP voltage balance control. (a) m = 0.8, d_f = 0. (b) m = 0.8, d_f = 0.1.

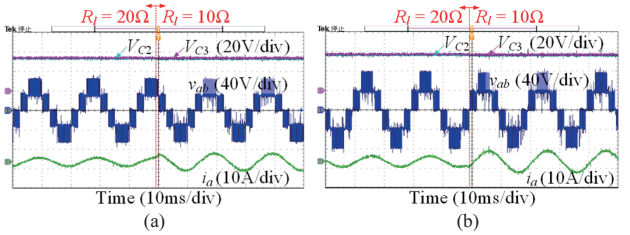

Fig. 17. Dynamic experimental waveforms with load changes. (a) m = 0.8, d_f = 0. (b) m = 0.8, d_f = 0.1.

As shown in Fig. 16, the transient waveforms are obtained in non-boost and boost modes. During the operation of the high-gain HANPC TLI, the NP voltage balance control is disabled by a button on the controller. The voltages across C_2 and C_3 are no longer balanced. The NP voltage imbalance causes current harmonics (specifically reflected in the THD), reduces output power quality, and even damages power switches. Therefore, it is essential to control the NP voltage balance while maintaining high output quality.

In order to more intuitively observe the effect of the NP voltage imbalance on the output current, the data for output current waveforms are stored by adopting the digital storage oscilloscope, and the THD of output current are subsequently obtained by using the MATLAB software. It can be seen that after the NP voltage separation, the current THD increases in both non-boost and boost modes.

Fig. 17 illustrates the dynamic output waveforms with load changes. The experimental results are consistent with the simulation results. With the decrease of load resistance, the output current magnitude is increased. Thus, the proposed method effectively ensures the normal operation under varying load conditions.

VII. Conclusion

This paper presents a novel high-gain HANPC TLI topology, which has the advantages of reduced cost and voltage boosting ability. Based on the characterization of the proposed topology, a hybrid frequency modulation scheme for the proposed topology is implemented. First, to achieve the balance of NP voltage and boosting function, a NP voltage distribution factor and shoot-through duty cycles were introduced. In addition, the switching sequences are designed separately, accordingly, the gate drive signals of the power devices are generated.

The hybrid frequency modulation is realized by the proposed modulation method, which further reduce the switching losses. In grid-tied photovoltaic (PV) systems, the high-gain HANPC TLI presents an alternative to traditional Si-based inverters. Furthermore, the proposed inverter topology can be applied in motor drives for electric vehicles and power supplies for modern data centers. To summarize, the proposed inverter has a wider voltage application range, regarding the capability to boost operation.

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