An Improved Finite Control Set Model Predictive Control Based on a Novel Dual-Port Three-Level Inverter

Guifeng WANG, Xin YUAN, Yunhui JIANG, Jianfei WANG, Fei WANG, and Zhan LIU

***Abstract*—In response to the high cost and large size issues associated with traditional back-to-back three-level inverters, this paper proposes a novel dual-port three-level inverter (DP-TLI) that simplifies the system structure through the utilization of switch multiplexing. Based on the proposed inverter topology, a time-sharing coordination finite control set model predictive control (TSC-FCS-MPC) strategy is developed. The strategy, grounded in the concept of time-sharing control, incorporates a coordinated approach within a two-cycle control loop. During the first cycle, the primary control objective is to optimize the output current of the upper port, with the selection of the optimal vector centered around this goal. Subsequently, the lower port's output is coordinated through control, leveraging the unique aspects of switch multiplexing and the redundancy in switch states inherent in the proposed topology. In the second cycle, the emphasis is reversed, with the optimization of the lower port's output current taking precedence, while the upper port is subjected to coordinated control. The implementation of this method significantly enhances the quality of the output current and the overall efficiency of the system. The viability and effectiveness of both the proposed topology and the control strategy are confirmed through simulation and experimental results.**

***Index Terms*—Dual-port; finite control set model predictive control (FCS-MPC); inverter; switch multiplexing; time-sharing coordination.**

I. Introduction

THE multiplexed dual-output inverter has demonstrated significant advantages over traditional back-to-back inverters, including a reduced number of switches, lower production costs, and a more compact size. This innovative technology has been successfully implemented in various applications, such as wind power generation systems [1]−[3], high-power traction systems [4]−[6], and unified power quality regulators [7]−[9].

The nine-switch converter (NSC) employs switch multiplexing to minimize the number of switches [7], enabling AC outputs at two ports [10]. However, this topology is constrained by several limitations, including higher voltage stress on the switches, fewer output levels, and increased harmonic generation. These drawbacks restrict its application in high-power and high-direct current voltage scenarios [11], [12].

Multi-level inverters offer distinct advantages over their two-level counterparts, including an increased number of output levels, enhanced output waveform quality, and reduced voltage stress and switching losses on the switches [13]. J. Haruna proposed a three-level twin drive inverter (TL-TDI), which produces two sets of three-phase AC outputs using 21 power switches [14]. However, this topology subjects the common switches to high voltage stress. Professor Wang Rutian's team at Northeast Electric Power University introduced a three-phase dual-output neutral point-clamped three-level inverter (DO-NPC-TLI), comprising 20 switches and 12 diodes. This design halves the voltage stress across all power switches to half of the DC link voltage. Nevertheless, the topology's inherent limitations prevent independent control of the upper and lower output ports [15]. The team also developed a novel dual-output T-type three-level inverter (DO-T-TLI), which integrates the T-type three-level topology with the NSC topology to control two independent loads. However, a larger number of switches in this design bear the full DC link voltage [16]. In [17], a five-leg, three-level dual-output inverter (5-leg, 3-level DOI) was proposed, based on two F-type inverters [18]. This design shares one phase leg between the two inverters, ensuring three-phase voltage outputs at both output ports and independent output for each phase.

Modulation strategies for multiplexed dual-output inverters primarily encompass carrier-based pulse width modulation (PWM) [19], [20], space vector modulation (SVM) [22]−[24], and finite control set model predictive control (FCS-MPC) [25]−[27]. FCS-MPC has garnered significant attention in power electronics research due to its simplicity in implementation, rapid dynamic response, and ease in achieving coordinated control of multiple objectives. In [28], FCS-MPC was first applied to NSC, utilizing the sum of the absolute values of current tracking errors at the upper and lower output ports as the cost function. However, this approach involves a substantial computational load due to 27 optimizations in each rolling step. To address the high ripple values in FCS-MPC for NSC generation drive applications, [29] proposed a duty cycle optimization decoupled predictive current control method. This approach reduces the computational load of the coupled section and achieves low-ripple technology for NSC generation. In [30], FCS-MPC was applied to a three-phase, three-level dual-output inverter, enabling output control at the dual output ports with different amplitudes, frequencies, and phase angles.

Manuscript received July 7, 2024; revised September 19, 2024 and October 29, 2024; accepted November 21, 2024. Date of publication December 30, 2024; date of current version November 26, 2024. This work was supported by Basic Research Program of Jiangsu Education Department under the Grant KYCX23_2913. *(Corresponding author: Fei Wang.)*

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Digital Object Identifier 10.24295/CPSSTPEA.2024.00027

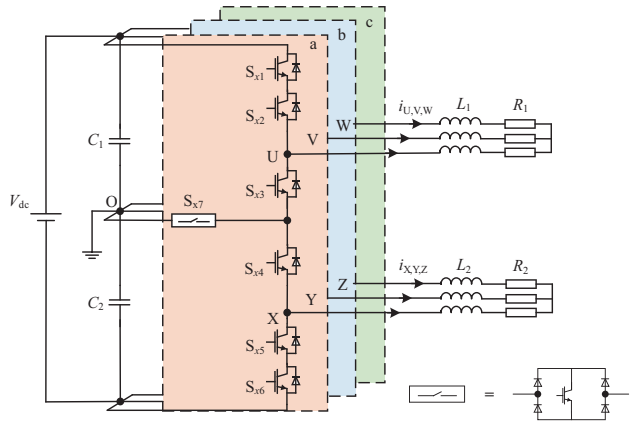


Fig. 1. Topology of DP-TLI.

This development laid the foundation for the subsequent advancement of FCS-MPC in three-level dual-output topologies.

This paper introduces a novel DP-TLI topology that simplifies the structure through switch multiplexing. Based on the characteristics of this topology, a time-sharing coordinated control finite control set model predictive control (TSC-FCS-MPC) method is proposed. This innovative approach enhances the quality of the output current and improves the overall efficiency of the system operation.

The structure of this paper is organized as follows: Initially, a comprehensive analysis of the DP-TLI topology and its operating principle is presented. Subsequently, the TSC-FCS-MPC strategy is introduced, which is tailored to the topology's characteristics. This strategy encompasses the establishment of current prediction models and cost functions for both upper and lower ports, the formulation of voltage vector selection rules, and the development of a time-sharing coordinated control mechanism. The efficacy of the proposed topology and control strategy is then validated through extensive simulations and experimental studies. This paper concludes with a summary of primary contributions and innovative aspects of this research.

II. DP-TLI Topology and Operating Principle

A. DP-TLI Topology

The proposed DP-TLI topology is illustrated in Fig. 1. The topology consists of three phases (a, b, and c), with each phase comprising six power switches, denoted as S_{xy}, where $x \in \{a, b, c\}$, $j \in \{1, 2, ..., 6\}$, and one bidirectional switch S_{x7} connects to the DC side. The output ports are connected to resistive-inductive loads, characterized by inductances L_1 and L_2, and resistances R_1 and R_2 for the upper and lower ports, respectively. The upper port's output phase voltages (v_{UO}, v_{VO}, and v_{WO}) are measured at nodes U, V, and W with respect to the midpoint O, with corresponding output load currents i_{UVW}. Similarly, the lower port's output phase voltages (v_{XO}, v_{YO}, and v_{ZO}) are measured at nodes X, Y, Z, with output load currents i_{XYZ}. The total DC link voltage is denoted as V_{dc}, with capacitors C_1 and C_2. In addition, it is noteworthy that the series connection of power switches S_{x1} and S_{x2}, S_{x5} and S_{x6} may present voltage unbalancing issues in practical applications, which is a limitation of this topology. While the primary focus of this paper is to analyze and verify the topology's feasibility using idealized switches, and future research will address the series equalization problem in detail.

TABLE I
Relationship Between Effective Switch State and Output Voltage

State	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a5}	S_{a6}	S_{a7}	v_{UO}	v_{XO}
1	1	1	1	1	0	0	0	P	P
2	1	1	0	1	1	0	1	P	O
3	1	1	0	0	1	1	1	P	N
4	0	1	1	1	1	0	1	O	O
5	0	1	1	0	1	1	1	O	N
6	0	0	1	1	1	1	0	N	N

B. Operating Principle

The topology's inherent constraints dictate that output pins can't be left floating and the DC bus mustn't be short-circuited. Consequently, 6 valid switching states are possible for the output, as delineated in Table I. In this representation, "1" indicates an ON switch, "0" indicates an OFF switch, while "P", "O", and "N" represent output voltages of $V_{dc}/2$, 0, and $-V_{dc}/2$, respectively. Owing to the symmetry of the three phases, phase a is used to illustrate the specific current flow paths for the six valid switching states, as depicted in Fig. 2. The upper output load current (i_U) flow path is indicated by red lines, while the lower output load current (i_X) flow path is denoted by blue lines. Analysis reveals that the topology imposes a constraint where the upper output voltage cannot be less than the lower output voltage.

C. Voltage Stress of Switches

An analysis of the voltage stress across each power switch is conducted based on the following assumptions:

(1) The voltage drop across simultaneously conducting power switches S_{a1} and S_{a2}, as well as S_{a5} and S_{a6}, is identical.

(2) The DC bus voltage remains constant. The maximum voltage stress across each switch is determined to be $V_{dc}/2$. A comparative analysis of the proposed topology with existing literature is presented in Table II. The proposed DP-TLI achieves dual-port output while reducing the number of switches, with all switches experiencing voltage stress equal to half of the DC link voltage. This configuration significantly reduces the system's size and cost.

III. TSC-FCS-MPC Method

A. Traditional FCS-MPC Operating Principle

1) Mathematical Modeling

The traditional FCS-MPC methodology comprises three primary components: prediction model, overall optimization,

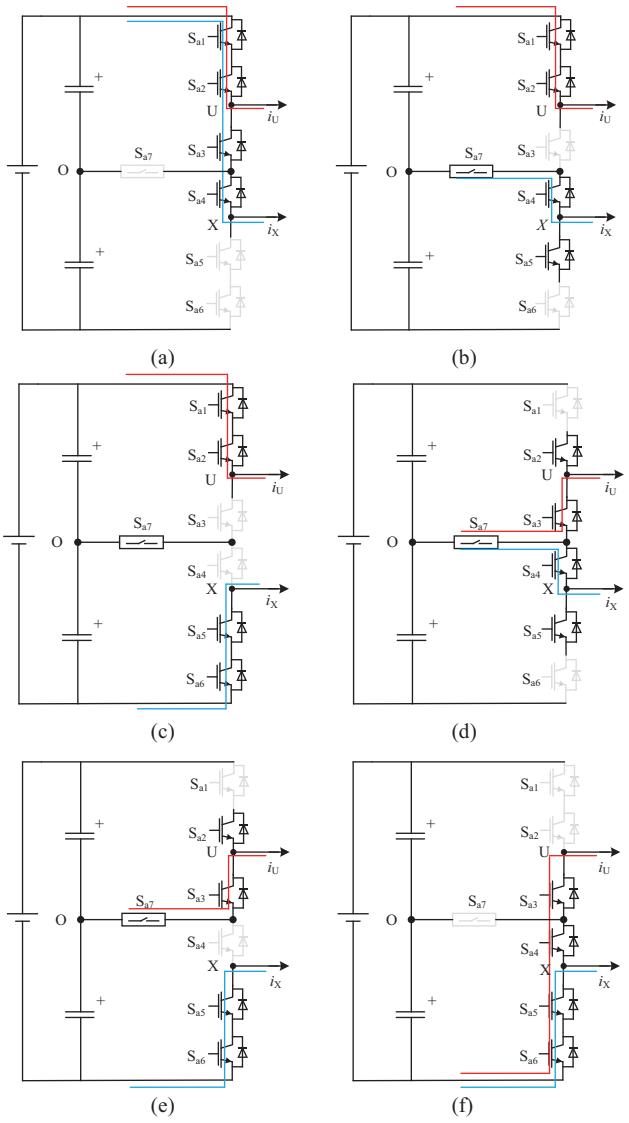


Fig. 2. Effective switch states of DP-TLI. (a) v_{UO}= P, v_{XO}= P. (b) v_{UO}= P, v_{XO}= O. (c) v_{UO}= P, v_{XO}= N. (d) v_{UO}= O, v_{XO}= O. (e) v_{UO}= O, v_{XO}= N. (f) v_{UO}= N, v_{XO}= N.

and feedback correction. Initially, based on the sampling value at time k and the established discretized mathematical model of the object, multiple possible output trajectories of the controlled object at time $(k + 1)$ are derived. Subsequently, a cost function is employed to optimize the desired target, determining the switch state that minimizes the error between the system's output at time $(k + 1)$ and the given value. Through continuous iteration of this process, overall system optimization is achieved. Fig. 3 illustrates the structure block diagram of the inverter FCS-MPC control system.

To model and analyze the proposed topology, the dynamic models of the upper and lower ports are represented as follows:

$$\begin{cases} v_{\mathrm{up}}(k) = i_{\mathrm{up}}(k)R_1 + L_1 \dfrac{\mathrm{d}i_{\mathrm{up}}(k)}{\mathrm{d}t} \\ v_{\mathrm{low}}(k) = i_{\mathrm{low}}(k)R_2 + L_2 \dfrac{\mathrm{d}i_{\mathrm{low}}(k)}{\mathrm{d}t} \end{cases} \tag{1}$$

where $v_{\mathrm{up}}(k)$ and $v_{\mathrm{low}}(k)$ denote the three-phase voltage output from the upper and lower ports at moment k, and $i_{\mathrm{up}}(k)$ and $i_{\mathrm{low}}(k)$ represent their corresponding output currents. The above equation is subjected to Clark transformation to obtain a simplified model of the inverter in the $\alpha\beta$ rotating coordinate system:

$$\begin{cases} v_{\mathrm{up}\alpha}(k) = i_{\mathrm{up}\alpha}(k)R_1 + L_1 \dfrac{\mathrm{d}i_{\mathrm{up}\alpha}(k)}{\mathrm{d}t} \\ v_{\mathrm{up}\beta}(k) = i_{\mathrm{up}\beta}(k)R_2 + L_2 \dfrac{\mathrm{d}i_{\mathrm{up}\beta}(k)}{\mathrm{d}t} \end{cases} \tag{2}$$

$$\begin{cases} v_{\mathrm{low}\alpha}(k) = i_{\mathrm{low}\alpha}(k)R_1 + L_1 \dfrac{\mathrm{d}i_{\mathrm{low}\alpha}(k)}{\mathrm{d}t} \\ v_{\mathrm{low}\beta}(k) = i_{\mathrm{low}\beta}(k)R_2 + L_2 \dfrac{\mathrm{d}i_{\mathrm{low}\beta}(k)}{\mathrm{d}t} \end{cases} \tag{3}$$

where T_s represents the sampling period, and $i_{\mathrm{up}\alpha,\beta}(k)$, $i_{\mathrm{low}\alpha,\beta}(k)$ denote the current values output from the two ports in the $\alpha\beta$ rotational coordinate system.

$$\begin{cases} i_{\mathrm{up}\alpha}(k+1) = (1 - \dfrac{R_1 T_s}{L_1}) i_{\mathrm{up}\alpha}(k) + \dfrac{T_s}{L_1} v_{\mathrm{up}\alpha}(k) \\ i_{\mathrm{up}\beta}(k+1) = (1 - \dfrac{R_1 T_s}{L_1}) i_{\mathrm{up}\beta}(k) + \dfrac{T_s}{L_1} v_{\mathrm{up}\beta}(k) \end{cases} \tag{4}$$

$$\begin{cases} i_{\mathrm{low}\alpha}(k+1) = (1 - \dfrac{R_2 T_s}{L_2}) i_{\mathrm{low}\alpha}(k) + \dfrac{T_s}{L_2} v_{\mathrm{low}\alpha}(k) \\ i_{\mathrm{low}\beta}(k+1) = (1 - \dfrac{R_2 T_s}{L_2}) i_{\mathrm{low}\beta}(k) + \dfrac{T_s}{L_2} v_{\mathrm{low}\beta}(k) \end{cases} \tag{5}$$

2) Establishment of the Value Function

Building upon the established mathematical model, with current constraint variables as target variables, a model predictive controller for the proposed inverter is developed. The traditional FCS-MPC strategy constructs a cost function based on the sum of the absolute values of the errors between the reference values and the predicted values of the dual-output load currents:

$$\begin{aligned} g = &\left| i^*_{\mathrm{up}\alpha}(k+1) - i_{\mathrm{up}\alpha}(k+1) \right| + \left| i^*_{\mathrm{up}\beta}(k+1) - i_{\mathrm{up}\beta}(k+1) \right| + \\ &\left| i^*_{\mathrm{low}\alpha}(k+1) - i_{\mathrm{low}\alpha}(k+1) \right| + \left| i^*_{\mathrm{low}\beta}(k+1) - i_{\mathrm{low}\beta}(k+1) \right| \end{aligned} \tag{6}$$

where $i^*_{\mathrm{up}\alpha,\beta}(k+1)$ and $i^*_{\mathrm{low}\alpha,\beta}(k+1)$ represent the reference values of upper and lower output currents at moment $(k+1)$.

With each phase having switch combinations as shown in Table I, the proposed inverter exhibits $6^3 = 216$ possible switching states. The controller must perform 216 optimizations within one control cycle to select the switching state that minimizes the cost function. This optimal state is then applied in the subsequent control instance to achieve optimal output control of the inverter. This method necessitates simultaneous consideration of the output effects of both upper and lower port currents, resulting in a substantial computational load for the controller within one control cycle.

TABLE II
COMPARISON OF VARIOUS TYPICAL DUAL-OUTPUT THREE-LEVEL CONVERTERS

Inverter	Number of				Maximum voltage stress
	Switches	Clamping diodes	Bidirectional switches	Active switch sstates of two ports	
Back to back converter	24	12	0	9	V_{dc}
TL-TDI	21	0	0	6	V_{dc}
FSI	15	6	0	4	V_{dc}
DO-NPC-TLI	20	12	0	6	V_{dc}
DO-T-TLI	12	0	3	6	V_{dc}
DP-TLI	18	0	3	6	$V_{dc}/2$

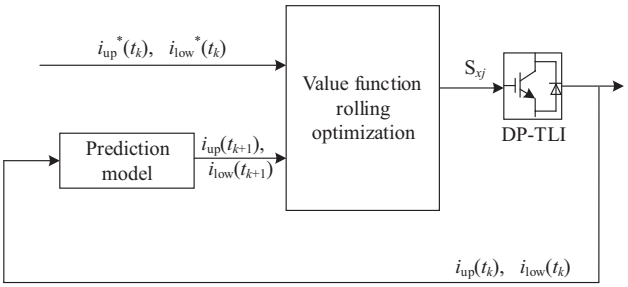


Fig. 3. Block diagram of the inverter FCS-MPC.

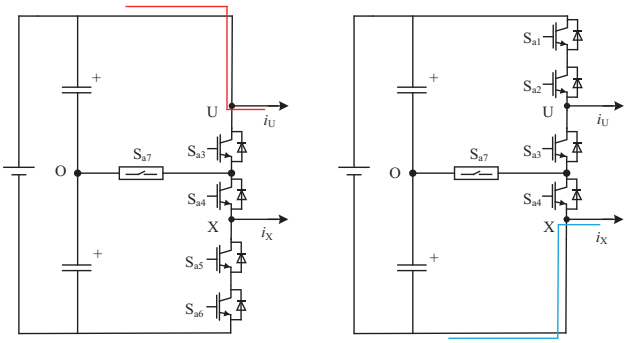


Fig. 4. Mode division of time-sharing work.

B. Time-Sharing Operating Principle

To reduce the controller's prediction operations and achieve independent control of the two ports in DP-TLI, a time-sharing finite control set model predictive control (TS-FCS-MPC) method is proposed. This method alternates between two operating modes: in the first control cycle (Mode 1), the lower port operates while the upper port remains at $+V_{dc}/2$; in the subsequent control cycle (Mode 2), the upper port operates while the lower port remains at $-V_{dc}/2$. These two cycles are continuously alternated for control. Fig. 4 illustrates the two operating modes for phase a, and Table III delineates the output states of the two ports.

The $(k+1)$ moment output currents of the upper and lower ports based on discrete time are represented by (4) and (5). Additionally, considering the dynamic model of the DC side capacitance, the capacitance current is expressed as:

TABLE III
RELATIONSHIP BETWEEN SWITCHING STATE AND OUTPUT VOLTAGE IN TS-FCS-MPC

Mode	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a5}	S_{a6}	S_{a7}	v_{UO}	v_{XO}
	1	1	0	0	1	1	1	P	N
Mode 1	0	1	1	0	1	1	1	O	N
	0	0	1	1	1	1	0	N	N
	1	1	1	1	0	0	0	P	P
Mode 2	1	1	0	1	1	0	1	P	O
	1	1	0	0	1	1	1	P	N

$$i_{C_n}(t) = C_n \frac{\mathrm{d}v_{C_n}}{\mathrm{d}t} \tag{7}$$

where $n \in \{1, 2\}$ and C_n idenotes the upper and lower bus capacitance value. Discretization is performed using the forward Euler method to obtain the discrete-time based DC side capacitance voltage:

$$v_{C_n}(k+1) = v_{C_n}(k) + \frac{T_s}{C_n} i_{C_n}(k) \tag{8}$$

The time-sharing control enables independent control of the upper and lower ports. Considering the DC bus midpoint balance, an additional term representing the midpoint potential difference is incorporated. The value function g_1 for the upper port is constructed as:

$$g_1 = \left|i_{up\alpha}^*(k+1) - i_{up\alpha}(k+1)\right| + \left|i_{up\beta}^*(k+1) - i_{up\beta}(k+1)\right| + \lambda\left|v_{C1}(k+1) - v_{C2}(k+1)\right| \tag{9}$$

Similarly, the value function g_2 for the lower port is formulated as:

$$g_2 = \left|i_{low\alpha}^*(k+1) - i_{low\alpha}(k+1)\right| + \left|i_{low\beta}^*(k+1) - i_{low\beta}(k+1)\right| + \lambda\left|v_{C1}(k+1) - v_{C2}(k+1)\right| \tag{10}$$

where λ represents a weight coefficient that determines the priority of the controlled variable in the global optimization. Utilizing time-sharing control method, only one port operates in each control cycle, The controller performs 27 optimization searches within one cycle.

C. TSC-FCS-MPC Operating Principle

The time-sharing nature of the operation, wherein simultaneous current output control for both ports is not feasible, results in a relatively low utilization rate of the DC voltage. To address this limitation, a coordinated control approach has been implemented. This approach involves the establishment of predictive models and cost functions for both the upper and lower ports. Within a single control cycle, the optimal output current for one port (upper or lower) is determined initially. Subsequently, based on the principles of time-sharing coordinated control, the optimal output current for the other port is established within the effective vector range. In the following control cycle, this process is reversed, with the previously secondary port taking priority. This alternating operation over two cycles facilitates the coordinated functioning of both ports.

The TSC-FCS-MPC methodology constructs value function g_1 for the upper port:

$$g_1 = \left|i^*_{\mathrm{up}\alpha}(k+1) - i_{\mathrm{up}\alpha}(k+1)\right| + \left|i^*_{\mathrm{up}\beta}(k+1) - i_{\mathrm{up}\beta}(k+1)\right| \quad (11)$$

Similarly, the TSC-FCS-MPC methodology constructs the value function g_2 for the lower port:

$$g_2 = \left|i^*_{\mathrm{low}\alpha}(k+1) - i_{\mathrm{low}\alpha}(k+1)\right| + \left|i^*_{\mathrm{low}\beta}(k+1) - i_{\mathrm{low}\beta}(k+1)\right| \quad (12)$$

1) Vector Selection Principle Based on TSC-FCS-MPC

The output three-phase voltage vectors for the upper and lower ports are defined as $\boldsymbol{v}_{\mathrm{up}} = [v_{\mathrm{U}} v_{\mathrm{V}} v_{\mathrm{W}}]$ and $\boldsymbol{v}_{\mathrm{low}} = [v_{\mathrm{X}} v_{\mathrm{Y}} v_{\mathrm{Z}}]$.

In contrast to traditional methods, when determining the three-phase voltage vector of one port at a given moment, the vector of the other port is not unique. The three-phase voltage vector can be selected as the optimal output state when constraints are satisfied. For instance, when the upper port outputs $\boldsymbol{v}_{\mathrm{up}}$ = [PON], the lower port can select from six states: [PON], [PNN], [OON], [ONN], [NON], and [NNN], all of which satisfy the topology's inherent constraints. Fig. 5 illustrates the vector selection principle for $\boldsymbol{v}_{\mathrm{up}}$ = [PON]. When the upper port's output state is P, the corresponding voltage states of the lower port can be P, O, or N. When the upper port's voltage state is O, the lower port's output states are limited to O and N due to topological constraints. When the upper port's voltage state is N, the lower port's output state is restricted to N. Based on this principle, Fig. 5 depicts the effective switching states of vlow when $\boldsymbol{v}_{\mathrm{up}}$ = [PON]. The effective states are summarized as [PON], [PNN], [OON], [ONN], [NON], and [NNN]. Consequently, the effective voltage vectors for the lower port corresponding to each upper port voltage vector can be derived, as shown in Table IV.

2) TSC-FCS-MPC System

The time-sharing cooperative control operates cyclically over two control cycles. In one cycle, the upper port operates as the primary component while the lower port operates cooperatively. In the subsequent cycle, these roles are reversed.

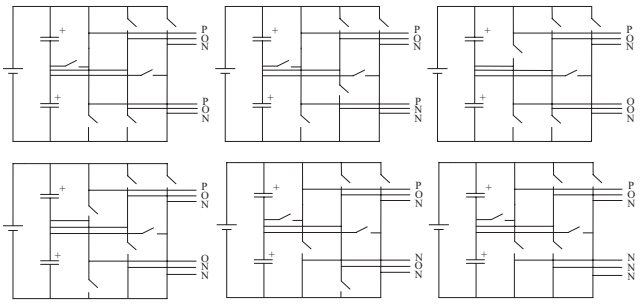


Fig. 5 Three-phase effective switching of the topology when $\boldsymbol{v}_{\mathrm{up}}$ = [PON] states.

When the upper port is the primary component, the controller performs a 27-voltage vector rolling optimization for its output current value function g_1. The voltage vector yielding the smallest value function is selected. After obtaining this optimal voltage vector, the controller performs a rolling optimization for the lower port's output current value function g_2 based on the corresponding effective voltage vectors listed in Table III. The optimal voltage vector for the lower port is then selected. Finally, a digital signal is generated according to the switching states of the power switches corresponding to the output voltages of both ports, as outlined in Table I. The process is mirrored when the lower port operates as the primary component. After selecting the optimal voltage vector for g_2 through rolling optimization, the effective voltage vector for the upper port is chosen, followed by a rolling optimization to select the optimal vector for g_1. Fig. 6 presents a flowchart of the main operations of the TSC-FCS-MPC system when the upper port is the primary component. Fig. 7 illustrates the overall control block diagram of the system.

This method ensures prioritized operation of one port in each control cycle, with the other port operating cooperatively according to topology switch multiplexing and switch state redundancy. The alternating priority over two cycles reduces the number of optimization searches from 216 to 27−54 per control cycle, significantly enhancing computational efficiency.

IV. Simulation and Experimental Validation

A. Simulation Results and Analysis

Simulation studies were conducted using MATLAB/Simulink software to validate the effectiveness of the proposed TSC-FCS-MPC. The simulation parameters were set as follows: V_{dc} = 600 V, T_{s} = 80 μs. The results of conventional FCS-MPC and TS-FCS-MPC were provided for comparison.

The operating modes of the inverter were categorized into two groups: common frequency (CF) mode and different frequency (DF) mode. In CF mode, the operating frequencies of two three-phase outputs are equal, while in DF mode, they differ.

For CF mode, the following parameters were utilized: $i_{\mathrm{up}}{}^*$ and $i_{\mathrm{low}}{}^*$ reference currents of 10 A, frequencies $f_1 = f_2$ = 50 Hz, load

TABLE IV
THE LOWER PORT EFFECTIVE VOLTAGE VECTOR CORRESPONDING TO THE UPPER PORT VOLTAGE VECTOR

$\boldsymbol{v}_{up}$	Effective vector corresponding to $\boldsymbol{v}_{low}$
PPP	PPP PPO PPN POP POO PON PNP PNO PNN OPP OPO OPN OOP OOO OON ONP ONO ONN NPP NPO NPN NOP NOO NON NNP NNO NNN
PPO	PPO PPN POO PON PNO PNN OPO OPN OOO OON ONO ONN NPO NPN NOO NON NNO NNN
PPN	PPN PON PNN OPN OON ONN NPN NON NNN
POP	POP POO PON PNP PNO PNN OOP OOO OON ONP ONO ONN NOP NOO NON NNP NNO NNN
POO	POO PON PNO PNN OOO OON ONO ONN NOO NON NNO NNN
PON	PON PNN OON ONN NON NNN
PNP	PNP PNO PNN ONP ONO ONN NNP NNO NNN
PNO	PNO PNN ONO ONN NNO NNN
PNN	PNN ONN NNN
OPP	OPP OPO OPN OOP OOO OON ONP ONO ONN NPP NPO NPN NOP NOO NON NNP NNO NNN
OPO	OPO OPN OOO OON ONO ONN NPO NPN NOO NON NNO NNN
OPN	OPN OON ONN NPN NON NNN
OOP	OOP OOO OON ONP ONO ONN NOP NOO NON NNP NNO NNN
OOO	OOO OON ONO ONN NOO NON NNO NNN
OON	OON ONN NON NNN
ONP	ONP ONO ONN NNP NNO NNN
ONO	ONO ONN NNO NNN
ONN	ONN NNN
NPP	NPP NPO NPN NOP NOO NON NNP NNO NNN
NPO	NPO NPN NOO NON NNO NNN
NPN	NPN NON NNN
NOP	NOP NOO NON NNP NNO NNN
NOO	NOO NON NNO NNN
NON	NON NNN
NNP	NNP NNO NNN
NNO	NNO NNN
NNN	NNN

resistors $R_1 = R_2 = 10\ \Omega$, and inductors are $L_1 = L_2 = 15$ mH. Fig. 8 displays the output current waveforms and their total harmonic distortion (THD) for both ports, obtained using the three strategies.

The output currents i_{UVW}, i_{XYZ} and their THDs for the upper and lower ports based on conventional FCS-MPC are presented in Fig. 8(a) and (b). The current waveforms exhibit stable sinusoidal patterns with THDs of 2.71% and 2.73%, respectively. Fig. 8(c) and (d) illustrates i_{UVW}, i_{XYZ} and their THDs for conventional TS-FCS-MPC, showing stable sinusoidal waveforms with THDs of 2.31% and 1.91%. i_{UVW}, i_{XYZ} and their THDs of the upper and lower ports based on the conventional TSC-FCS-MPC are depicted in Fig. 8(e) and (f), demonstrating stable sinusoidal waveforms with THDs of 1.92% and 1.66%. In CF mode, the THDs obtained by all three control methods comply with the national standard, which stipulates that the THD of load current in the public grid should not exceed 5%. Notably, the proposed strategy achieves higher current quality and lower THD values compared to the previous two methods.

For DF mode, the parameters were set as follows: i_{up}^* and i_{low}^* reference currents of 10 A, $f_1 = 50$ Hz, $f_2 = 60$ Hz, $R_1 = R_2 = 10\ \Omega$, and $L_1 = L_2 = 15$ mH. Fig. 9 presents the output current waveforms and their THDs for both ports, obtained using the three strategies. Fig. 10 displays the output waveforms of voltages v_{UVW} and v_{XYZ}, showing sinusoidal patterns with an amplitude of 100 V for each phase.

The output wrrents i_{UVW}, i_{XYZ} and their THDs for the upper and lower ports based on the proposed TSC-FCS-MPC are shown in Fig. 9(a) and (b). The current waveforms exhibit stable sinusoidal patterns with THDs of 1.93% and 1.45%, respectively. Table V provides a comparison of current THDs obtained with the other two methods. In conclusion, the THDs obtained by all three control methods in DF mode meet the national grid standards. The proposed strategy demonstrates superior performance, achieving lower THD values and higher quality currents compared to the two previous methods.

For the time-sharing operation, the following parameters were employed: voltage $V_{dc} = 600$ V, $C_1 = C_2 = 3\ 600$ μF, resistive inductive load $R_1 = R_2 = 10\ \Omega$, $L_1 = L_2 = 15$ mH, and $\lambda = 2$. Fig. 11 illustrates the voltages of the capacitors. The voltages v_{C1} and v_{C2} on C_1 and C_2 are presented in Fig. 11(a) and (b), respectively. Both voltages stabilize at approximately 300 V, with their difference maintained within ±0.05 V, demonstrating balanced capacitor voltages.

The predictive current control method's efficacy is highly dependent on the accuracy of inductor parameters, as evidenced by (4) and (5). The control circuit necessitates direct incorporation of inductor parameters in calculations, and its performance is contingent upon the degree of congruence between the control circuit's inductor parameters and those of the main circuit. Dis-

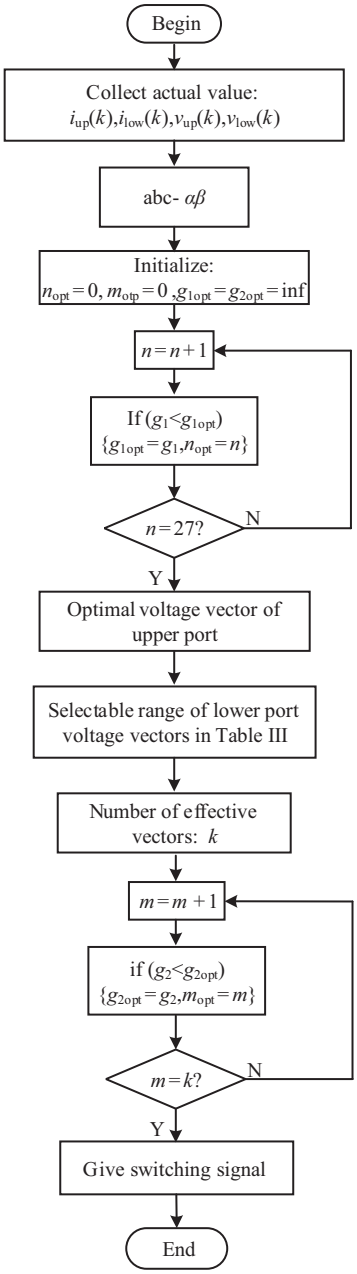


Fig. 6. Flow diagram of inverter 1 as main component based on time-sharing cooperative control.

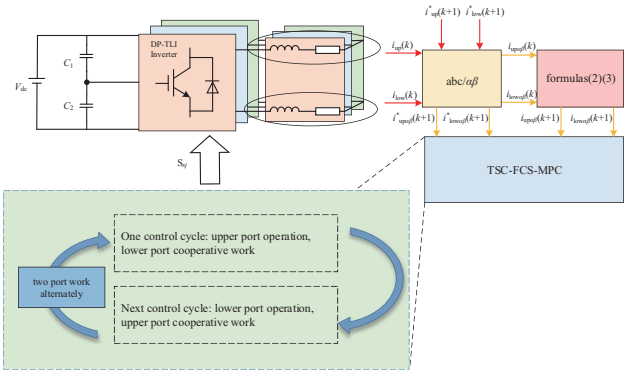


Fig. 7. Control block diagram of the proposed time-sharing cooperative control.

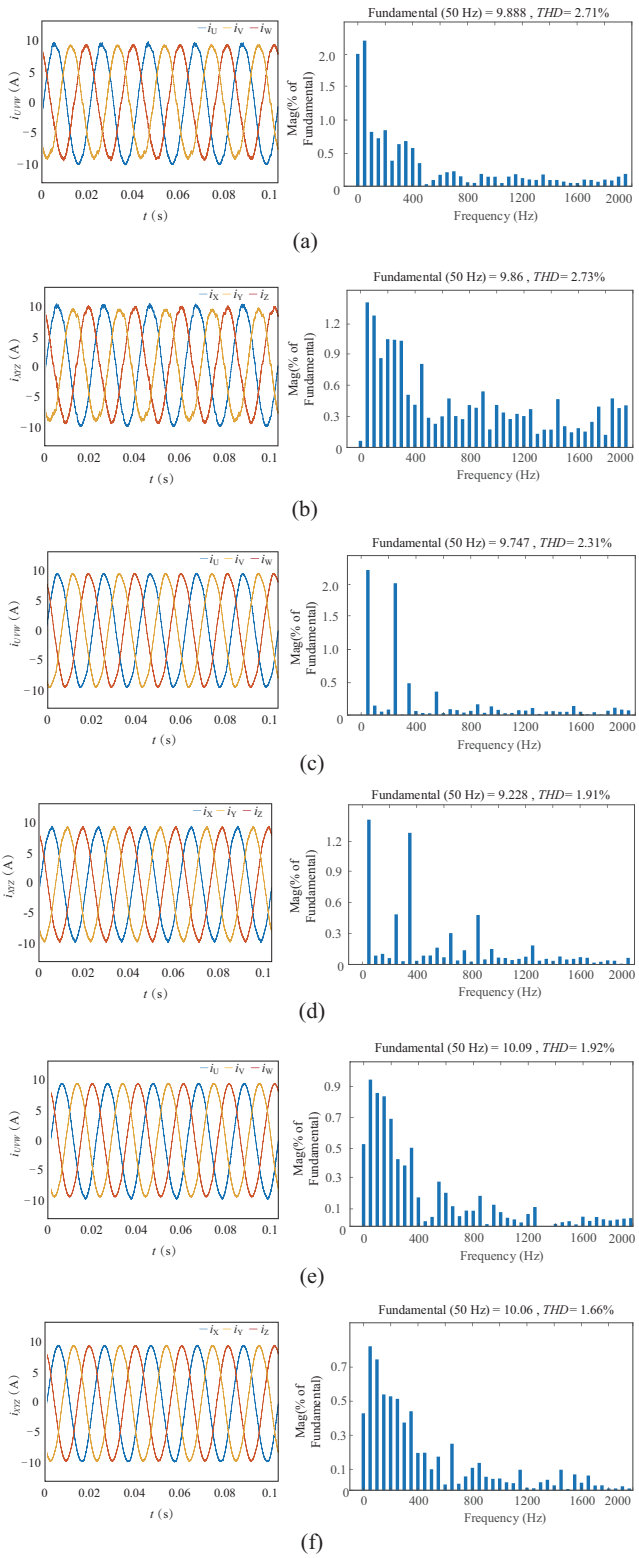


Fig. 8. Output current and its THD in CF mode. (a)i_{UVW} and its THD of FCS-MPC. (b) i_{XYZ} and its THD of FCS-MPC. (c) i_{UVW} and its THD of TS-FCS-MPC. (d) i_{XYZ} and its THD of TS-FCS-MPC. (e) i_{UVW} and its THD of TSC-FCS-MPC. (f) i_{XYZ} and its THD of TSC-FCS-MPC.

crepancies between the resistive-inductive parameters of the control and main circuits can lead to inaccurate output current values and ineffective reference current tracking. Consequent-

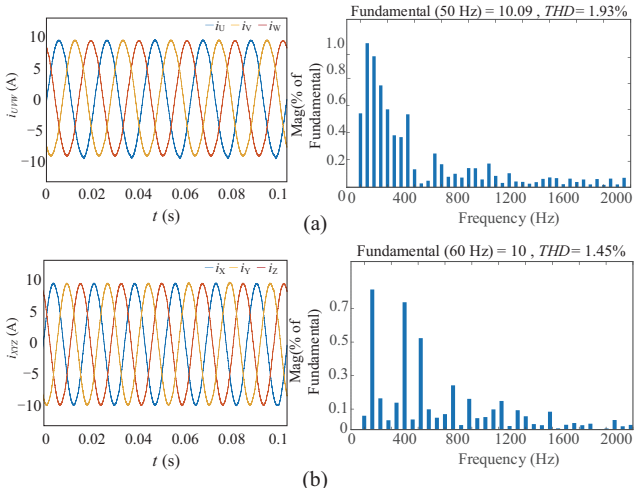


Fig. 9. Output current and its THD in DF mode. (a) i_{UVW} and its THD of TSC-FCS-MPC. (b) i_{XYZ} and its THD of TSC-FCS-MPC.

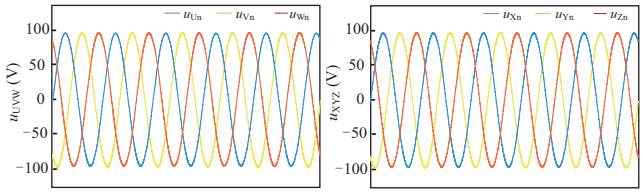


Fig. 10. The output waveforms of voltages v_{UVW} and v_{XYZ} of TSC-FCS-MPC.

TABLE V
THD COMPARISON OF DIFFERENT ALGORITHMS IN DF MODE

Strategy	THD of different port current/%	
	Upper	Lower
FCS-MPC	2.56	2.67
TS-FCS-MPC	2.32	1.90
TSC-FCS-MPC	1.93	1.45

ly, this mismatch may result in diminished system response, reduced stability, and potential oscillations.

An analysis was conducted to evaluate the system's control capability under parameter incompatibility. Parameter errors of ±60% were introduced, with resistance values ranging from 4–16 Ω and inductance values from 6–24 mH. Fig. 12 presents a comparative analysis of the THD for the upper port currents using the three methods at various parameter values. Similarly, Fig. 13 illustrates the THD of the lower port currents for the three methods across different parameter values.

As depicted in Figs. 12 and 13, the output current THD for both traditional FCS-MPC and TS-FCS-MPC methods exhibits higher values at 60% parameter error, exceeding the 5% threshold permitted by national public grid standards. In contrast, the proposed TSC-FCS-MPC method demonstrates consistently lower THD values, all below 5%, thereby adhering to the national standards for permissible load current THD in public grids. This method maintains superior overall current quality, ensuring that system stability remains unaffected by parameter mismatches.

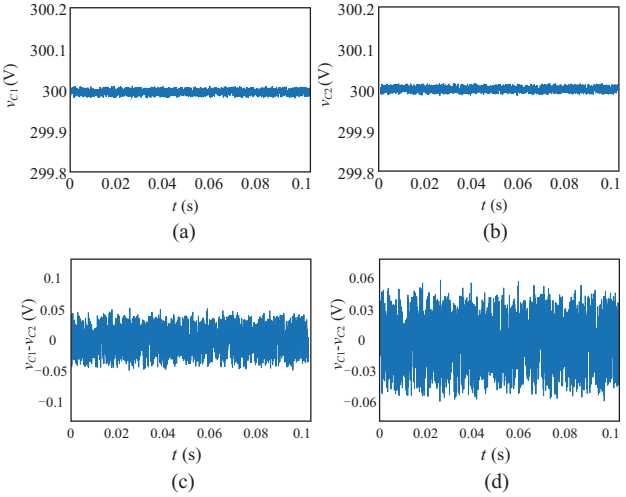


Fig. 11. Waveforms of the DC-link capacitor voltages. (a) C_1. (b) C_2. (c)v_{C1}–v_{C2}. (d) Local zoom of v_{C1}–v_{C2}.

B. Experimental Validation

To substantiate the viability of the proposed topology and strategy, a hardware-in-the-loop testing platform was constructed based on the experimental setup illustrated in Fig. 14. The main circuit was implemented in the TyphoonHIL 402 semi-physical platform, with pulse signals generated by an HDSP-DF28335P real-time controller. Voltage and current harmonic distortion rates were analyzed using a HIOKI power quality analyzer PQ3198. The experimental parameters were configured to match those used in the simulation.

1) In CF Mode

Fig. 15 presents the three-phase output current waveforms for the upper and lower ports, comparing the three strategies: conventional FCS-MPC, TS-FCS-MPC, and TSC-FCS-MPC in CF mode. The corresponding THD values for these currents are displayed in Fig. 16.

The experimental results depicted in Figs. 15 and 16 demonstrate that the output three-phase currents at both the upper and lower ports exhibit stable sinusoidal waveforms in CF mode for all three control strategies. The THD values of these currents are consistently below 5%. Notably, the proposed control strategy yields superior current quality compared to the two preceding methods, aligning with the simulation outcomes.

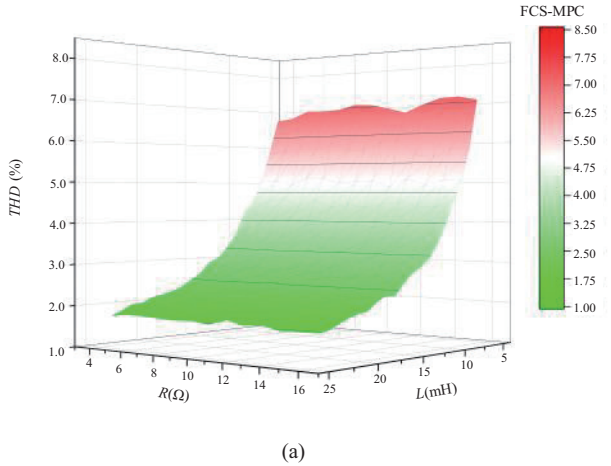
2) In DF Mode

Fig. 17 illustrates the three-phase output current waveforms for the upper and lower ports, comparing the conventional FCS-MPC, TS-FCS-MPC, and TSC-FCS-MPC strategies in DF mode. The corresponding THD values for these currents are presented in Fig. 18.

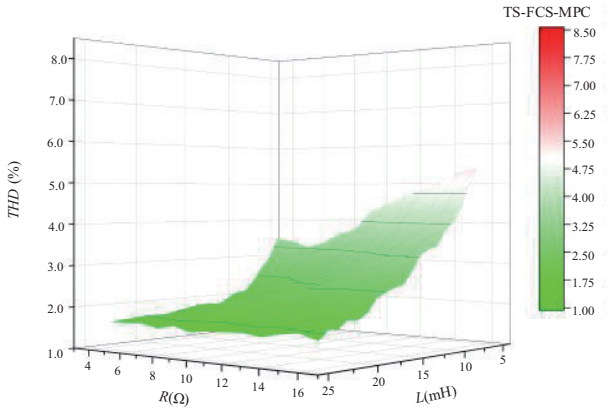
As evidenced by Figs. 17 and 18, the proposed control strategy demonstrates overall superior performance in DF mode compared to both the conventional FCS-MPC and time-sharing control methods. These findings corroborate the simulation results.

3) Dynamic Performance

To further assess the dynamic performance, a reference



(a)



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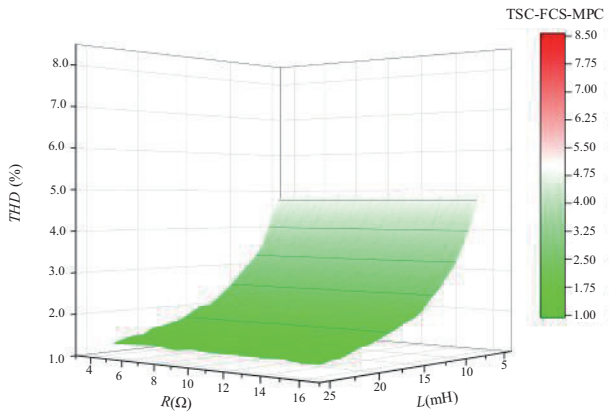
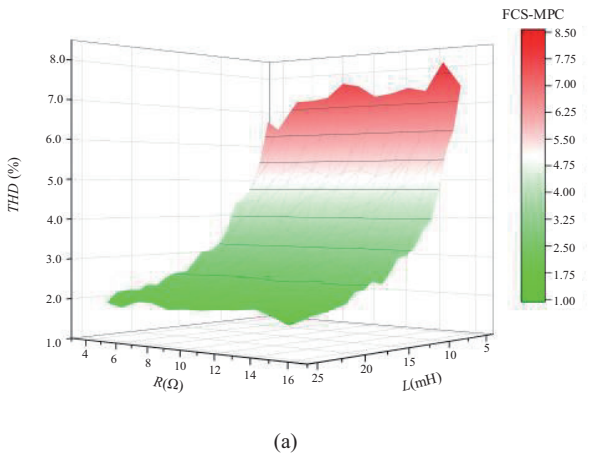
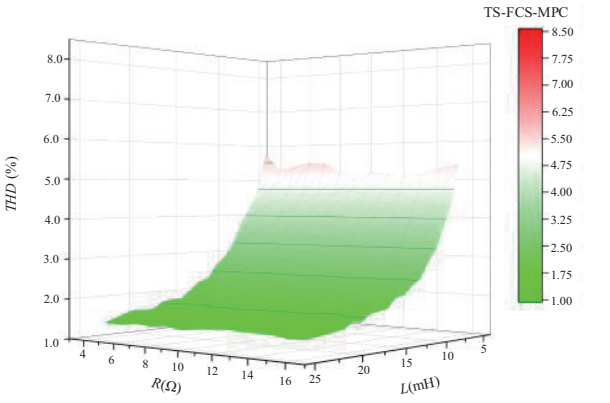


(c)

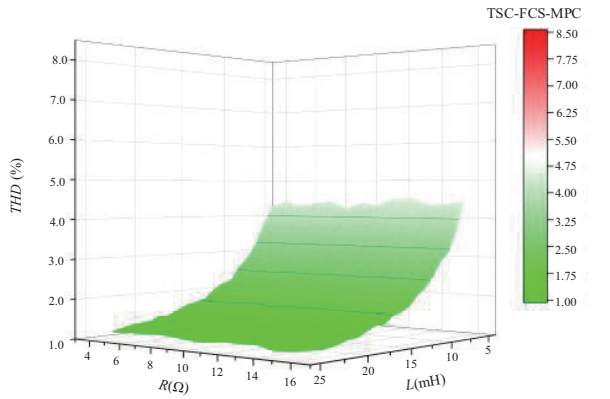
Fig. 12. THD of the upper output port current for different parameters (a) FCS-MPC. (b) TS-FCS-MPC. (c) TSC-FCS-MPC.



(a)



(b)



(c)

Fig. 13. THD of the lower output port current for different parameters. (a) FCS-MPC. (b) TS-FCS-MPC. (c) TSC-FCS-MPC.

current frequency of $f_1 = f_2 = 50$ Hz was applied to i_{up}^* and i_{low}^* in CF mode. Subsequently, the amplitude of i_{up}^* was abruptly altered from 10 A to 15 A. Fig. 19 illustrates the dynamic responses of the three control strategies under these conditions.

Fig. 19 reveals that when the upper port reference current is modified, the dynamic switching times for the upper port output current in CF mode are 1.634, 1.205, and 0.933 ms for the conventional FCS-MPC, TS-FCS-MPC, and TSC-FCS-MPC strategies, respectively. All three control strategies demonstrate rapid current stabilization and good dynamic performance. Notably, the TSC-FCS-MPC strategy achieves the shortest stabilization time for the three-phase output current of the upper port, indicating a faster dynamic response.

To validate the efficacy of the proposed control method in

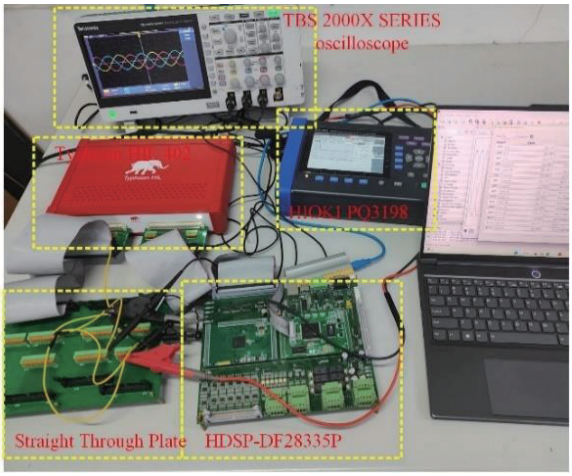


Fig. 14. Hardware-in-the-loop experimental platform.

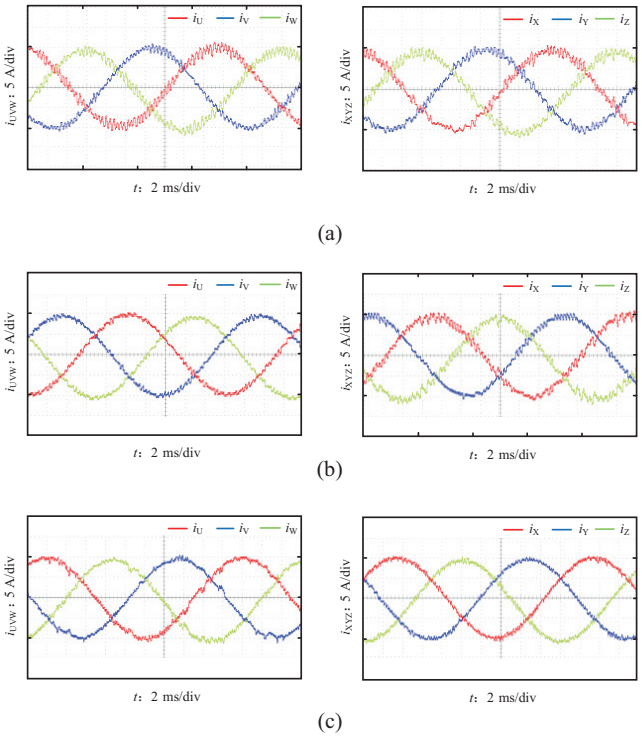


Fig. 15. Experimental waveforms of output current in CF. (a)FCS-MPC. (b)TS-FCS-MPC. (c)TSC-FCS-MPC.

reducing computational burden, the predicted operation times of the three control methods were compared, as shown in Fig. 20. The conventional FCS-MPC strategy requires a prediction operation time of 62.88 μs, constituting 78.6% of the control cycle time. The TS-FCS-MPC strategy necessitates 26.96 μs, accounting for 33.7% of the control cycle time. The TSC-FCS-MPC strategy requires 32.72 μs, representing 40.9% of the control cycle time. This represents a 48% reduction in computing time compared to the conventional FCS-MPC. Although the number of optimization searches per control cycle is increased compared to the TS-FCS-MPC, resulting in a 5.76 μs increase in computing time, these findings align with the theoretical analysis.

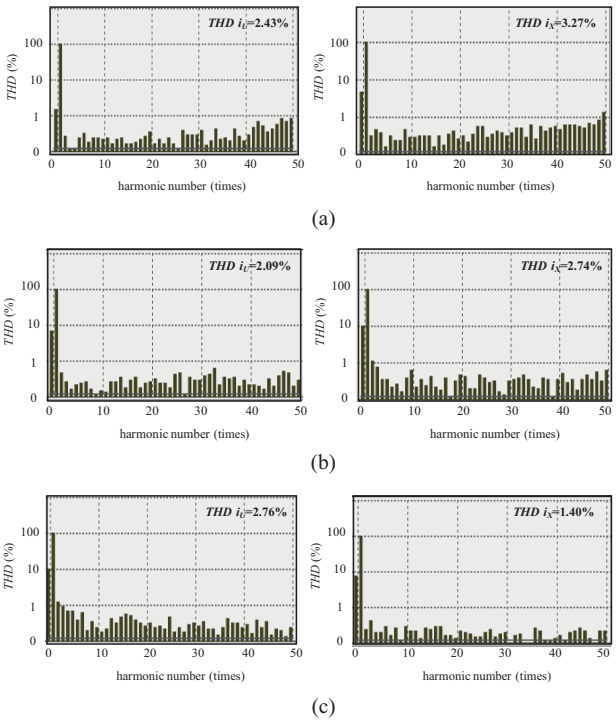


Fig. 16. THD of output current in CF. (a)FCS-MPC. (b)TS-FCS-MPC. (c)TSC-FCS-MPC.

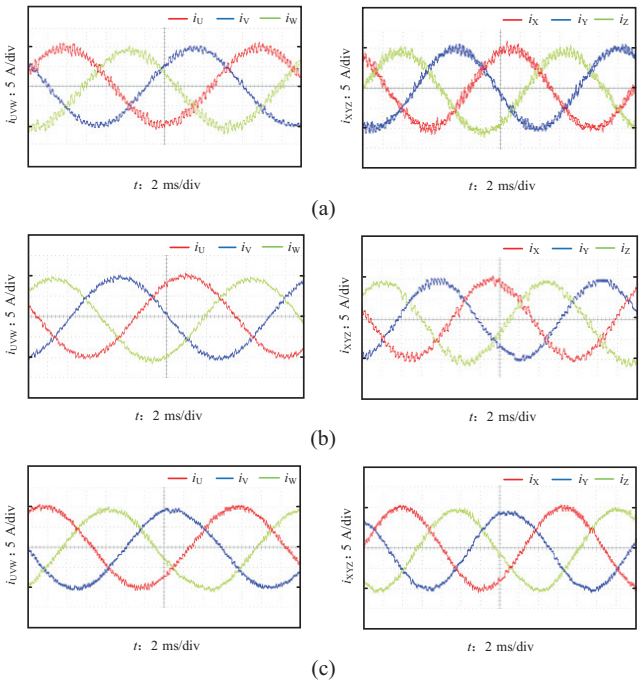


Fig. 17. Experimental waveforms of output current in DF. (a)FCS-MPC, (b) TS-FCS-MPC and (c)TSC-FCS-MPC.

In conclusion, the proposed TSC-FCS-MPC strategy demonstrates superior output current waveform quality, enhanced dynamic stability, and reduced prediction arithmetic compared to the traditional FCS-MPC. These improvements result in enhanced system response speed and stability. Furthermore, when compared to the TS-FCS-MPC, the TSC-FCS-MPC achieves

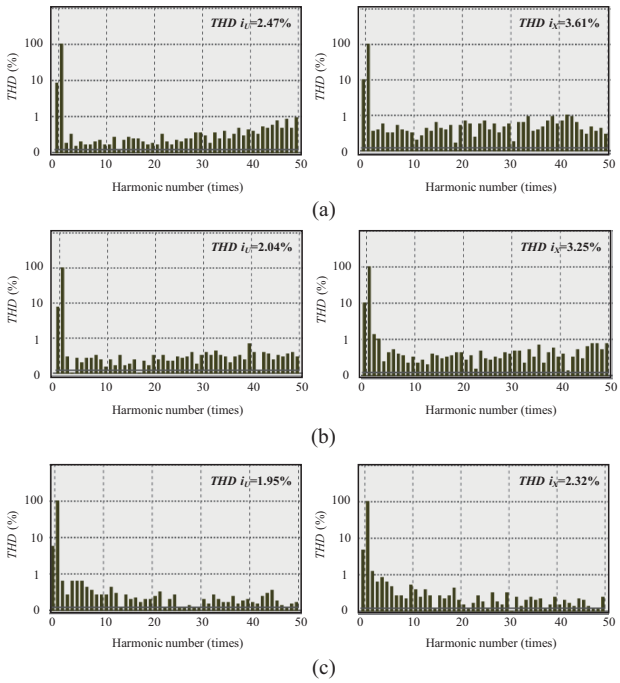


Fig. 18. THD of output current in DF. (a)FCS-MPC, (b)TS-FCS-MPC and (c) TSC-FCS-MPC.

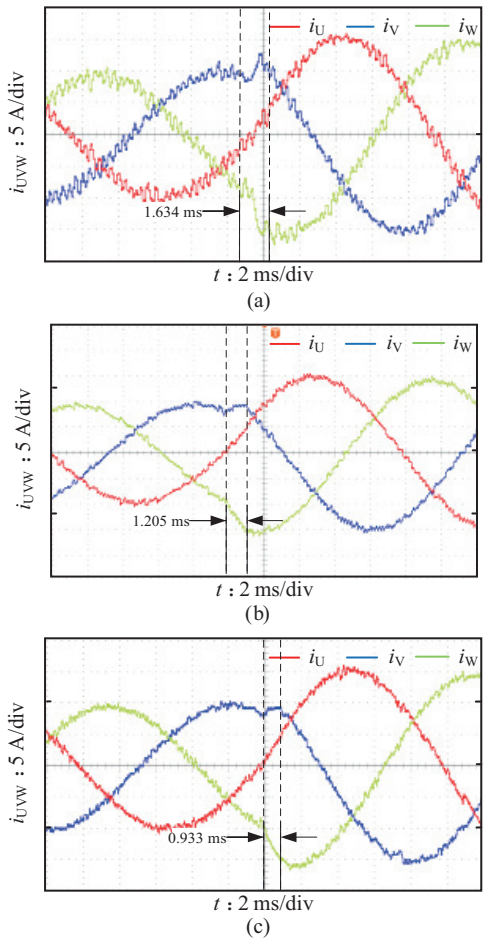


Fig. 19. Dynamic performance in CF. (a)FCS-MPC. (b)TS-FCS-MPC. (c)TSC-FCS-MPC.

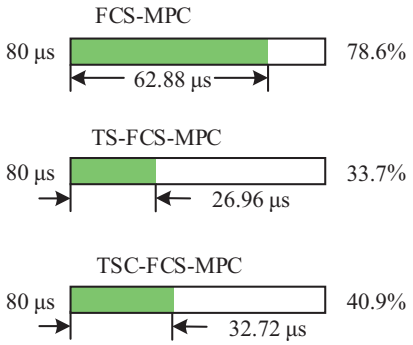


Fig. 20. Predictive operation time. (a)FCS-MPC. (b)TS-FCS-MPC. (c)TSC-FCS-MPC.

coordinated operation of the upper and lower output ports, thereby enhancing the overall output performance of both ports.

V. Conclusion

A novel DP-TLI topology has been proposed in this paper, which simplifies the structure through switch multiplexing, thereby reducing system costs. To complement this topology, a TSC-FCS-MPC strategy has been introduced. This strategy incorporates coordinated control on top of time-sharing control, treating two control cycles as a single loop. Consequently, the coordinated operation of both ports is enabled, fully utilizing the redundancy in switch states offered by the device multiplexing of the proposed topology. This approach significantly enhances the overall output performance of the inverter. Furthermore, the prediction computation has been substantially reduced from the traditional exhaustive optimization method of 216 iterations to a mere 27 to 54 iterations. This reduction markedly improves the system's operational efficiency and response speed. The effectiveness of the proposed topology and control strategy has been rigorously validated through both simulation and experimental results.

References

[1] S. Ye, D. Zhou, X. Yao, and F. Blaabjerg, "Component-level reliability assessment of a direct-drive PMSG wind power converter considering two terms of thermal cycles and the parameter sensitivity analysis," in *IEEE Transactions on Power Electronics*, vol. 36, no. 9, pp. 10037–10050, Sept. 2021.

[2] H. Chen, D. Xu, and X. Deng, "Control for power converter of small-scale switched reluctance wind power generator," in *IEEE Transactions on Industrial Electronics*, vol. 68, no. 4, pp. 3148–3158, Apr. 2021.

[3] X. Peng, Z. Liu, and D. Jiang, "A review of multiphase energy conversion in wind power generation," in *Renewable and Sustainable Energy Reviews*, vol. 147, pp. 111172, 2021.

[4] S. Bhattacharya, D. Mascarella, G. Joós, J. -M. Cyr, and J. Xu, "A dual three-level T-NPC inverter for high-power traction applications," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 2, pp. 668–678, Jun. 2016.

[5] E. Yolacan, M. K. Guven, M. Aydin, and A. M. El-Refaie, "Modeling and experimental verification of an unconventional 9-phase asymmetric winding PM motor dedicated to electric traction applications," in *IEEE Access*, vol. 8, pp. 70182–70192, 2020.

[6] S. Wu, M. Wu, and Y. Wang, "A novel co-phase power-supply system based on modular multilevel converter for high-speed railway AT traction

power-supply system," in *Energies*, vol. 14, no. 1, pp. 253, 2021.
[7] S. K. Yadav, A. Patel, and H. D. Mathur, "Study on comparison of power losses between UPQC and UPQC-DG," in *IEEE Transactions on Industry Applications*, vol. 58, no. 6, pp. 7384–7395, Nov.-Dec. 2022.
[8] L. Meng, L. Ma, W. Zhu, H. Yan, T. Wang, W. Mao, X. He, and Z. Shu, "Control strategy of single-phase UPQC for suppressing the influences of low-frequency DC-link voltage ripple," in *IEEE Transactions on Power Electronics*, vol. 37, no. 2, pp. 2113–2124, Feb. 2022.
[9] D. Li, T. Wang, W. Pan, X. Ding, and J. Gong, "A comprehensive review of improving power quality using active power filters," in *Electric Power Systems Research*, vol. 199, pp. 107389, 2021.
[10] T. Kominami and Y. Fujimoto, "A novel nine-switch inverter for independent control of two three-phase loads," in *Proceedings of 2007 IEEE Industry Applications Annual Meeting,* New Orleans, LA, USA, 2007, pp. 2346–2350.
[11] P. Wang, H. Xu, and L. Yuan, "Research on cascaded multilevel converters for dual motor drive systems based on a nine switch converter," in *IET Electric Power Applications*,vol. 18, no. 8, pp. 849–858, 2024.
[12] Y. Pang, J. Zhang, D. Xu, and C. Yin, "Model predictive control of nine-switch converter with output filter for independent control of two loads," in *Journal of Power Electronics*, vol. 21, pp. 224–234,2021.
[13] G. K. Srinivasan, M. Rivera, V. Loganathan, D. Ravikumar, and B. Mohan, "Trends and challenges in multi-level inverter with reduced switches," in *Electronics*, vol. 10, no. 4, pp. 368, 2021.
[14] J. Haruna and N. Hoshi, "A novel three-level inverter which can drive two PMSMs," in *Proceedings of 7th IET International Conference on Power Electronics, Machines and Drives (PEMD 2014)*, Manchester, UK, 2014, pp. 1–6.
[15] R. Wang, L. Ai, and C. Liu, "A novel three-phase dual-output neutral-point-clamped three-level inverter," in *IEEE Transactions on Power Electronics*, vol. 36, no. 7, pp. 7576–7586, Jul. 2021.
[16] R. Wang, S. Yuan, C. Liu, D. Guo, and X. Shao, "A three-phase dual-output T-type three-level converter," in *IEEE Transactions on Power Electronics*, vol. 38, no. 2, pp. 1844–1859, Feb. 2023.
[17] C. I. Odeh, A. Lewicki, M. Morawiec, and D. Kondratenko, "Three-level F-type inverter," in *IEEE Transactions on Power Electronics*, vol. 36, no. 10, pp. 11265–11275, Oct. 2021.
[18] C. I. Odeh, A. Lewicki, M. Morawiec, and J. O. Ojo, "A five-leg three-level dual-output inverter," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 70, no. 2, pp. 690–694, Feb. 2023.
[19] M. K. Pinjala and R. Bhimasingu, "Improving the DC-link utilization of nine-switch boost inverter suitable for six-phase induction motor," in *IEEE Transactions on Transportation Electrification*, vol. 6, no. 3, pp. 1177–1187, Sept. 2020.
[20] C. I. Odeh, A. Lewicki, and M. Morawiec, "A single-carrier-based pulse-width modulation template for cascaded H-bridge multilevel inverters," in *IEEE Access*, vol. 9, pp. 42182–42191, 2021.
[21] W. Wang, K. Ma, and X. Cai, "Efficient capacitor voltage balancing method for modular multilevel converter under carrier-phase-shift pulse width modulation," in *IEEE Transactions on Power Electronics*, vol. 36, no. 2, pp. 1553–1562, 2020.
[22] L. Pan, J. Zhang, J. Zhang, Y. Pang, B. Wang, K. Wang, and D. Xu, "A novel space-vector modulation method for nine-switch converter," in *IEEE Transactions on Power Electronics*, vol. 35, no. 2, pp. 1789–1804, Feb. 2020.
[23] Y. Wu, N. He, M. Chen, and D. Xu, "Generalized space-vector-modulation method for soft-switching three-phase inverters," in *IEEE Transactions on Power Electronics*, vol. 36, no. 5, pp. 6030–6045, May 2021.
[24] D. Schuetz, C. R. D. Osório, L. A. Maccari, D. M. Lima, F. de M. Carnielutti, and V. F. Montagner, "Space vector modulated model predictive control for grid-tied converters," in *IEEE Transactions on Industrial Informatics*, vol. 19, no. 1, pp. 414–425, Jan. 2023.
[25] P. R. U. Guazzelli, S. T. C. A. dos Santos, A. G. de Castro, W. C. de A. Pereira, C. M. R. de Oliveira, and J. R. B. de A. Monteiro, "Decoupled predictive current control with duty-cycle optimization of a grid-tied nine-switch converter applied to an induction generator," in *IEEE Transactions on Power Electronics*, vol. 37, no. 3, pp. 2778–2789, Mar. 2022.
[26] S. Vazquez, D. Marino, E. Zafra, M. D. V. Peña, J. J. R. Andina, and L. G. Franquelo, "An artificial intelligence approach for real-time tuning of weighting factors in FCS-MPC for power converters," in *IEEE Transactions on Industrial Electronics*, vol. 69, no. 12, pp. 11987–11998, Dec. 2022.
[27] A. G. Prieto, C. Martin, I. G. Prieto, M. J. Duran, J. C. Ríos, and J. J. Aciego, "Hybrid multivector FCS–MPC for six-phase electric drives," in *IEEE Transactions on Power Electronics*, vol. 37, no. 8, pp. 8988–8999, Aug. 2022.
[28] O. Gulbudak and E. Santi, "Model predictive control of dual-output nine-switch inverter with output filter," in *Proceedings of 2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Montreal, QC, Canada, 2015, pp. 1582–1589.
[29] P. R. U. Guazzelli, S. T. C. A. dos Santos, A. G. de Castro, W. C. de A. Pereira, C. M. R. de Oliveira, and J. R. B. de A. Monteiro,"Decoupled predictive current control with duty-cycle optimization of a grid-tied nine-switch converter applied to an induction generator," in *IEEE Transactions on Power Electronics*, vol. 37, no. 3, pp. 2778–2789, Mar. 2022.
[30] A. S. Hussein, V. Jayan, and A. Ghias, "Modeling and control of a three-level dual output voltage converter," in *Proceedings of 2019 IEEE International Conference on Industrial Technology (ICIT)*, Melbourne, VIC, Australia, 2019, pp. 1215–1219.

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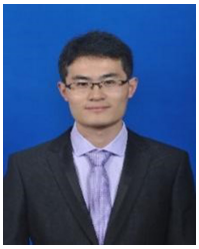

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