Frequency Multiplier Algorithm Based Fundamental Active Current Extraction and Phase Locked Loop for the Control of 3-Phase Shunt Active Power Filter

Amit V. SANT, Arpitkumar J. PATEL, and Josep M. GUERRERO

***Abstract*—Control of shunt power active filter (SAPF) necessitates estimation of the fundamental active component (FAC) of load current and unit voltage templates (UVTs). In this paper, a frequency multiplier based FAC and UVT extractor is proposed, wherein the α–β quantities of load current and supply voltage undergo frequency multiplier action to obtain the respective components with fundamental frequency four times the power frequency. With the band pass filtering of these signals, the components corresponding to four times the power frequency are determined. Thus obtained current components are further processed to extract the FAC of load current. Similarly obtained voltage signals are used by the synchronous reference frame theory based phase locked loop for accurate UVT extraction with the help of the designed synchronizing logic. The comparative analysis performed using an experimental setup demonstrates faster dynamic response and accurate estimation with a developed extractor compared to earlier reported schemes. The performance of SAPF controlled with the proposed extraction algorithm is investigated in PSIM software. Further, experimental validation is also presented. The SAPF operation with the proposed control scheme ensures unity power-factor operation and adherence to total harmonic distortion (THD) limits by drawing sinusoidal currents from the grid.**

***Index Terms*—Active filters, frequency multiplier, harmonics, power quality, shunt active power filter.**

I. Introduction

With the advances in signal and power electronics, power converters have emerged as the most suitable option for the modulation of power from supply to load in an efficient and automated manner. Moreover, with the increasing focus on energy conservation, power converters are increasingly being employed in lighting, electronic appliance, transportation, industrial and utility sectors [1]. However, the power converters usually necessitate the drawing of non-sinusoidal currents from the utility grid and thus, are seen as a nonlinear load from the utility end.

The increasing penetration of nonlinear loads is liable for power quality (PQ) degradation through current distortions and consequent voltage distortions [2]–[4]. These PQ issues have a detrimental effect on distribution system equipment and connected loads. These distortions are also accountable for increased line losses, overheating of cables, failure of protective systems and critical loads, etc. [2], [4]–[8]. As the PQ problems are directly or indirectly responsible for economic losses and an impediment to energy savings, it is necessary to mitigate them [9]. Hence, installation of a shunt active power filter (SAPF) for employing shunt compensation, at end user premise is advisable to prevent the deterioration of PQ due to the proliferation of current harmonics into the supply [10]. With SAPF supplying the harmonic and reactive components of load current, the grid needs to provide only the fundamental active component (FAC).

To control SAPF, extraction of FAC of load current and unit voltage template (UVT) extraction is critical. For estimating the FAC of load current, use of self-tuning filters [11], II-order filters [5], [7], [12], generalized integrators [13], neural networks [2], [14], [15], variants of least mean square (LMS) algorithm [16]–[19], and $I\cos(\phi)$ algorithm [20] are reported. The performance of generalized integrators and self-tuning filters is highly affected by the values of the constants used [5]. It necessitates proper selection of the constants to obtain optimal performance in terms of dynamic response and accuracy [5]. Training neural networks require a large data set corresponding to each possible case for accurate estimation when implemented in real-time [5], [21]. LMS algorithms are computationally intensive, which is further compounded when a variable convergence factor is employed for the performance enhancement of the LMS algorithm [5], [22]. With a fixed convergence factor, tuning is required and the LMS algorithm cannot provide optimal FAC extraction with respect to dynamic and steady-state response. In $I\cos(\phi)$ algorithm, the load current is filtered to obtain the fundamental component with a phase shift of 90° [20]. The FAC is the value of filtered current at the phase angle of π. $I\cos(\phi)$ algorithm is computationally simple and determines the peak value of FAC once every cycle [20]. A self-constructing fuzzy neural fractional order sliding mode control of active power filter is proposed in [23]. This control algorithm processes the reference harmonic current

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TABLE I
COMPARISON OF PROPOSED FAC EXTRACTION SCHEMES WITH STATE-OF-THE-ART METHODS

Fundamental active current extraction technique		ADALINE LMS [19]	SRF with low cut-off frequency for LPF [5], [26]–[27]	SRF with higher cut-off frequency for LPF [5], [26]–[27]	Proposed
Steady state ripples	Balanced load	Present when step size is high	None	None	None
	Unbalanced load	Present when step size is high	None	Present	None
Dynamic response		Fast for higher step size Sluggish for smaller step size	Sluggish	Faster	Faster

and the actual harmonic current for the generation of reference signal for the sinusoidal pulse width modulation technique. The control scheme is free from performance deterioration under variations in load or passive elements. In [24], fuzzy neural super twisting sliding mode control of SAPF using nonlinear extended state observer is proposed. This control scheme utilizes fast harmonic detection algorithm to compute the reference current.

UVT extraction is another significant part of the control of SAPF. For UVT extraction, synchronous reference frame (SRF) theory-based phase-locked loop (PLL) and generalized integrators are largely employed [25]. For FAC and UVT extraction, the challenge is maintaining the operation undisturbed without compromising the accuracy under non-ideal grid conditions and fast dynamic response. Also, a minimum requirement for the determinations of involved constants is preferable.

In this paper, the frequency multiplier based FAC and UVT extractor is proposed for the control of SAPF. This extraction method can also be extended for controlling distributed static compensator and unified power quality conditioner. In the proposed method, α–β axis quantities of load current and supply voltage with fundamental frequency as four times the power frequency are computed with the designed frequency multiplier. Thus, obtained current and voltage signals are filtered using band pass filter (BPF) to extract the components corresponding to four times the power frequency. Synchronizing logic is developed to assist the SRF-PLL in processing the determined voltage signals for the extraction of UVTs corresponding to fundamental positive sequence component (FPSC) of supply voltage. The obtained voltage and current signals are processed by the FAC extractor for computing peak value and power-factor (PF) of the FPSC of load current. Based on these computations, the FAC of load current is extracted. The proposed methodology results in accurate extraction of FAC and UVTs even under non-ideal operating conditions. With frequency multiplier action, faster extraction can be achieved and consequently dynamic response of SAPF can be improved. A comparative analysis of the proposed FAC extraction method with state-of-the-art techniques is presented in Table I, wherein, the proposed FAC extraction technique is compared with ADALINE-LMS and SRF theory-based FAC extraction methods [5], [19], [26]–[27].

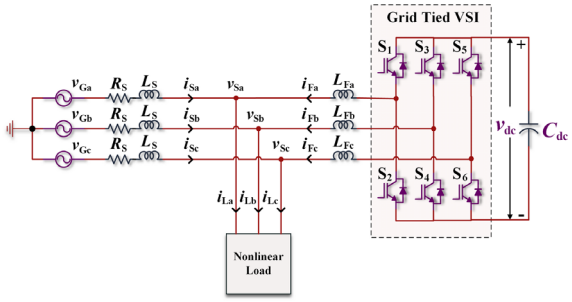

Fig. 1. Power circuit configuration of SAPF.

Highlights of the proposed work are: (a) frequency multiplier algorithm based on fundamental active current and unit voltage template extractor for the control of shunt active power filter is proposed, (b) proposed extraction algorithm offers a fast dynamic and accurate steady-state response, (c) control of SAPF with the proposed frequency multiplier based FAC and UVT extraction method is evaluated through simulation and experimental studies, and (d) SAPF operation using the proposed technique ensures power quality compliance with sinusoidal and balanced supply currents and unity PF.

II. GENERALIZED CONTROL OF SHUNT ACTIVE POWER FILTER

Fig. 1 demonstrates the power structure of SAPF consisting of a voltage source inverter (VSI) integrated with the grid at the point of common coupling (PCC) via coupling inductors, L_{Fa}-L_{Fb}-L_{Fc}. In the power structure, C_{dc} and v_{dc} represent the *DC*-link capacitor and the voltage measured across it. The three-phase voltages measured at PCC and the grid voltages are denoted as v_{Sa}-v_{Sb}-v_{Sc} and v_{Ga}-v_{Gb}-v_{Gc}, respectively. R_s and L_s represents the line resistance and inductance, respectively. i_{La}-i_{Lb}-i_{Lc} and i_{Sa}-i_{Sb}-i_{Sc} are the load currents and currents drawn from the grid, respectively. i_{Fa}-i_{Fb}-i_{Fc} are the currents supplied by SAPF for the requisite shunt compensation.

In case of non-linear loads, i_{La}-i_{Lb}-i_{Lc} are distorted and for the k^{th} phase can be represented as

$$i_{Lk}(t) = i_{LkFAC}(t) + i_{LkFRC}(t) + i_{LkHC}(t) \quad (1)$$

where, i_{LkFAC} is the FAC of i_{Lk}, , i_{LkHC} is the harmonic component

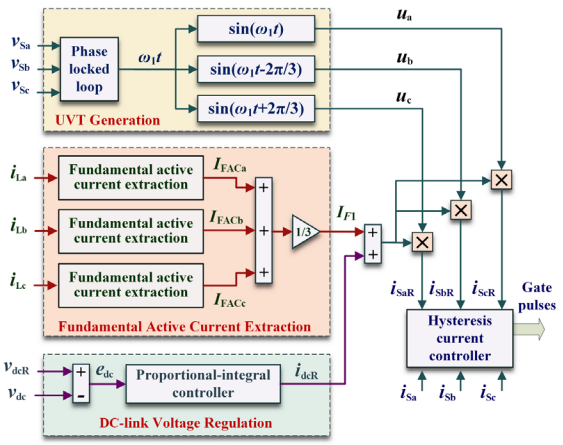

Fig. 2. Generalized control circuit configuration of SAPF.

(HC) of i_{Lk}, i_{LkFRC} is the fundamental reactive component of (FRC) of i_{Lk}, t is time, and k can be a, b or c.

The three components of i_{Lk} are i_{LkFAC} (fundamental active part responsible for supplying active power to the load), i_{LkFRC} (fundamental reactive part responsible for load magnetization) and i_{LkHC} (harmonics part responsible for the PQ degradation). In absence of SAPF, i_{LkFAC}, i_{LkFRC}, and i_{LkHC} are supplied by the grid. i_{LkFRC} and i_{LkHC} are responsible for grid congestion and reduced power transfer capability. Also, the flow of i_{LkHC} through the line is responsible for the non-sinusoidal voltage drop across the line impedance, resulting in distorted grid voltages and further deterioration of PQ. To collectively solve these issues, SAPF can be installed at the consumer premises to ensure that i_{Sa}-i_{Sb}-i_{Sc} are sinusoidal with unity PF. For this, i_{Fa}-i_{Fb}-i_{Fc} need to be controlled as per (2). This results in i_{Sk} being equal to i_{LkFAC} part of i_{Lk}. Thus, the proliferation of FRC and HC into the grid and occurrence of consequent issues, will be prevented, resulting in energy conservation and reduced energy bills.

$$i_{Fk}(t) = i_{LkFRC}(t) + i_{LkHC}(t) \tag{2}$$

The generalized control of SAPF, presented in Fig. 2, involves computation of reference source currents, i_{SaR}-i_{SbR}-i_{ScR}, for the indirect control of i_{Fa}-i_{Fb}-i_{Fc}. As per (3), computation of i_{SaR}-i_{SbR}-i_{ScR} requires extraction of peak value of FAC, I_{F1}, and UVT, u_k, corresponding to v_{Sk}. u_k is stated in (4), where ω_1 is the fundamental power frequency and p_k is the phase difference between u_k and UVT for the a-phase.

$$i_{SkR}(t) = I_{F1}(t)\, u_k(t) \tag{3}$$
$$u_k(t) = \sin(\omega_1 t - p_k) \tag{4}$$

The DC-link control of SAPF involves processing e_{dc}, the difference between v_{dc} and its reference value, v_{dcR}, through a proportional-integral (PI) controller for determining the active current required to be drawn from the grid, i_{dcR}, for the necessary regulation. Subsequently, to incorporate regulation of v_{dc}, i_{SkR} is modified as per (5). Gate pulses for the SAPF are

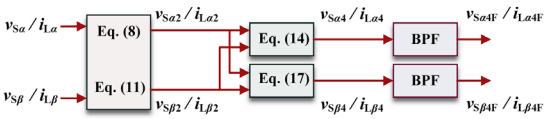

Fig. 3. Block diagram representation of the computational process for frequency multiplier action as per (8)-(19).

TABLE II
FREQUENCY SPECTRUM OF $x_{\alpha 4}$

f (Hz)	100	200	400	500	700	800	1000
%Magnitude	70.1	100.0	6.7	19.2	3.8	7.4	1.2

generated upon comparing i_{SkR} with the respective i_{Sk} using hysteresis current controller.

$$i_{SkR}(t) = [I_{F1}(t) + i_{dcR}(t)]\; u_k(t) \tag{5}$$

III. Frequency Multiplier Based UVT and FAC Extraction

A. Proposed Frequency Multiplier Action

3-phase voltages or currents can be represented in α–β reference frame as given in (6)-(7), where x represents voltage or current, X_m and θ_{1x} are the peak value and phase angle of FPSC, and H_α-H_β are the respective harmonic components. The frequency multiplier action is employed in two steps. First, x_α-x_β are individually processed by the frequency multiplier to determine $x_{\alpha 2}$-$x_{\beta 2}$, whose fundamental frequency is twice that of x_α-x_β. Thereafter, $x_{\alpha 2}$-$x_{\beta 2}$ undergo frequency multiplier action for obtaining $x_{\alpha 4}$-$x_{\beta 4}$, which are having the fundamental frequency as four times that of x_α-x_β. Fig. 3 displays the block diagram depiction of the computational process for frequency multiplier action as per (8)-(19). The steps involved in frequency multiplier action are elaborated in the Appendix.

$$x_\alpha = X_m \sin\theta_{1x} + H_\alpha \tag{6}$$
$$x_\beta = X_m \cos\theta_{1x} + H_\beta \tag{7}$$
$$x_{\alpha 2} = 2x_\alpha x_\beta \tag{8}$$
$$x_{\alpha 2} = X_m^2 \sin 2\theta_{1x} + H_{\alpha 2} \tag{9}$$
$$H_{\alpha 2} = 2(H_\alpha H_\beta + H_\alpha X_m \cos\theta_{1x} + H_\beta X_m \sin\theta_{1x}) \tag{10}$$
$$x_{\beta 2} = x_\beta^2 - x_\alpha^2 = X_m^2 \cos 2\theta_{1x} + H_{\beta 2} \tag{11}$$
$$x_{\beta 2} = X_m^2 \cos 2\theta_{1x} + H_{\beta 2} \tag{12}$$
$$H_{\beta 2} = H_\beta^2 - H_\alpha^2 + 2X_m(H_\beta \cos\theta_{1x} - H_\alpha \sin\theta_{1x}) \tag{13}$$
$$x_{\alpha 4} = 2x_{\alpha 2}x_{\beta 2} \tag{14}$$
$$x_{\alpha 4} = X_m^4 \sin 4\theta_{1x} + H_{\alpha 4} \tag{15}$$
$$H_{\alpha 4} = H_{\alpha 2}H_{\beta 2} + H_{\alpha 2}X_m^2 \cos 2\theta_{1x} \tag{16}$$
$$x_{\beta 4} = x_{\beta 2}^2 - x_{\alpha 2}^2 \tag{17}$$
$$x_{\beta 4} = X_m^4 \sin 4\theta_{1x} + H_{\beta 4} \tag{18}$$
$$H_{\beta 4} = H_{\beta 2}^2 - H_{\alpha 2}^2 + 2X_m^2(\sin 2\theta_{1x} \cos 2\theta_{1x}) \tag{19}$$

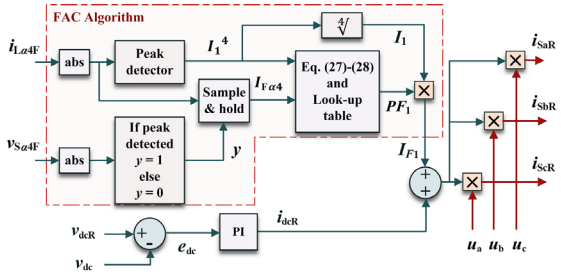

Fig. 4. Block diagram illustration of proposed algorithm for FAC estimation and reference current generation.

The frequency spectrum for the distorted $x_{\alpha 4}$, having the fundamental frequency of 200 Hz, is tabulated in Table II. It is clear that both harmonics and sub-harmonics are present. Using second-order BPF with center frequency as the nominal frequency, the fundamental component of $x_{\alpha 4}$-$x_{\beta 4}$ are obtained as shown in (20)-(21). Now, the fundamental orthogonal components $v_{S\alpha 4F}$-$v_{S\beta 4F}$ and $i_{L\alpha 4F}$-$i_{L\beta 4F}$ can be computed as shown by (22)-(25), where V_1 and I_1 are the peak amplitudes of PSFC of $v_{S\alpha}$-$v_{S\beta}$ and $i_{L\alpha}$-$i_{L\beta}$. The phase angle of PSFC of $v_{S\alpha}$ and displacement angle are denoted by θ_1 and ϕ_1, respectively.

$$x_{\alpha 4F} = X_m^{\,4} \sin 4\theta_{1x} \tag{20}$$

$$x_{\beta 4F} = X_m^{\,4} \cos 4\theta_{1x} \tag{21}$$

$$v_{S\alpha 4F} = V_1^{\,4} \sin(4\theta_1) \tag{22}$$

$$v_{S\beta 4F} = V_1^{\,4} \cos(4\theta_1) \tag{23}$$

$$i_{L\alpha 4F} = I_1^{\,4} \sin(4\theta_1 - 4\phi_1) \tag{24}$$

$$i_{L\beta 4F} = I_1^{\,4} \cos(4\theta_1 - 4\phi_1) \tag{25}$$

B. Proposed FAC Extraction Scheme

The block diagram representation of the proposed algorithm for extracting I_{F1} and generating of i_{SaR}-i_{SbR}-i_{ScR} is shown in Fig. 4. As reported in [20], I_{F1} can be computed by sampling the fundamental component of i_L phase shifted by 90° at the zero-crossing instant of the fundamental supply voltage. However, I_{F1} can also be computed by sampling the $|i_L|$ at the peak of $|v_s|$. Both the quantities should comprise of respective fundamental component only. Based on this alternate concept, the developed algorithm employs sample and hold logic for sampling $|i_{L\alpha 4F}|$ at the maximum value of $|v_{S\alpha 4F}|$. The sampled current, $I_{F\alpha 4}$, is mathematically expressed in (26). The determination of V_1 and I_1 are also included in this proposed algorithm. The peak value is computed by observing three consecutive samples. If the middle sample is greater than both the adjacent samples than that value represents the peak value.

Using (27), ϕ_1 is calculated. ϕ_1 can vary from 0° to $-\pi/2$ for inductive loads and $4\phi_1$ can range from 0 to -2π. Generally, in software the inverse cosine operation computes angles in the range of $-\pi$ to π. When ϕ_1 ranges from 0 to $-\pi/4$, the computation of $4\phi_1$ will be correct since it ranges from 0 to $-\pi$. However, when ϕ_1 ranges from $-\pi/4$ to $-\pi/2$, $4\phi_1$ varies between $-\pi$ to -2π, which leads to erroneous result. Hence, to overcome this error the corrected displacement angle, ϕ_2, is

TABLE III
LOOK-UP TABLE FOR DETERMINING ϕ_2

Case	sign($v_{S\alpha 4F}$)	sign($di_{L\alpha 4F}/dt$)	ϕ_2
I	$+ve$	$-ve$	$(2\pi - \phi_1)/4$
II	$-ve$	$+ve$	$(2\pi - \phi_1)/4$
III	$+ve$	$+ve$	$\phi_1/4$
IV	$-ve$	$-ve$	$\phi_1/4$

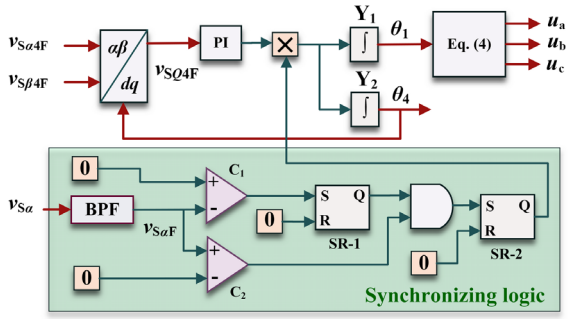

Fig. 5. Block diagram representation of the proposed frequency multiplier based SRF-PLL with synchronizing logic for UVT extraction.

calculated based on the polarity of $v_{S\alpha 4F}$ and $di_{L\alpha 4F}/dt$ as per the look-up table given in Table III. Next, the fundamental power-factor, PF_1, and I_{F1}, are computed as per (28)-(29), respectively. During steady state, I_{F1} is filtered through a moving average filter for removing the high frequency components and noise.

$$I_{F\alpha 4} = |i_{L\alpha 4F}||_{\theta = 22.5\ \&\ \theta = 67.5} = I_1^{\,4} \cos(4\phi_1) \tag{26}$$

$$\phi_1 = \cos^{-1}\left(\frac{I_{F\alpha 4}}{I_1^{\,4}}\right)/4 \tag{27}$$

$$PF_1 = \cos(\phi_2) \tag{28}$$

$$I_{F1} = I_1 \times \cos\phi_2 \tag{29}$$

C. Proposed UVT Extraction Scheme

Fig. 5 displays the block diagram representation of the proposed frequency multiplier based SRF-PLL with synchronizing logic for UVT extraction. $v_{S\alpha 4F}$-$v_{S\beta 4F}$ are utilized by the SRF-PLL structure for determining the *d*-*q* axis components, v_{Sd4F}-v_{Sq4F}. v_{Sq4F} is processed by a PI controller for computing ω_4 (=$4\omega_1$). Thereafter, for computing θ_4 (= $4\theta_1$) and θ_1, ω_4 is individually processed by integrators Y_2 and Y_1, which are correspondingly reset at 2π and 8π. θ_1 (=$\omega_1 t$) is obtained by dividing the output of Y_1 by four.

Referring to Fig. 6, the exact instant to reset θ_4, at which θ_1 is also reset, needs to be determined for ensuring proper synchronization. By the time θ_1 reaches from 0 to 2π, θ_4 has been reset four times. Hence, the initial starting point for θ_1 is to be determined for proper synchronization. This is ensured by the developed synchronizing logic shown in Fig. 5. In this logic, SR flip-flop *SR*-2 is initially reset, which results in the input and output of Y_1 being held at zero. At start, the first

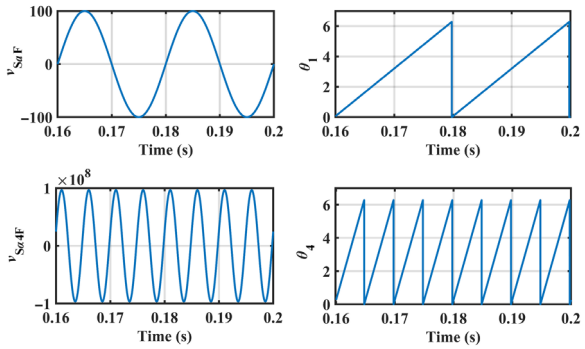

Fig. 6. Extraction of θ_1 and θ_4 with the proposed method.

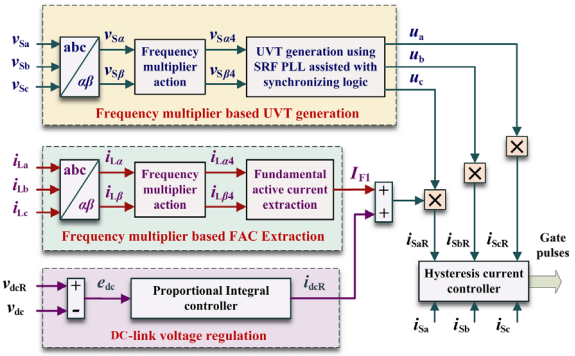

Fig. 7. Proposed frequency multiplier algorithm based control of SAPF.

negative half cycle of $v_{S\alpha F}$, the fundamental component of $v_{S\alpha}$, results in output of comparator C_1 being set to logic one. This in turn sets SR flip-flop *SR*-1. But, the output of AND gate is logic zero as the output of comparator C_2 is low. Upon the occurrence of subsequent positive half cycle, output of C_2 and consequently that of AND gate goes high. This sets *SR*-2 and enables Y_1-Y_2. Thus, the synchronizing logic ensures that Y_1-Y_2 are enabled at the beginning of positive half cycle of $v_{S\alpha F}$ and thereby results in synchronization of θ_1 with $v_{S\alpha F}$. Based on θ_1, the UVTs are computed and subsequently, based on u_k, I_1, i_{dcR} and ϕ_2, i_{SkR} is computed.

IV. Control of Shunt Active Power Filter With Frequency Multiplier Based UVT and FAC Extraction

The block diagram illustration of the control of SAPF with the proposed frequency multiplier algorithm based FAC and UVT extraction is shown in Fig. 7. Based on v_{Sa}–v_{Sb}–v_{Sc}, $v_{S\alpha 4}$–$v_{S\beta 4}$, having fundamental frequency as ω_4 (i.e. $4\omega_1$) are obtained using (8)-(19). The fundamental components, $v_{S\alpha 4F}$–$v_{S\beta 4F}$, are further determined by processing $v_{S\alpha 4F}$–$v_{S\beta 4F}$ through BPF. As shown in Fig. 5, SRF-PLL assisted with synchronizing logic is implemented for the computation of θ_1 and u_a–u_b–u_c. Similarly, using (8)-(19), the frequency multiplier algorithm computes $i_{L\alpha 4}$–$i_{L\beta 4}$, having fundamental frequency as ω_4. $i_{L\alpha 4F}$–$i_{L\beta 4F}$ are then obtained by filtering $i_{L\alpha 4}$–$i_{L\beta 4}$. As shown in Fig. 4, using alternate implementation of $I\cos(\phi)$ algorithm, $|i_{L\alpha 4F}|$ is sampled at the peak of $|v_{S\alpha 4F}|$. The sampled value is used to obtain I_{F1} as per (26)-(29) and Table III. Further, the regulation of v_{dc} is implemented as per the discussion presented in Section II and as shown in Fig. 7. The peak value of active current to be drawn from the grid is summation of I_{F1} and i_{dcR}, which is multiplied with u_a–u_b–u_c to generate the i_{SaR}–i_{SbR}–i_{ScR} as per (5). Hysteresis current controller generates the appropriate gate pulses for SAPF by comparing i_{Sa}–i_{Sb}–i_{Sc} with i_{SaR}–i_{SbR}–i_{ScR}. The produced gate signals ensure the VSI operation that results in requisite harmonic current mitigation and reactive power compensation as mandated by the established standards.

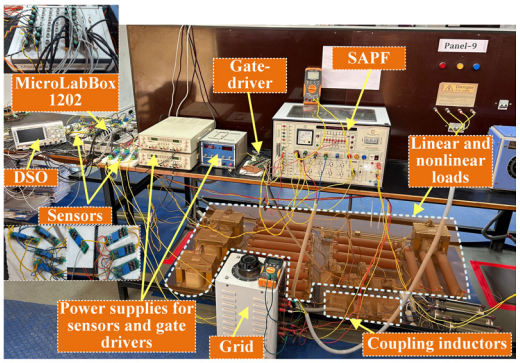

Fig. 8. Experimental prototype model of SAPF controlled with the proposed method.

V. Results and Discussions

For validating the performance of SAPF with the proposed frequency multiplier based FAC and UVT extractor, simulation as well as experimental studies are carried out. For simulation study, the system is modeled in PSIM software and its performance is analyzed for non-ideal supply and non-linear loading. The developed laboratory prototype model utilized to validate the performance of SAPF controlled with proposed technique is shown in Fig. 8 wherein major components of experimental set-up are labelled. The system parameters and part numbers of the components used in this study are given in Table IV. The SAPF comprise of IGBT's with part number SKM100GB12T4 is interface with the grid through L_{Fa}-L_{Fb}-L_{Fc} of 10 mH. The value of C_{dc} is 1800 µF. 3-phase, 122.47 V AC supply having nominal frequency of 50 Hz is utilized for the study. Same parameters for grid, L_{Fa}-L_{Fb}-L_{Fc} and C_{dc} are selected for the simulation studies. In experimental set-up, current sensors (LA55-P/SP1) and voltage sensors (LV 25-P/SP2) are utilized. These sensors will pass sensed signals to dSPACE MicroLab Box 1202, which implements the developed algorithm in real-time. The waveforms are observed with digital storage oscilloscope DSO-X2002A (Agilent Technologies) and DS1074Z (RIGOL). To validate the performance of SAPF controlled with the proposed technique under various operating conditions, different load configurations are utilized. Load–I is a 3-phase diode bridge rectifier (DBR) with 50 Ω load, Load–II is parallel combination of Load–I and 3-phase load of $(50 + j\omega_1 0.2)$, $(50 + j\omega_1 0.2)$ and $(100 + j\omega_1 0.2)$ Ω, Load–III is a 3-phase DBR with 25 Ω load, Load–IV is parallel combination of Load–I and 3-phase load of $(50 + j\omega_1 0.2)$,

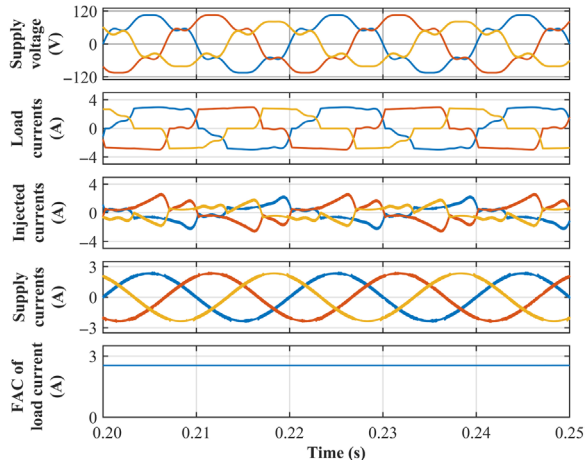

Fig. 9. SAPF operation with the proposed frequency multiplier based FAC and UVT extractor under steady state.

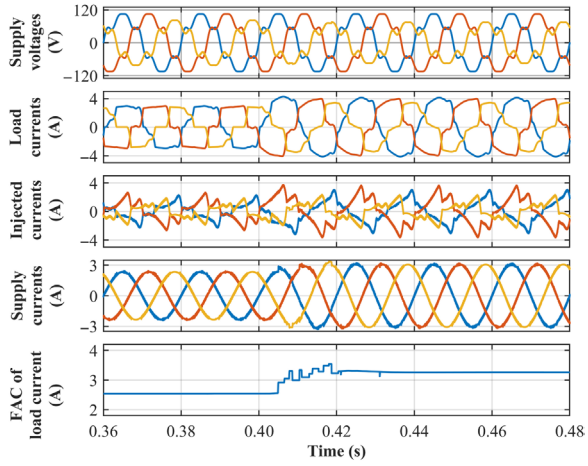

Fig. 10. SAPF operation with the proposed frequency multiplier based FAC and UVT extractor under change in load.

(50 + j$\omega_1$0.2) and (50 + j$\omega_1$0.2) Ω, and Load–V is parallel combination of Load–III and 3-phase load of (50 + j$\omega_1$0.2), (50 + j$\omega_1$0.2) and (50 + j$\omega_1$0.2) Ω.

Based on simulation studies, the performance of 3-phase SAPF controlled using the developed frequency multiplier based FAC and UVT extractor under steady state and load change is illustrated in Figs. 9 and 10, respectively. v_{Sa}–v_{Sb}–v_{Sc} are unbalanced and distorted with the corresponding peak values of 105-105-82 V and total harmonic distortion (THD) of 18-18-23.5%. For steady state analysis with Load-I, i_{La}–i_{Lb}–i_{Lc} have the %THD and peak amplitudes of 17.5-23-28 and 3-3-2.8 A, respectively. I_{F1} and PF_1 determined with the proposed method are 2.5 A and 0.89, respectively. The control of SAPF with frequency multiplier based FAC and UVT extractor results in i_{Sa}–i_{Sb}–i_{Sc} being balanced with %THD and peak amplitude of 3.5 and 2.31 A, respectively. With the change in load from Load–I to Load–II at 0.4 s, the peak values of i_{La}–i_{Lb}–i_{Lc} increase to 4.1-4.0-3.4 A. At the new steady state, they have %THD value of 12.8-17.7-24.3. The highest value of load current in the dynamic state is 4.2 A. The new steady state is attained in

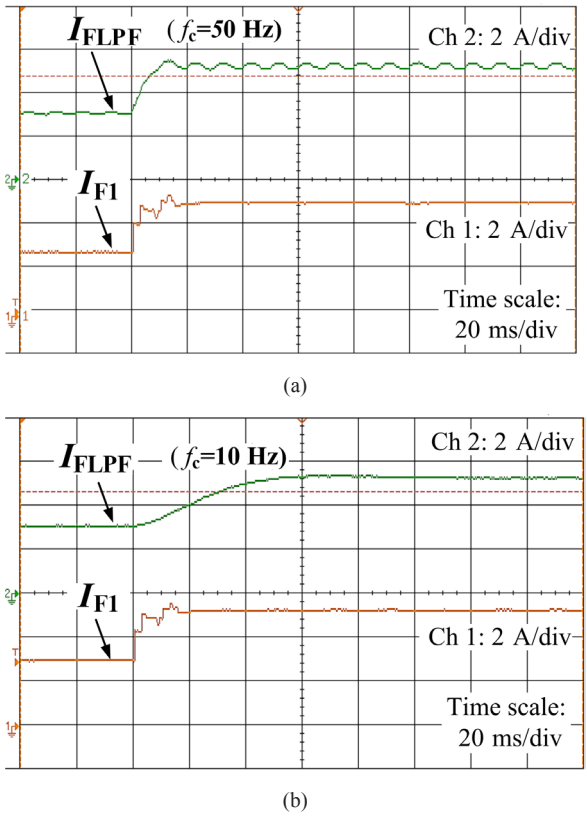

Fig. 11. Experimental results for (a) I_{FLPF} (f_c = 50 Hz) and I_{F1} under load change, (b) I_{FLPF}(f_c = 10 Hz) and I_{F1} under load change.

0.011 s with the I_{F1} and PF_1 recorded as 3.3 A and 0.84. SAPF operation results in i_{Sa}–i_{Sb}–i_{Sc} having %THD of 2.7 and the peak value of 3.08 A. In both cases, the SAPF operation with the proposed extraction method results in supply current being sinusoidal, balanced and in phase with the respective phase voltage irrespective of non-linear and unbalanced loading or unbalanced supply. Also, v_{dc} is regulated at the reference value of 250 V.

Fig. 11 shows the comparison of FAC extraction with the proposed algorithm and SRF theory employing the cut-off frequency, f_c, of 10 Hz and 50 Hz for the low pass filter. Upon switching of load, the extracted value of I_{F1} increases from 2.997 A to 5.284 A. The time required to attain the new steady state after the load change is 14 ms. In case of f_c = 10 Hz, extracted FAC, I_{FLPF}, demonstrates sluggish response, whereas with f_c = 50 Hz the dynamic response of I_{FLPF} is comparable to that of I_{F1}. With f_c = 50 Hz, there is presence of steady state ripple in I_{FLPF} when the load is unbalanced, which is unacceptable. The average value of I_{F1} matches that of the I_{FLPF} with f_c as 10 and 50 Hz. The proposed frequency multiplier based FAC extraction provides faster dynamic response without any steady state ripple even under non-ideal operating conditions.

The comparison of the proposed algorithm with the adaptive linear neuron (ADALINE) based LMS, reported in [19], is shown in Fig. 12. In [19], convergence factor, μ, is considered as 0.01. Similar implementation of ADALINE based LMS with μ = 0.01 results in sluggish dynamic response for FAC

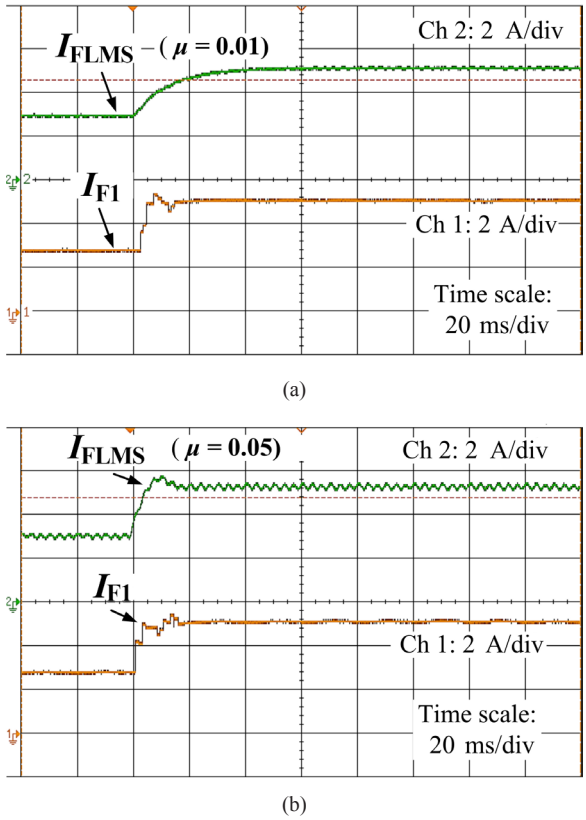

Fig. 12. Experimental results for (a) I_{FLMS} (μ = 0.01) and I_{F1} under load change, (b) I_{FLMS}(μ = 0.05) and I_{F1} under load change.

TABLE IV
SYSTEM PARAMETERS AND PART NUMBER OF COMPONENTS USED IN STUDIES

Parameter	Value
Nominal supply voltage	3-phase, 122.47 V AC voltage
Nominal grid frequency	50 Hz
L_{Fa}-L_{Fb}-L_{Fc}	10 mH
C_{dc}	1800 µF
Current sensors	LA55-P/SP1
Voltage sensors	LV25-P/SP2
IGBT	SKM100GB12T4
Controller	dSPACE MicroLab Box 1202
Sampling frequency	10 kHz
DSO	DS1074Z (Rigol) DSO-X2002A (Agilent Technologies)
Load-I	3-phase DBR with 50 Ω load
Load-II	Parallel of Load–I and 3-phase load of $(50 + j\omega_1 0.2)$, $(50 + j\omega_1 0.2)$ and $(100 + j\omega_1 0.2)$ Ω
Load-III	3-phase DBR with 25 Ω load
Load-IV	Parallel of Load–I and 3-phase load of $(50 + j\omega_1 0.2)$, $(50 + j\omega_1 0.2)$ and $(50 + j\omega_1 0.2)$ Ω
Load-V	Parallel of Load–III and 3-phase load of $(50 + j\omega_1 0.2)$, $(50 + j\omega_1 0.2)$ and $(50 + j\omega_1 0.2)$ Ω

extraction in the considered system. On the contrary, when μ is increased to 0.05 for improving the dynamic response, FAC

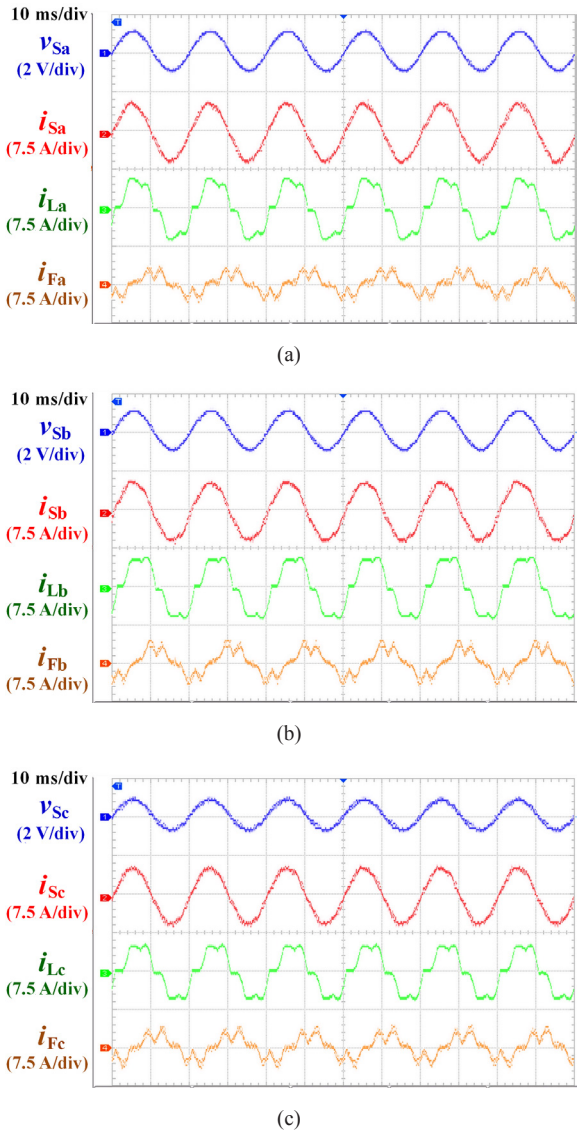

Fig. 13. Experimental results for steady-state operation of SAPF with the proposed frequency multiplier based FAC and UVT extractor with Load–III for (a) phase–a, (b) phase–b, and (c) phase–c.

extracted with ADALINE based LMS algorithm exhibits faster dynamic response with persistent oscillations at steady state. For load–I, FAC calculated using ADALINE based LMS, I_{FLMS}, are 3.13 A and 3.11 A for μ as 0.01 and 0.05, respectively. Similarly, for Load–III, I_{FLMS} is recorded as 5.31 and 5.26 for μ selected as 0.01 and 0.05, respectively. However, the developed scheme demonstrates faster dynamic response and no oscillations at the steady state.

For the experimental analysis of the proposed frequency multiplier based SAPF operation under steady state, three cases are considered: (I) unbalanced v_{Sa}-v_{Sb}-v_{Sc} and Load-III, (II) unbalanced v_{Sa}-v_{Sb}-v_{Sc} and Load-IV, and (III) unbalanced v_{Sa}-v_{Sb}-v_{Sc} and Load-V. For the three cases, the measured currents and voltages are tabulated in Table V. Experimental results for case-I are shown in Fig. 13. The peak values and %THD of v_{Sa}-v_{Sb}-v_{Sc} are 104-101-85 V and 2.51-2.61-3.87, respectively. Also, i_{La}-i_{Lb}-i_{Lc} are observed to be non-sinusoidal

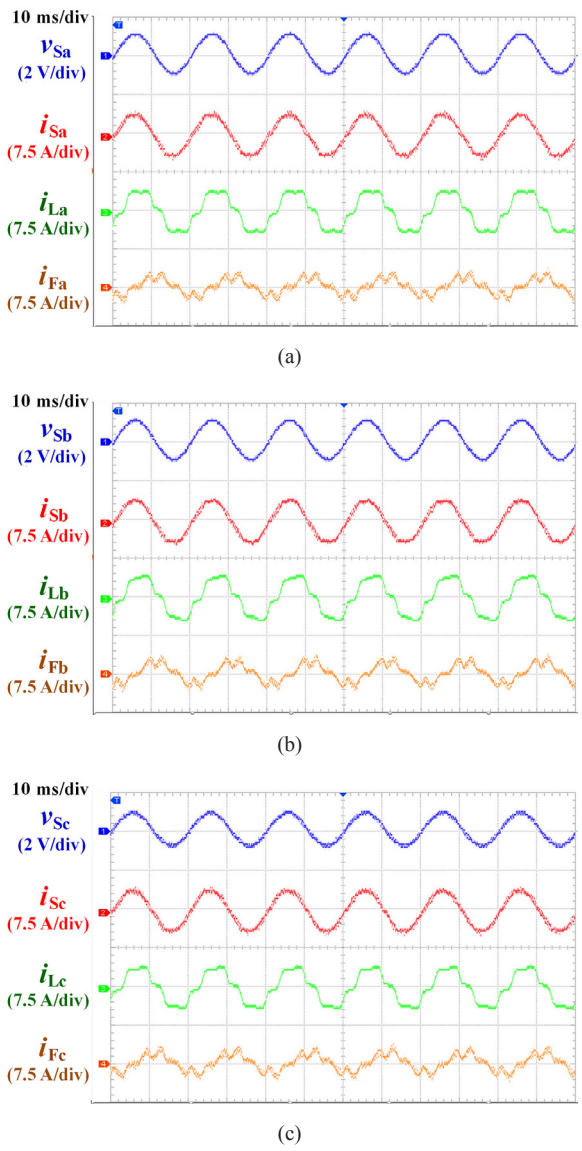

Fig. 14. Experimental results for steady-state operation of SAPF with the proposed frequency multiplier based FAC and UVT extractor with Load–III for (a) phase–a, (b) phase–b, and (c) phase–c.

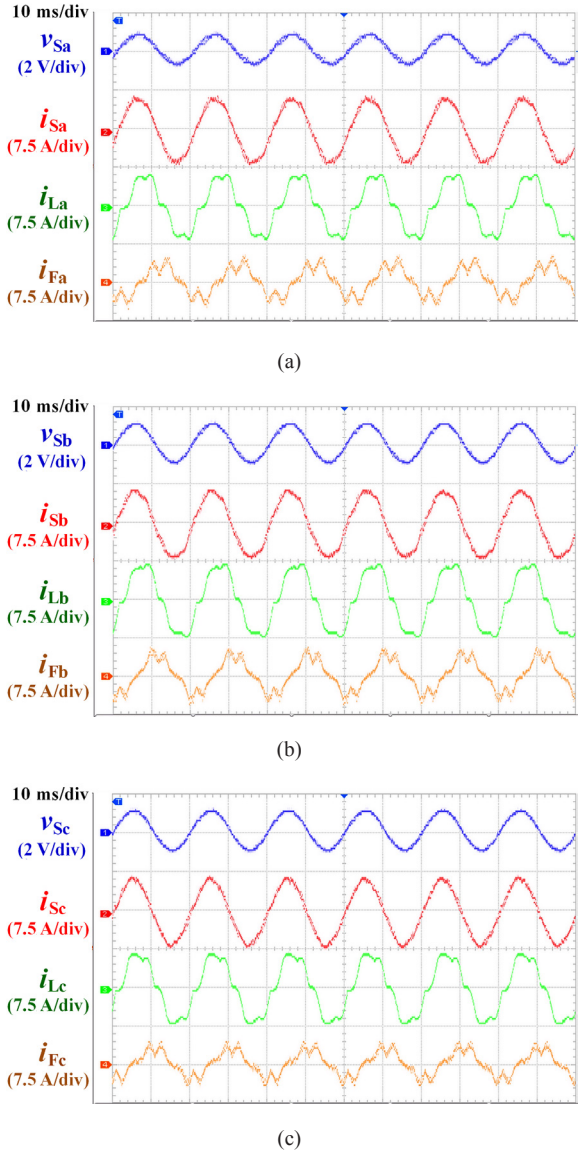

Fig. 15. Experimental results for steady-state operation of SAPF with the proposed frequency multiplier based FAC and UVT extractor with Load–III for (a) phase–a, (b) phase–b, and (c) phase–c.

with the corresponding %THD as 17.77-16.34-21.08. Moreover, with the unbalanced supply voltages, the peak values of i_{La}-i_{Lb}-i_{Lc} are measured as 5.8-5.8-5.3 A, respectively. The frequency multiplier algorithm based control of SAPF injects i_{Fa}-i_{Fb}-i_{Fc}, having peak values 3.3-4.3-3.9 A, to ensure i_{Sa}-i_{Sb}-i_{Sc} are maintained sinusoidal with %THD of 3.98-4.44-4.01. i_{Sa}-i_{Sb}-i_{Sc} are observed to have the peak values of 5.9-5.7-5.7 A, respectively. Sensor gain for v_{sa}-v_{sb}-v_{sc} in 0.01.

The experimental results for the steady state operation of SAPF using the developed algorithm for case-II are shown in Fig. 14, where v_{Sa}-v_{Sb}-v_{Sc} are unbalanced with peak values 105-104-94 V. Peak amplitudes and %THD of i_{La}-i_{Lb}-i_{Lc} are noted as 4.1-4.4-4.1A and 16.38-15.72-17.87, respectively. SAPF injects i_{Fa}-i_{Fb}-i_{Fc}, having the peak values 2.8-3.1-3.2 A, to implement shunt compensation so that i_{Sa}-i_{Sb}-i_{Sc} are observed to be sinusoidal with %THD of 4.45-4.20-3.92. The maximum values of i_{Sa}-i_{Sb}-i_{Sc} are noted as 4.6-4.4-4.6 A.

The experimental results for the steady state performance of SAPF controlled with the proposed algorithm for case-III are shown in Fig. 15. v_{Sa}-v_{Sb}-v_{Sc} are unbalanced with the peak values measured as 103-104-84 V. With the increased loading due to Load-V, the peak values of i_{La}-i_{Lb}-i_{Lc} are increased to 6.6-7.0-6.3 A. Despite high %THD of i_{La}-i_{Lb}-i_{Lc}, recorded as 14.86-13.40-18.05, i_{Sa}-i_{Sb}-i_{Sc} are controlled to be sinusoidal having %THD values as 4.38-4.63-3.64. The maximum values f i_{Sa}-i_{Sb}-i_{Sc} and i_{Fa}-i_{Fb}-i_{Fc} are correspondingly observed as 6.7-6.4-6.6 A and 4.0-5.0-4.5 A, respectively.

Figs. 11-12 validate the faster dynamic response of the proposed algorithm for computing the FAC of load current. Further, the experimental results for the dynamic performance evaluation of SAPF controlled using developed algorithm for switching of load from Load-IV to Load-V are presented

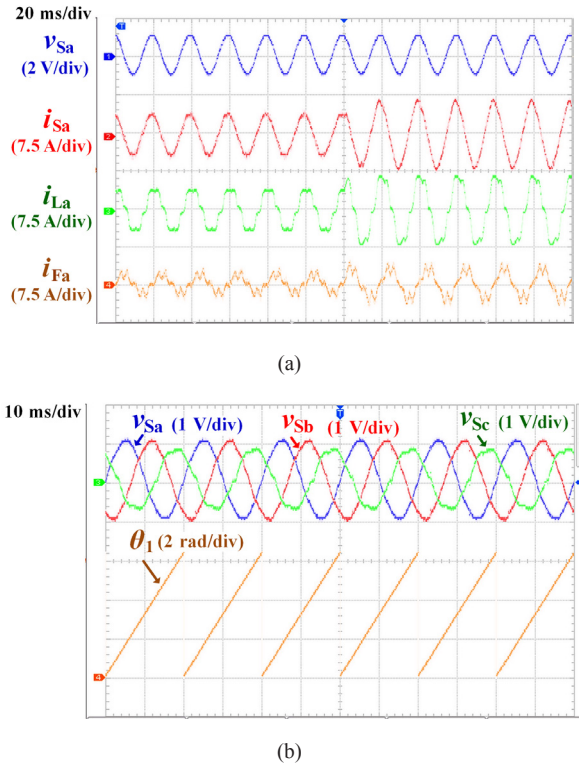

Fig. 16. Experimental results for (a) dynamic operation of SAPF with the proposed frequency multiplier based FAC and UVT extractor when the load is switched from Load–IV to Load–V, and (b) extraction of θ_1 with the proposed frequency multiplier based UVT extractor under unbalanced supply voltages.

TABLE V
STEADY STAGE PERFORMANCE ANALYSIS OF SAPF OPERATION WITH THE PROPOSED ALGORITHM

	Case-I		Case-II		Case-III	
Case	Peak value	%THD	Peak value	%THD	Peak value	%THD
v_{Sa}	104 V	2.51	105 V	2.28	103 V	2.67
v_{Sb}	101 V	2.61	104 V	2.54	104 V	2.94
v_{Sc}	85 V	3.87	94 V	3.16	84 V	4.33
i_{Sa}	5.9 A	3.98	4.6 A	4.45	6.7 A	4.38
i_{Sb}	5.7 A	4.44	4.4 A	4.20	6.5 A	4.63
i_{Sc}	5.7 A	4.01	4.6 A	3.92	6.4 A	3.64
i_{La}	5.8 A	17.77	4.1 A	16.38	6.6 A	14.86
i_{Lb}	5.8 A	16.34	4.4 A	15.72	7.0 A	13.40
i_{Lc}	5.3 A	21.08	4.1 A	17.87	6.3 A	18.05
i_{Fa}	3.3 A	–	2.8 A	–	4.0 A	–
i_{Fb}	4.3 A	–	3.1 A	–	5.0 A	–
i_{Fc}	3.9 A	–	3.2 A	–	4.5 A	–

in Fig. 16(a). After the load change, the peak magnitudes of load, supply and injected current increases from 4.1-4.6-2.8 A to 6.6-6.7-4.0 A, respectively. %THD for i_{Sa} is 4.45 before the load change and decreases to 4.38 after the change in load. The new steady state is attained before one cycle without any overshoots, oscillations or any other abnormality.

Fig. 16(b) demonstrates the effectiveness of the proposed SRF-PLL assisted with synchronizing logic for phase angle extraction and subsequent computation of UVTs. Even for the unbalanced grid voltages, θ_1 is accurately estimated without any presence of oscillations or any other abnormalities. This results in accurate UVT generation which are essentially required to ensure that the generated i_{SRa}-i_{SRb}-i_{SRc} and consequently i_{Sa}-i_{Sb}-i_{Sc} are in phase with the respective FPSC of v_{Sa}-v_{Sb}-v_{Sc}.

The presented simulation and experimental study reveal that the SAPF operation using the developed frequency multiplier algorithm based control results in sinusoidal grid currents and unity PF operation. The faster dynamic and accurate steady state response of the proposed scheme for computing the FAC of load current is also evident from the presented results. The simulation and experimental results presented in this section validate the feasibility, applicability, fast dynamic response and compliance with established power quality standards under ideal and non-ideal operating conditions.

VI. CONCLUSION

The control of SAPF with frequency multiplier based FAC and UVT extraction scheme is presented in this paper. The proposed algorithm individually processes the α-β components of load current and supply voltage through frequency multiplier and BPF to obtain the respective fundamental quantities with frequency four times the power frequency. Thus computed α-axis load current is sampled at the peak of the obtained α-axis supply voltage. PF is estimated using this sampled value and lookup table. FAC of load current is computed by multiplying PF and peak value of α-axis fundamental current raise to the power of 0.25. The obtained α-β voltages are used by SRF-PLL assisted with the designed synchronizing logic to correctly estimate the phase angle of the FPSC of supply voltage and UVTs corresponding to the power frequency. The simulation and experimental results validate that the proposed frequency multiplier based extraction scheme provides faster and accurate extraction of FAC and UVT regardless of the operating condition. The experimental studies for SAPF operation with the proposed extractor demonstrate drawing of sinusoidal and balanced source currents with THD less than 5% and in-phase with the supply voltages even under abnormal operating conditions.

APPENDIX

As mentioned in Section III, the frequency multiplier based algorithm is elaborated in this Appendix. $x_{\alpha 2}$ is defined in (8) as $2x_\alpha x_\beta$. Using (6) and (7), this can be expanded as

$$x_{\alpha 2} = 2[X_m \sin(\theta_{1x}) + H_\alpha][X_m \cos(\theta_{1x}) + H_\beta] \tag{30}$$

For separating the fundamental and harmonic components, $x_{\alpha 2}$ can be rewritten as

$$\begin{aligned} x_{\alpha 2} = {} & 2(X_m)^2 \sin(\theta_{1x}) \cos(\theta_{1x}) + \\ & 2H_\alpha X_m \cos(\theta_{1x}) + \\ & 2H_\beta X_m \sin(\theta_{1x}) + 2H_\alpha H_\beta \end{aligned} \tag{31}$$

The first term of (31) can be written in form of $2\theta_{1x}$ component to obtain component having frequency twice that of the fundamental component as

$$x_{\alpha 2} = (X_m)^2 \sin(2\theta_{1x}) + 2H_\alpha X_m \cos(\theta_{1x}) + 2H_\beta X_m \sin(\theta_{1x}) + 2H_\alpha H_\beta \quad (32)$$

$$x_{\alpha 2} = (X_m)^2 \sin(2\theta_{1x}) + H_{\alpha 2} \quad (33)$$

where, $H_{\alpha 2}$ is as defined in (10).

Similarly, frequency multiplier operation is performed to obtain $x_{\beta 2}$. For this, (11) can be written in expanded form using (6) and (7) as

$$x_{\beta 2} = (X_m \cos\theta_{1x} + H_\beta)^2 - (X_m \sin\theta_{1x} + H_\alpha)^2 \quad (34)$$

$$x_{\beta 2} = (X_m)^2 \cos^2(\theta_{1x}) + 2X_m \cos(\theta_{1x}) H_\beta + H_\beta^2 - (X_m)^2 \sin^2(\theta_{1x}) - 2X_m \sin(\theta_{1x}) H_\alpha - H_\alpha^2 \quad (35)$$

$$x_{\beta 2} = (X_m)^2 \cos^2(\theta_{1x}) - (X_m)^2 \sin^2(\theta_{1x}) + 2X_m [H_\beta \cos(\theta_{1x}) - H_\alpha \sin(\theta_{1x})] + H_\beta^2 - H_\alpha^2 \quad (36)$$

The first two terms of (36) have frequency twice that of the fundamental frequency and the remaining terms can be represented as $H_{\beta 2}$, which is defined in (13). Based on this, $x_{\beta 2}$ can now be expressed as

$$x_{\beta 2} = (X_m)^2 \cos(2\theta_{1x}) + H_{\beta 2} \quad (37)$$

Similar steps as mentioned in (30)-(37) can be used to process $x_{\alpha 2}$ and $x_{\beta 2}$ to further multiply the frequency and obtain components having fundamental frequency four times that of the grid frequency, $x_{\alpha 4}$ and $x_{\beta 4}$. The final expression for $x_{\alpha 4}$-$x_{\beta 4}$ are expressed in (15)-(18), respectively.

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