

A Configurable Multi Input Port Hybrid Inverter Topology With Quadrupled Voltage Gain for PV and Hybrid Applications

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Abstract—The presented work demonstrates the three-port inverter configuration for a quadrupled reduction in the operating DC bus voltage compared to conventional inverter topology. Thus, the proposed configuration consists the single inversion stage and operates with single or multiple sources. Irrespective of the source connected at input ports, the three inverters in the tri-inverter configuration synthesize the 512 switching combinations and spread across 61 voltage space locations to realize the load space vector. The switching states are segregated from the space spread not only to realize the maximum voltage gain but also to eliminate the common mode voltage during common DC source operations. In the case of common DC source operation, the CMV eliminated switching combinations ensures the elimination of circulating current with minimum compromise of the voltage gain. The improved voltage gain and eliminated circulating current guarantees the maximum energy yield from source and improved reliability of the converter compared to the conventional inverter. The proposed converter's efficacy and realized space vector switching states in terms of realizable four times voltage gain and the elimination of intra-inverter circulating currents are validated experimentally with single and multiple sources.

Index Terms—A multi-port network, common DC bus, configurable input ports, hybrid photovoltaic systems, inverter topology, renewable energy sources, voltage gain.

I. INTRODUCTION

THE power electronic converters are well suited for modulating the renewable energy in accordance with the load demand characteristics for efficient energy harvesting. The abundance, ease in installations and global political scenarios make the solar energy is an attractive green generation option among renewable sources. But the intermittent solar nature demands appropriate power converters topologies operate in hybrid mode with multiple energy and storage systems.

Therefore in recent, a multi input power converters are getting attention of researchers to prepare customized hybrid interfaces aiming to maximize the PV energy yield and ensure seamless power to the load as per the demand [1]–[5]. However, the major challenge is arbitrating the source characteristics for maximized efficiency, cost optimization and instantaneous load demand. In general PV panel exhibits the current source characteristics, thus it offer better energy yield at low voltage and high current. Contrary AC loads operate at high voltage and low current to achieve the optimized efficiency, thus inversion stage demands the higher DC voltage to synthesize the load AC voltage. To accomplish the required DC bus voltage, the researchers have suggested either step-up converters or PV panel interconnections at the inverter's input terminals. With the use of boost converters at the input terminals make the inverter configuration double stage. Even in two stage conversion, the limitations associated with the DC-DC converters in terms of voltage boost, the researchers have used either cascaded boost topologies or boost converter with sufficiently boosted input voltage through source (PV strings) interconnections to derive the demanded DC voltage for the inverter [6]–[14]. In the case of cascaded DC-DC converter configurations, the two or more number DC voltage conversion stages demands the complex synchronized stage algorithms for efficient voltage boost, and involved switching devices along with passive filter elements make the system less viable for industry adoption. Considering the drawbacks associated with the double stage conversion, past researchers have derived the DC bus voltages by connecting the PV strings/batteries in series at the input terminals, makes the inverter topology single stage [15]–[22]. In this case, although the requirement of the DC-DC converters is eliminated, the elevated DC potentials across the PV string negatively influence the life of solar panels and energy-yielding capacity during partial irradiation due to potential induced degradation effect and total number of involved panels per string, respectively [23].

In hybrid source applications with the double stage configurations, the DC converters are connected in parallel to feed to the common inversion stage. In the case of single-stage conversion topologies, the inverters are connected in parallel to feed to the single AC load/grid. However, the parallel topologies, the common DC (double stage) and AC (single-stage) coupling, attract the intramodular circulating current due to uncertainties in the instantaneous switching, control signal propagation delay, and impedance mismatch [24]–[26]. Since the common

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mode voltages between the converters are root cause for the circulating current, it is required to analyze the magnitude and frequency of the common mode voltage to cease/reduce the circulating current, thus to improve the thermal performance of the converters.

Apart from the circulating current in a parallel configuration, the other serious concern is the demand for bulky electrolytic capacitors with elevated DC potential at the input terminals [8]–[10], [18], [19]. The electrolytic capacitor generally has a short life span with a steep detrimental performance gradient and occupies more design space that adds to the overall weight, size, and cost of the inverter. At higher DC potential, the DC capacitors required to handle the higher voltage ripple acts as weak links in determining the system reliability and negatively influence the conversion power density of the configuration. Although the past researchers have tried to reduce the failure rate of the configuration and improve power density by reducing the DC link capacitor size [10], [19] but at the cost of demanded capacitance during uncertainties and over voltage scenarios. Since these methods are not addressing the root cause of the problem which is higher DC bus voltages, the recommended solutions can be seen as partial solutions. To overcome the associated drawbacks, it is required to reduce the operating potentials of the DC bus of inverter terminals.

This research introduces a novel tri-port voltage-sharing topology designed for hybrid source applications, addressing drawbacks found in existing typologies. The proposed configuration is adaptable for operation with both isolated and common DC sources, achieving maximum quadrupled voltage conversion gain through strategic switching. When connected to a common DC source, a comprehensive common mode voltage (CMV) analysis is crucial for selecting optimal switching states to achieve zero CMV. The categorization of switching states based on voltage gain and CMV magnitudes, derived through thorough analysis, enables multi and single source operations. Experimental validation against single and dual inverter typologies demonstrates the effectiveness of the proposed configuration, which, while demonstrated for 50 Hz applications, is versatile enough to accommodate any fundamental frequency by adjusting the reference space vector frequency. Additionally, the proposed configuration would attract the industry attention in the future due to the following associated advantages:

- 1) Ability to operate with single or multiple DC sources.
- 2) The reduced DC bus potential would ease the potential induced degradation (PID) effect on the solar panel that would improve solar panel life.
- 3) The minimum number of solar panels connected in series to derive the DC bus ensures the integrity of lower power applications compared to single-stage inverter topologies.
- 4) Due to lower DC bus requirement with the proposed configuration improves the MPPT efficiency during partial irradiation conditions.
- 5) The minimum DC bus voltages across the switching devices would ensure to go for maximum switching frequency.
- 6) The common-mode voltage elimination provides the

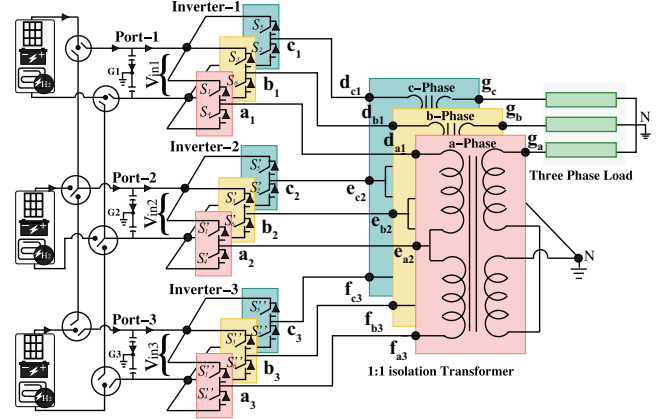


Fig. 1. The circuit diagram of proposed tri-port inverter configuration for voltage sharing.

flexibility to ground the DC bus.

II. THE PROPOSED HYBRID TRI-INPUT PORT SINGLE STAGE INVERTER CONFIGURATION

The proposed tri-input port single stage inverter configuration interfaced with the three phase load through three phase transformer as shown in Fig. 1. At the primary of the transformer, the derived center tapped winding (d–e and e–f) connected with the individual phases of tri-inverters. As it is shown in Fig. 1, the a-phase of the three inverter terminals a_1 , a_2 and a_3 connected with transformer terminals d_{a1} and e_{a2} and f_{a3} respectively. Similarly, the three inverter b-phase pole mid points (b_1 , b_2 and b_3) and c-phase pole mid points (c_1 , c_2 and c_3) are connected with the transformer primary winding terminals d_{b1} , e_{b2} , f_{b3} and d_{c1} , e_{c2} and f_{c3} respectively. At the secondary of the transformer, the three phase load connected with the terminals g_a , g_b and g_c and other end of the three phase secondary winding forms the neutral point as shown in Fig. 1. In this configuration, the three inverters connected with common/isolated DC sources collectively feeding to common AC load. Since the three inverters are involved in proposed configuration, with each inverter contribute 2^3 switching combination, combined $2^3 \times 2^3 \times 2^3 = 512$ switching combinations can be realized to synthesize the AC voltage across the load. Depending upon the switching combination of the proposed configuration, the realizable voltage space vector on transformer primary winding (d–e and e–f) and the load can be derived as:

Across primary winding (d–e) with Inverters 1 and 2 (Fig. 1)

$$V_{de_{ac}} = V_{dc} [(S_{a1} - S_{a2})e^{j0} + (S_{b1} - S_{b2})e^{j120} + (S_{c1} - S_{c2})e^{j240}] \quad (1)$$

Across primary winding (e–f) with Inverters 2 and 3 (Fig. 1)

$$V_{ef_{ac}} = V_{dc} [(S_{a2} - S_{a3})e^{j0} + (S_{b2} - S_{b3})e^{j120} + (S_{c2} - S_{c3})e^{j240}] \quad (2)$$

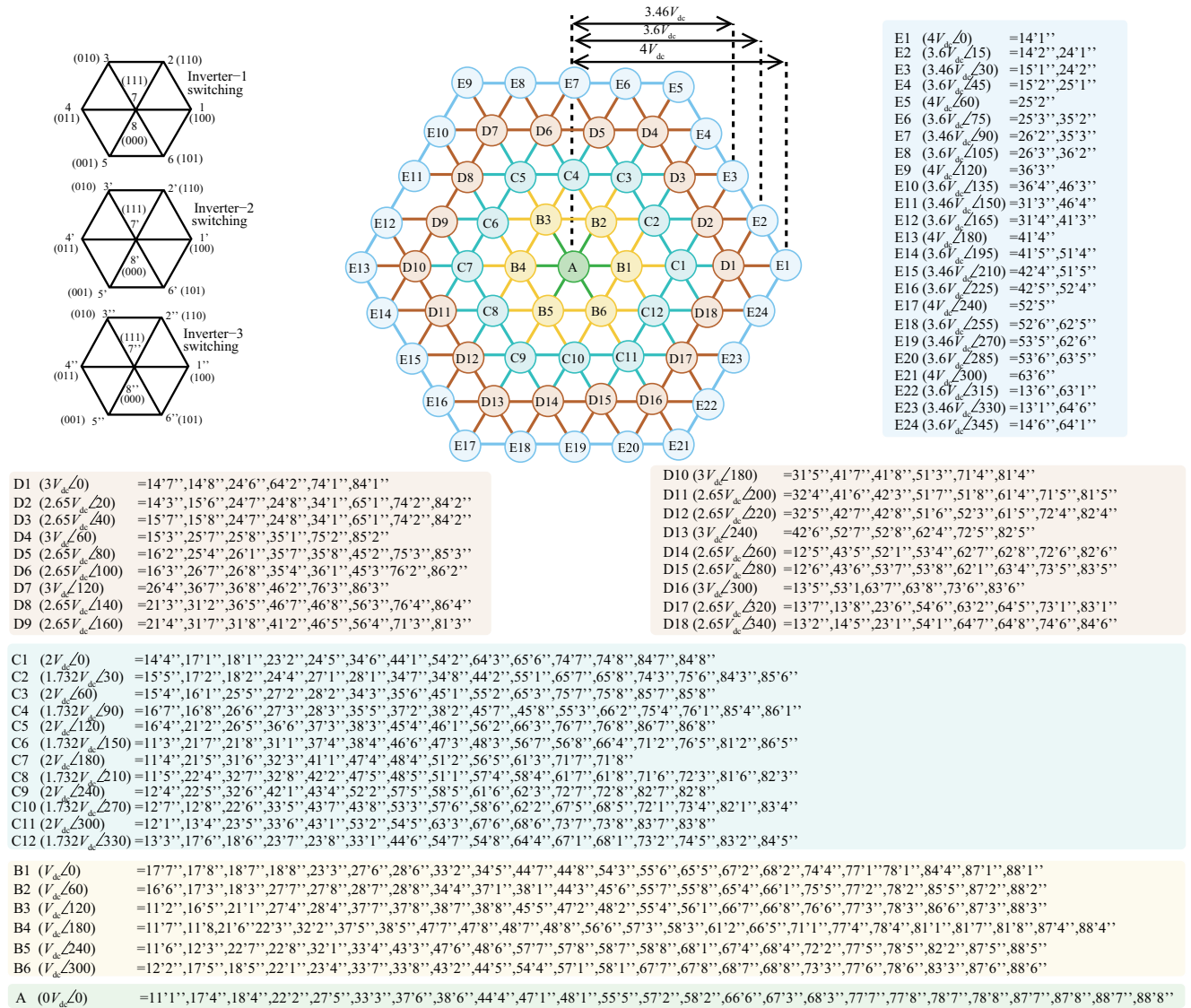


Fig. 2. The space spread of all possible switching combinations of the proposed configurations.

Combined voltage at secondary load terminals (V_{gabc})

$$V_{gabc} = V_{dc} \left[(S_{a1} - 2S_{a2} + S_{a3}) e^{j0} + (S_{b1} - 2S_{b2} + S_{b3}) e^{j120} + (S_{c1} - 2S_{c2} + S_{c3}) e^{j240} \right] \quad (3)$$

where S_{a1} , S_{b1} , S_{c1} are switching states of Inverter-1, S_{a2} , S_{b2} , S_{c2} are switching states of Inverter-2, S_{a3} , S_{b3} , S_{c3} are switching states of Inverter-3. The individual switch can attain either 1 (top switch of the leg is ON) or 0 (bottom switch of the leg is ON) and further, the top switch is complementary with the bottom switch. By substituting 512 switching combinations in (3), 61 space locations can be realized as shown in Fig. 2. For instance, the switching combination 1(100) with Inverter-1, 4'(011) with inverter-2 and 1''(100) with Inverter-3, the voltage at the load can be realized through (3) as $4V_{dc} \angle 0$. Although the derived switching combination can exhibit the voltage gain up to 4 compare to conventional topology, the interconnection of the inverter through winding demand inter-inverter influential

voltage (known as common mode voltage (CMV)) analysis of each switching state. In this work, the CMVs across the individual inverter (capacitor mid point) and the ground due to simultaneous switching of inverters in proposed configuration can be derived as:

$$CMV_{inv1} = \frac{1}{9} \left[(S_{a1} - S_{a2}) + (S_{a1} - S_{a3}) + (S_{b1} - S_{b2}) + (S_{b1} - S_{b3}) + (S_{c1} - S_{c2}) + (S_{c1} - S_{c3}) \right] \quad (4)$$

$$CMV_{inv2} = \frac{1}{9} \left[(S_{a2} - S_{a1}) + (S_{a2} - S_{a3}) + (S_{b2} - S_{b1}) + (S_{b2} - S_{b3}) + (S_{c2} - S_{c1}) + (S_{c2} - S_{c3}) \right] \quad (5)$$

$$CMV_{inv3} = \frac{1}{9} \left[(S_{a3} - S_{a1}) + (S_{a3} - S_{a2}) + (S_{b3} - S_{b1}) + (S_{b3} - S_{b2}) + (S_{c3} - S_{c1}) + (S_{c3} - S_{c2}) \right] \quad (6)$$

The magnitude of the derived CMV using (4), (5) and (6) for all 512 switching states are presented in Fig. 3. Further, it

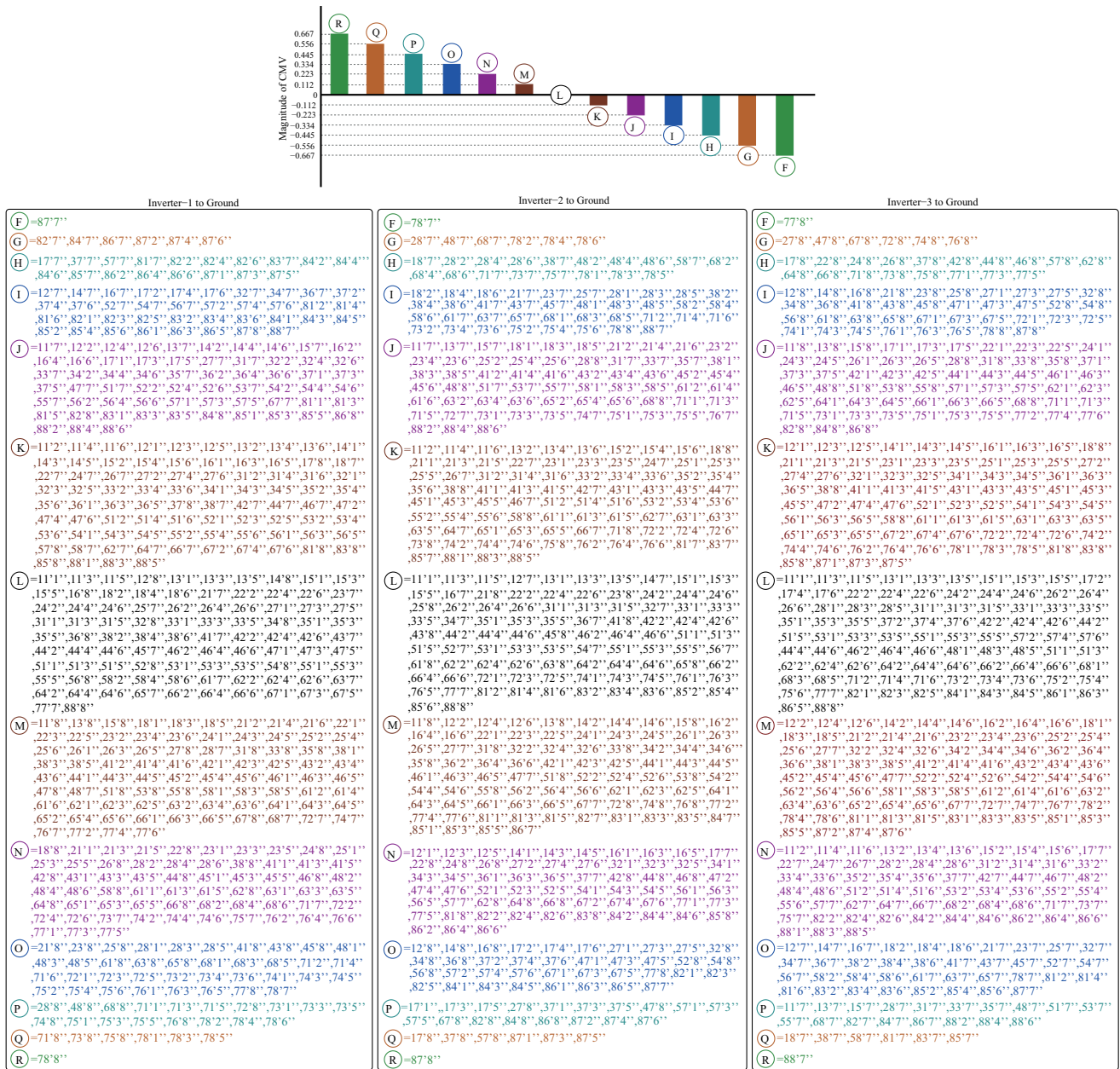


Fig. 3. The CMV magnitude variations and corresponding switching states with identified CMV between Inverter-1 and ground (from (4)), Inverter-2 and ground (from (5)) and Inverter-3 and ground (from (6)).

can be observed that the CMV between the individual inverter capacitor mid point and ground can attain 13 voltage levels $(+/-)0.667V_{dc}$, $(+/-)0.556V_{dc}$, $(+/-)0.445V_{dc}$, $(+/-)0.334V_{dc}$, $(+/-)0.223V_{dc}$, $(+/-)0.112V_{dc}$ and 0) as shown in Fig. 3. The existence of CMV between the capacitor mid point and ground restrict the DC bus grounding, thus only switching combinations with the zero common mode voltage (the switching combinations correspond to level ‘L’ shown in Fig. 3) can be used if in case DC bus need to be grounded. Further to operate the two/three inverter with the common DC bus, it is required to analyze the inter-inverter CMV between the inverters for zero influence of three inverters on each other. The inter-inverter CMV can be realized from the individual inverter CMV as:

$$CMV_{inv_{12}} = (CMV_{inv_{1g}} - CMV_{inv_{2g}}) \tag{7}$$

$$= \frac{1}{3} [(S_{a1} - S_{a2}) + (S_{b1} - S_{b2}) + (S_{c1} - S_{c2})] \tag{7}$$

$$CMV_{inv_{23}} = (CMV_{inv_{2g}} - CMV_{inv_{3g}}) \tag{8}$$

$$= \frac{1}{3} [(S_{a2} - S_{a3}) + (S_{b2} - S_{b3}) + (S_{c2} - S_{c3})] \tag{8}$$

$$CMV_{inv_{31}} = (CMV_{inv_{3g}} - CMV_{inv_{1g}}) \tag{9}$$

$$= \frac{1}{3} [(S_{a3} - S_{a1}) + (S_{b3} - S_{b1}) + (S_{c3} - S_{c1})] \tag{9}$$

With scrutiny of each possible switching combinations for three inverters present in the proposed configuration interms of realizable gain and the CMV magnitudes, the switching

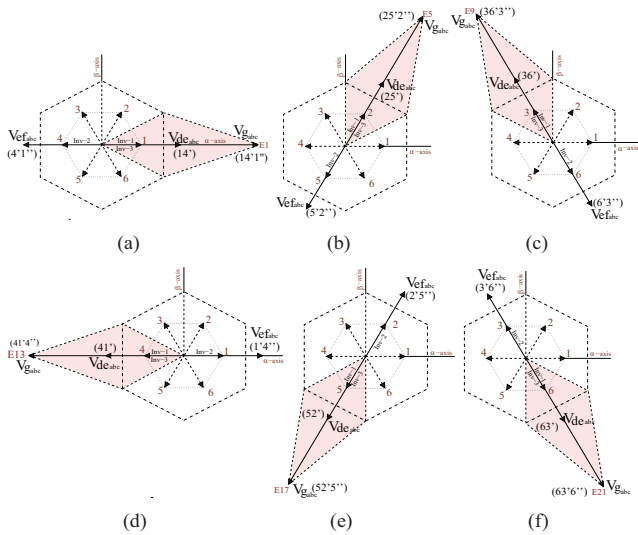


Fig. 4. The load space vector realization with the four gain switching locations. (a) 14°1', (b) 25°2', (c) 36°3', (d) 41°4', (e) 52°5', (f) 63°6'.

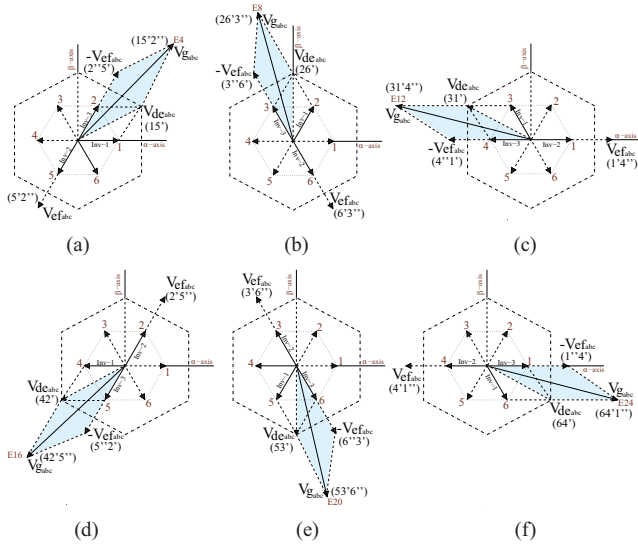


Fig. 5. The load space vector realization with the switching states mentioned in group-1 of Table I. (a) 15°2', (b) 26°3', (c) 31°4', (d) 42°5', (e) 53°6', (f) 64°1'.

combinations are categorized for different DC input port configurations as explained in the subsequent sub-section.

A. Case-1: The Three Isolated DC Sources Connected to the Each Input Port of the Three Inverter

In case of isolated DC sources, the electrical isolation between the primary side input ports and floating neutral allow to use all 512 switching combinations. Among 512 switching combinations, the outer hexagon switching locations E1, E5, E9, E13, E17 and E21 shown in Fig. 2 contribute to yield the maximum gain of four and synthesize the rotating magnetic field across the load (secondary of the transformer). Thus these switching combinations can be referred as "four gain" space locations and realization of quadrupled gain with these switching locations is shown in Fig. 4. For an instance, the switching combination 14°1', the Inverter-1 and Inverter-2

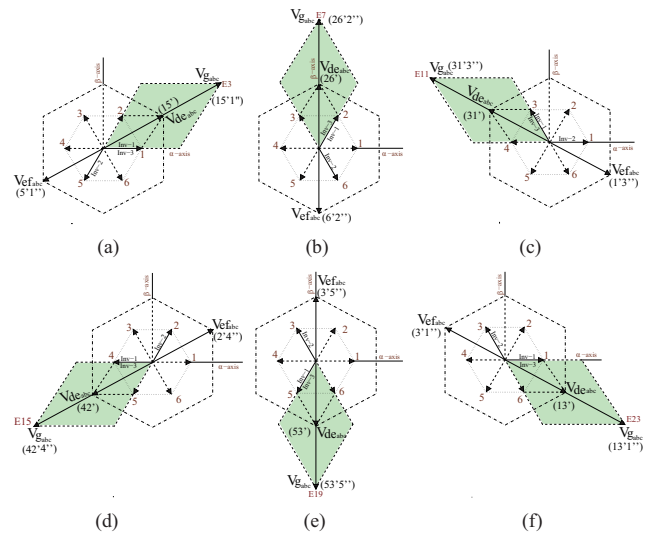


Fig. 6. The load space vector realization with the zero CMV switching states mentioned in group-4 of Table I. (a) 15°1', (b) 26°2', (c) 31°3', (d) 42°4', (e) 53°5', (f) 13°1'.

realizes the voltage of $2V_{dc}$ on winding d-e (Fig. 1), Inverter-2 and Inverter-3 also realizes the $2V_{dc}$ on winding e-f (Fig. 1) that generate the combined $4V_{dc}$ across the secondary winding as shown in Fig. 4(a). Similarly the the voltage gain realizations with the other four gain switching locations (E5, E9, E13, E17 and E21) in synthesizing the voltage space vector with the four gain is shown in Fig. 4.

B. Case-2: The Common DC Source Connected With Two Input Ports and Third Port Connected With Isolated DC Source

In case of two DC ports are fed from the common DC bus, it is required to ensure through switching combinations that, the CMV between inverters must be 0. In case of two inverters sharing the common DC bus, the corresponding switching combinations are categorized using (7)-(9) and presented in Table I based on the common DC bus fed inverter pair. As it is shown in Table I, the group-1 and group-4 switching combinations can exhibit zero CMV ensures the common DC bus for Inverters 1 and 2. Similarly, group-2 and group-4 switching combinations shown in Table I can be used with the shared DC bus between Inverters 2 and 3, and group-3 and group-4 switching combinations are used for common DC bus fed Inverters 3 and 1. Among these switching combinations, the group-1 of table I switching combinations representing the switching locations E4, E8, E12, E16, E20 and E24 (Fig. 2) are chosen to synthesize the rotating voltage vector in space. With these switching locations, the maximum voltage conversion gain of $3.6V_{dc}$ can be realized across the load with two inverters of the proposed configuration sharing the common DC bus as demonstrated in Fig. 5.

C. Case-3: The Common DC Source Shared With all Three Input Ports of the Inverters

When three inverters are fed from the common DC bus, the CMV voltages between the inverters must be 0 and inverters

TABLE I

THE IDENTIFIED SWITCHING COMBINATIONS FOR COMMON DC BUS FOR TWO INVERTER AND THREE INVERTER OPERATION OF PROPOSED CONFIGURATION

Input Port	Switching Combinations
Inverter-1 and Inverter-2 with common DC bus (Group-1)	11'2'',11'4'',11'6'',11'7'',11'8'',13'2'',13'4'',13'6'',13'7'',13'8'',15'2'',15'4'',15'6'',15'7'',15'8'',22'1'',22'3'',22'5'',22'7'',22'8'',24'1'',24'3'',24'5'',24'7'',24'8'',26'1'',26'3'',26'5'',26'7'',26'8'',31'2'',31'4'',31'6'',31'7'',31'8'',33'2'',33'4'',33'6'',33'7'',33'8'',35'2'',35'4'',35'6'',35'7'',35'8'',42'1'',42'3'',42'5'',42'7'',42'8'',44'1'',44'3'',44'5'',44'7'',44'8'',46'1'',46'3'',46'5'',46'7'',46'8'',51'2'',51'4'',51'6'',51'7'',51'8'',53'2'',53'4'',53'6'',53'7'',53'8'',55'2'',55'4'',55'6'',55'7'',55'8'',62'1'',62'3'',62'5'',62'7'',62'8'',64'1'',64'3'',64'5'',64'7'',64'8'',66'1'',66'3'',66'5'',66'7'',66'8'',77'1'',77'2'',77'3'',77'4'',77'5'',77'6'',77'8'',88'1'',88'2'',88'3'',88'4'',88'5'',88'6'',88'7''
Inverter-2 and Inverter-3 with common DC bus (Group-2)	12'2'',12'4'',12'6'',14'2'',14'4'',14'6'',16'2'',16'4'',16'6'',17'7'',18'8'',21'1'',21'3'',21'5'',23'1'',23'3'',23'5'',25'1'',25'3'',25'5'',27'7'',28'8'',32'2'',32'4'',32'6'',34'2'',34'4'',34'6'',36'2'',36'4'',36'6'',37'7'',38'8'',41'1'',41'3'',41'5'',43'1'',43'3'',43'5'',45'1'',45'3'',45'5'',47'7'',48'8'',52'2'',52'4'',52'6'',54'2'',54'4'',54'6'',56'2'',56'4'',56'6'',57'7'',58'8'',61'1'',61'3'',61'5'',63'1'',63'3'',63'5'',65'1'',65'3'',65'5'',67'7'',68'8'',71'1'',71'3'',71'5'',72'2'',72'4'',72'6'',73'1'',73'3'',73'5'',74'2'',74'4'',74'6'',75'1'',75'3'',75'5'',76'2'',76'4'',76'6'',81'1'',81'3'',81'5'',82'2'',82'4'',82'6'',83'1'',83'3'',83'5'',84'2'',84'4'',84'6'',85'1'',85'3'',85'5'',86'2'',86'4'',86'6'',87'7'',87'8''
Inverter-3 and Inverter-1 with common DC bus (Group-3)	12'1'',12'3'',12'5'',14'1'',14'3'',14'5'',16'1'',16'3'',16'5'',17'1'',17'3'',17'5'',18'1'',18'3'',18'5'',21'2'',21'4'',21'6'',23'2'',23'4'',23'6'',25'2'',25'4'',25'6'',27'2'',27'4'',27'6'',28'2'',28'4'',28'6'',32'1'',32'3'',32'5'',34'1'',34'3'',34'5'',36'1'',36'3'',36'5'',37'1'',37'3'',37'5'',38'1'',38'3'',38'5'',41'2'',41'4'',41'6'',43'2'',43'4'',43'6'',45'2'',45'4'',45'6'',47'2'',47'4'',47'6'',48'2'',48'4'',48'6'',52'1'',52'3'',52'5'',54'1'',54'3'',54'5'',56'1'',56'3'',56'5'',57'1'',57'3'',57'5'',58'1'',58'3'',58'5'',61'2'',61'4'',61'6'',63'2'',63'4'',63'6'',65'2'',65'4'',65'6'',67'2'',67'4'',67'6'',68'2'',68'4'',68'6'',71'7'',72'7'',73'7'',74'7'',75'7'',76'7'',78'7'',78'8'',81'8'',82'8'',83'8'',84'8'',85'8'',86'8''
Three inverters with common DC bus (Group-4)	11'1'',11'3'',11'5'',13'1'',13'3'',13'5'',15'1'',15'3'',15'5'',22'2'',22'4'',22'6'',24'2'',24'4'',24'6'',26'2'',26'4'',26'6'',31'1'',31'3'',31'5'',33'1'',33'3'',33'5'',35'1'',35'3'',35'5'',42'2'',42'4'',42'6'',44'2'',44'4'',44'6'',46'2'',46'4'',46'6'',51'1'',51'3'',51'5'',53'1'',53'3'',53'5'',55'1'',55'3'',55'5'',62'2'',62'4'',62'6'',64'2'',64'4'',64'6'',66'2'',66'4'',66'6''

must operate with the states mentioned group-4 of Table I. Among the group-4 switching combinations, the switching states correspond to switching locations E3, E7, E11, E15, E19 and E23 of Fig. 2 are identified to yield the maximum voltage conversion gain of $3.4V_{dc}$ as demonstrated in Fig. 6. From this discussion, it is evident that, the CMV eliminated switching locations can exhibit 13.5% and 3.8% lesser voltage conversion gain compare to case-1 and case-2 respectively.

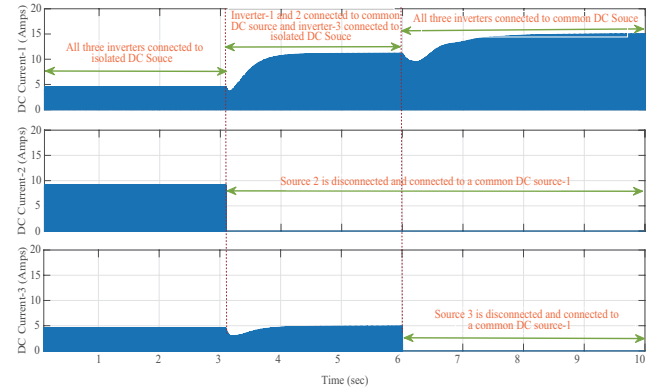


Fig. 7. Variation of DC source current-1 (top trace), source current-2 (middle trace) and source current-3 (bottom trace) with isolated and common DC Buses.

TABLE II
OPERATING PARAMETERS OF PROPOSED CONFIGURATION

Parameter	Value
Power (P)	2 kW
Operating DC voltage (V_{dc})	100 V
Load resistance (R)	38 Ω
Fundamental(f_s) and switching frequency(f_{sw})	50 Hz and 10 kHz
Leakage inductance(1:1 transformer)	0.21 mH

III. RESULTS AND DISCUSSIONS

A. Validation Through Simulation

The proposed tri-input port voltage sharing configuration was initially validated through Simulink simulations using the electrical parameters listed in Table II. In these simulations, all three inverters operated with an isolated DC bus of 100 V, utilizing the Case-3 switching algorithm. This setup aimed to demonstrate the effectiveness of the proposed configuration in functioning with either a common or isolated DC bus, particularly when source-2 and source-3 are unavailable.

The simulation results are illustrated in Fig. 7. As shown, until $t = 3.1$ s, all inverters operate with isolated DC sources, with the current shared among them, as evidenced by the top, middle, and bottom traces in Fig. 7. At $t = 3.1$ s, source-2 is disconnected and reconnected to source-1, causing Inverters 1 and 2 to share a common DC bus, while Inverter-3 continues to use the isolated DC source. Consequently, the current through source-1 doubles, source-2's current drops to 0, and source-3's current remains unchanged. At $t = 6$ s, source-3 is also disconnected and connected to the common DC source, resulting in source-2 and source-3 currents dropping to 0, with source-1 carrying the full load current. This transition was tested using the Case-3 algorithm due to its zero CMV, which allows for the safe connection of all DC buses without circulating currents among the inverter modules, as shown in Fig. 8. Additionally, the three phase-to-phase voltages are depicted in Fig. 9, illustrating a modulated square wave

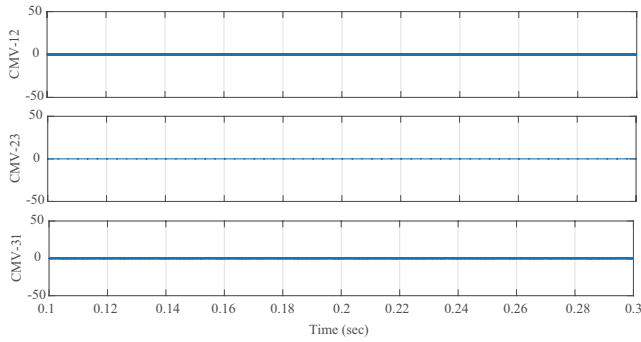


Fig. 8. CMV profile measured between capacitor midpoint of Inverter-1 and Inverter-2 (top trace), Inverter-2 and Inverter-3 (middle trace), and Inverter-3 and Inverter-1(bottom trace).

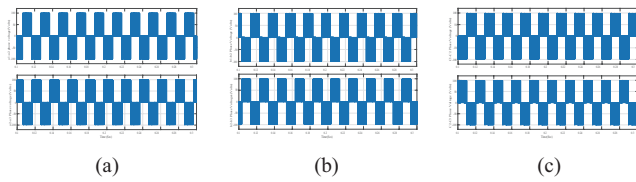


Fig. 9. Variation of phase-to-phase voltages at the transformer primary. (a) Phase-a voltages, (b) Phase-b voltages, (c) Phase-c voltages.

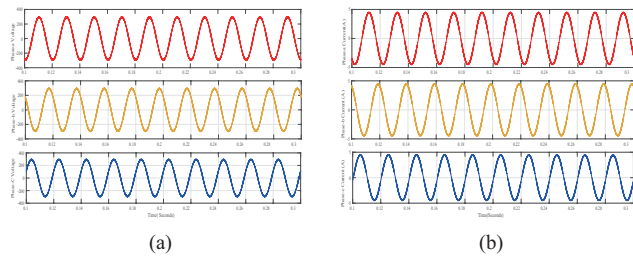


Fig. 10. Variation of three-phase load voltages and currents at the transformer secondary. (a)Three-phase voltages, (b)Three-phase currents.

shape with a ± 100 V variation, consistent with the 120-degree conduction mode and confirming the zero CMV. The output three phase load voltages and currents, shown in Fig. 10, demonstrate a perfect sinusoidal waveform. This highlights the effectiveness of the proposed configuration in operating with a reduced DC bus compared to conventional methods, and it also provides the flexibility to work with a common DC bus.

B. Validation Through Hardware

To further validate the system, an experimental prototype was developed and tested in the lab, as shown in Fig. 11. The prototype was tested with the electrical parameters listed in Table II across the three cases discussed in the preceding section. In all three cases, the maximum achievable gain and corresponding CMV profiles are validated experimentally as follows.

C. Case-1: Three Inverters Fed From Isolated DC Sources

As in case of three inverters operate with separate isolated DC sources, the switching locations 14'1''(E1), 25'2''(E5),

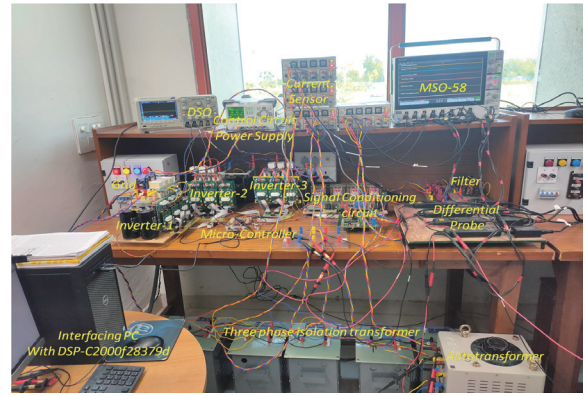


Fig. 11. The lab experimental prototype arrangement of proposed configuration.

36'3''(E9), 41'4''(E13), 52'5''(E17) and 63'6''(E21) are used in average to generate the load space vector as shown in Fig. 4 and corresponding a-phase pole voltages of Inverter-1 (V_{a1o}), Inverter-2 (V_{a2o}) and Inverter-3 (V_{a3o}) vary between $(+/-)50$ V with the DC bus of 100 V across each inverter is shown in top three traces of Fig. 12(a). The below two traces of the Fig. 12(a) shows the primary winding d-e and e-f (of Fig. 1) voltage vary between $(+/-)133$ V ($\frac{3}{4}V_{dc}$), $(+/-)66$ V ($\frac{2}{3}V_{dc}$) and 0 correspond to DC bus voltage of 100 V. The resulting three phase voltages across the load terminal with peak-peak magnitude of (460 V) and corresponding three phase load currents with peak magnitude of $(+/-)12$ A as shown in Fig. 12(b). From the experimental results it is evident that 100 V DC would yield 460 V (p-p) AC with the identified switching locations whereas in conventional parallel inverters 100 V would yield only 115 V (p-p) as demonstrated and compared in Fig. 15(c) that confirms the quadrupled gain with the proposed configuration. As it is depicted in preceding section, the "four gain" switching locations yield the corresponding CMV between the individual inverters DC capacitor mid point and ground depending upon the switching states of the three inverters as shown in Fig. 12(c). The magnitudes of the CMV shown in Fig. 12(c) is close concurrence with the theoretically computed CMV using (4), (5) and (6). For example, the switching state 41'4'' exhibits the CMV of $(+)11$ V ($\frac{1}{9}V_{dc}$) across the Inverter-1 DC bus and ground (left trace of Fig.12(c)), $(+)22$ V ($-\frac{2}{9}V_{dc}$) across Inverter-2 DC bus and ground (middle trace of Fig.12(c)) and $(+)11$ V ($\frac{1}{9}V_{dc}$) across the Inverter-3 DC bus and ground (right trace of Fig.12(c)) exactly matches with theoretical computations. Similarly, the CMV between Inverters 1 and 2 (left trace of Fig.12(d)), Inverters 2 and 3 (middle trace of Fig.12(d)) and inverters 3 and 1 (right trace of Fig.12(d)) also confirms the theoretically computed magnitudes using (7), (8) and (9).

D. Case-2: Two Inverters Operate With Common DC Bus

In case of sharing the common DC bus with Inverters 1 and 2, the switching locations from the group-2 and group-4 of Table I can be used. Among these switching combinations,

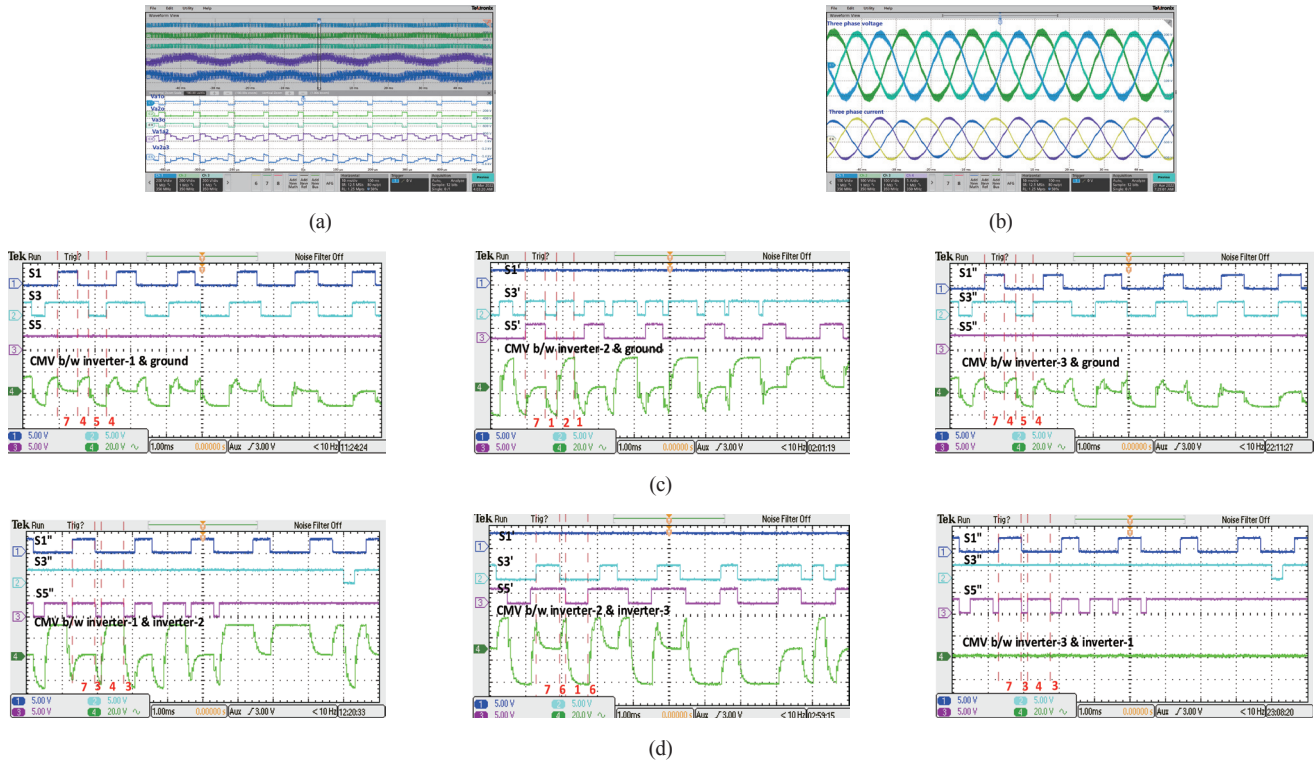


Fig. 12. The experimental results correspond to isolated DC sources feeding to the individual inverters (case-1) of the proposed configuration. (a) The pole voltage of Inverter-1 (top trace), Inverter-2 (2nd trace) and Inverter-3 (3rd trace) and resultant phase voltage across primary transformer winding d – e (4th trace) and e – f (bottom trace) (200 V/div). (b) The synthesized load three phase voltages (100 V/div) and three phase currents (5 A/div). (c) The switching states of Inverter-1 (left), Inverter-2 (middle) and Inverter-3 (right) and corresponding CMV of each inverter with reference to ground. (d) Inverter-1 switching states with CMV between Inverters 1 and 2 (left), Inverter-2 switching states with CMV between Inverters 2 and 3 (middle) and Inverter-3 switching states with CMV between Inverters 3 and 1 (right).

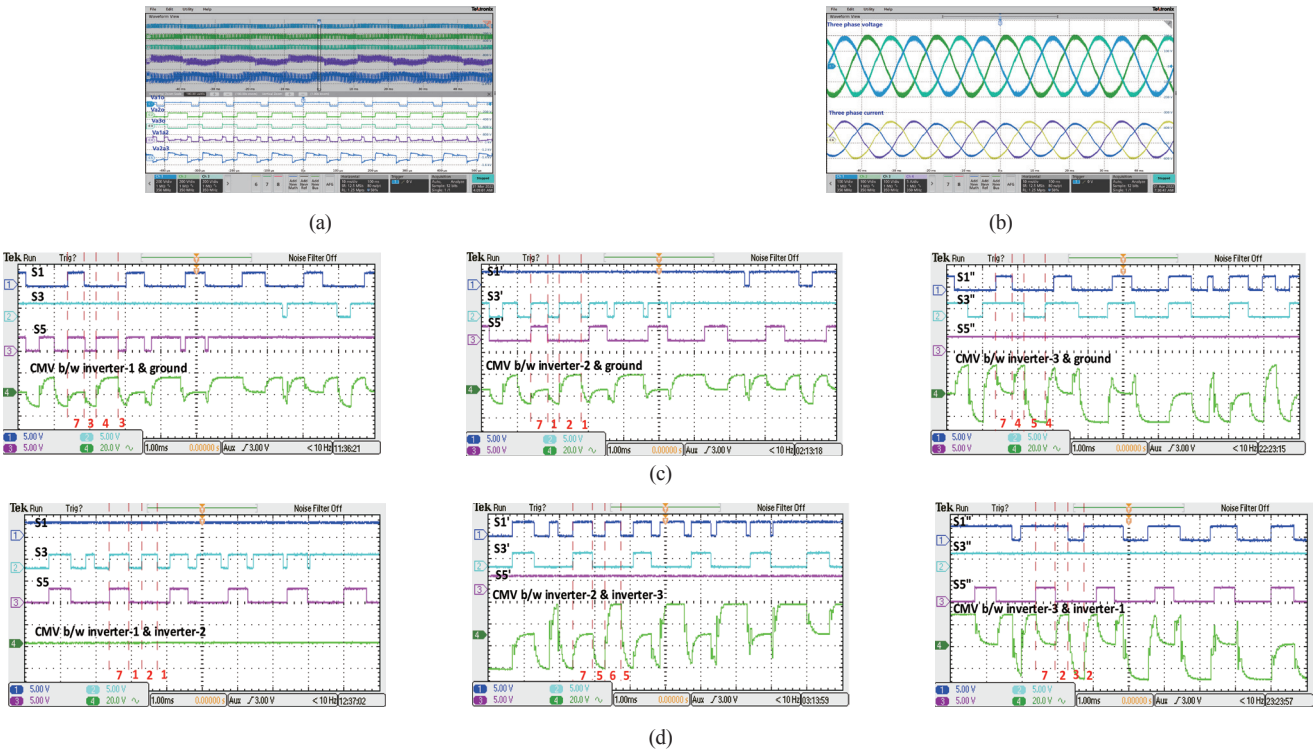


Fig. 13. The experimental results correspond to common DC sources feeding to the two inverters (case-2) of the proposed configuration. (a) The pole voltage of Inverter-1 (top trace), Inverter-2 (2nd trace) and Inverter-3 (3rd trace) and resultant phase voltage across primary transformer windings d – e (4th trace) and e – f (bottom trace) (200 V/div). (b) The synthesized load three phase voltages (100 V/div) and three phase currents (5 A/div). (c) The switching states of Inverter-1 (left), Inverter-2 (middle) and inverter-3 (right) and corresponding CMV of each inverter with reference to ground. (d) Inverter-1 switching states with CMV between Inverters 1 and 2 (left), Inverter-2 switching states with CMV between Inverters 2 and 3 (middle) and Inverter-3 switching states with CMV between Inverters 3 and 1 (right).

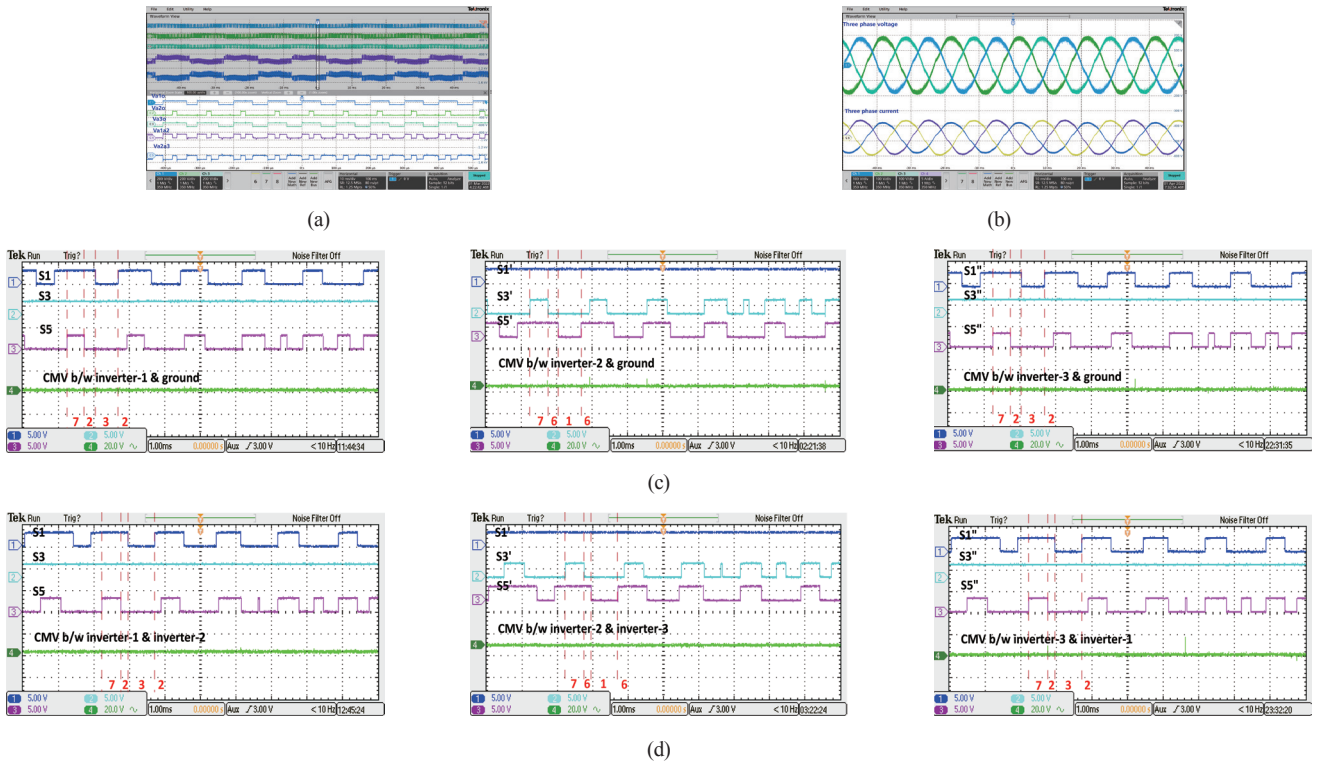


Fig. 14. The experimental results correspond to common DC sources feeding to all three inverters (case-3) of the proposed configuration. (a) The pole voltage of Inverter-1 (top trace), Inverter-2 (2nd trace) and Inverter-3 (3rd trace) and resultant phase voltage across primary transformer winding d – e (4th trace) and e – f (bottom trace) (200 V/div). (b) The synthesized load three phase voltages (100 V/div) and three phase currents (5 A/div). (c) The switching states of Inverter-1 (left), Inverter-2 (middle) and Inverter-3 (right) and corresponding CMV of each inverter with reference to ground. (d) Inverter-1 switching states with CMV between Inverters 1 and 2 (left), Inverter-2 switching states with CMV between Inverters 2 and 3 (middle) and Inverter-3 switching states with CMV between Inverters 3 and 1 (right).

the switching states 15'2''(E4), 26'3''(E8), 31'4''(E12), 42'5''(E16), 53'6''(E20) and 64'1''(E24) are used to synthesize the load voltage space vector as shown in Fig. 5. The corresponding experimentally obtained a-phase pole voltages of Inverter-1 (V_{a1o}), Inverter-2 (V_{a2o}) and Inverter-3 (V_{a3o}) vary between (+/-)50 V with the DC bus of 100 V each as shown in top three traces of Fig. 13(a). The primary winding d–e voltage vary between (+/-)100 V and e–f voltage vary between (+/-)133 V ($\frac{4}{3}V_{dc}$), (+/-)66 V ($\frac{2}{3}V_{dc}$) and 0 as shown in the below two traces of the Fig. 13(a). The resulting three phase voltages across the load terminal with peak-peak magnitude of 414 V and corresponding three load currents with the peak-peak magnitude of (+/-)11 A are shown in Fig. 13(b). The findings confirm a significant reduction in the DC bus requirement, demonstrating a 3.58-fold decrease compared to the SVPWM-based conventional parallel inverter and a 2.08-fold decrease compared to the per-phase balanced switching-based dual inverter configuration. Further, the common mode voltage patterns illustrated in Fig. 13(c) align with the defined switching states, affirming theoretical consistency. The matching CMV profiles between Inverter-1 DC bus to ground (left trace) and Inverter-2 DC bus to ground (middle trace) underscore the effectiveness of the proposed switching states in connecting the common DC bus for both inverters. The identical CMV profiles between Inverter-1 and Inverter-2 result in 0 circulating current between them, as verified by the CMV

measurement shown in the left trace of Fig. 13(d). However, varying CMV between Inverters 2 and 3 and Inverters 3 and 1, as per theoretical computations, are evident in the middle and right traces of Fig. 13(d). Notably, CMV between Inverter-2 and ground and Inverter-3 and ground exists, prohibiting the shorting of Inverter-3's DC bus with Inverter-2 or Inverter-1. Additionally, grounding the midpoint of the DC bus capacitor is not feasible, as it would result in continual circulating currents between the inverter modules and ground, primarily caused by the presence of common mode voltage (CMV).

E. Case-3: Three Inverters Operate With Common DC Bus

In case of three inverters operate with common DC bus, it is required to choose the switching states from group-4 of table I. In this case, the switching combinations 15'1'' (E3), 26'2''(E7), 31'3''(E11), 42'4''(E15), 53'5''(E19) and 13'1''(E23) are used in average sense to synthesize the load space vector as shown in Fig. 6. The corresponding experimentally obtained a-phase pole voltages of Inverter-1 (V_{a1o}), Inverter-2 (V_{a2o}) and Inverter-3 (V_{a3o}) vary between (+/-)50 V with the DC bus of 100 V each is shown in top three traces of Fig. 14. In this configuration, the voltage across primary windings d – e and e – f (refer to Fig. 1) varies within (+/-)100 V, as depicted in the two traces of Fig. 14(a). The resulting three-phase voltages at the load terminal measure 390 V (p-p), affirming a voltage gain compared to conventional inverters. Corresponding load currents exhibit a peak-to-peak magnitude of 10.3 A, as

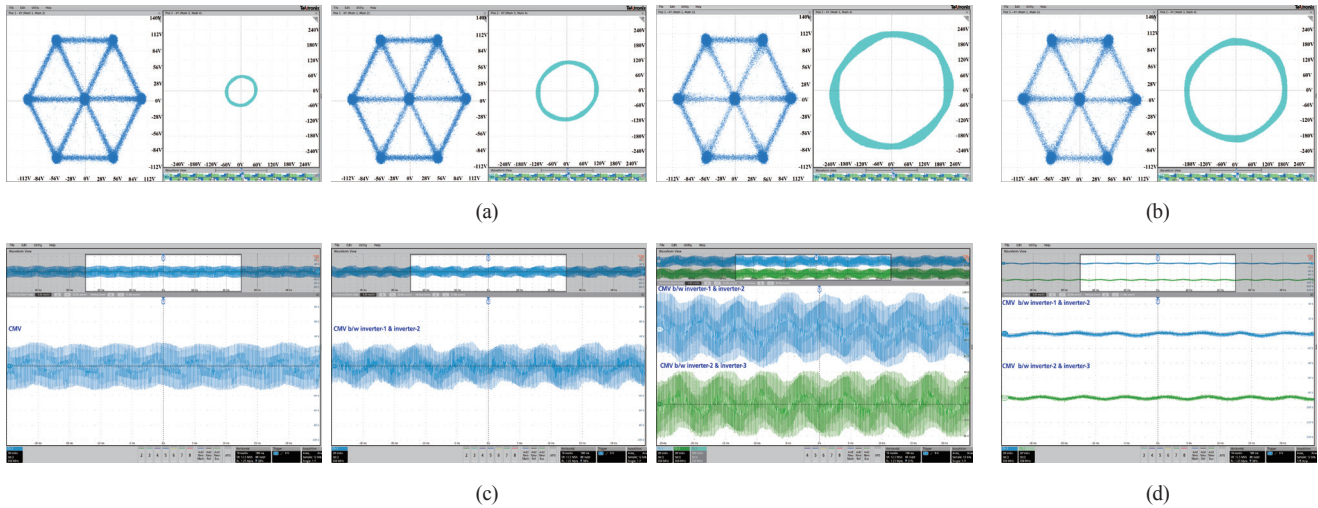


Fig. 15. Comparison of proposed configuration with conventional single stage and dual inverter configuration in terms voltage conversion gain and CMV profiles. (a) The three phase pole voltages and load voltage space vector variations in single inverter (left trace), dual inverter (middle trace) and proposed inverter configuration with maximum gain (right trace). (b) The three phase pole voltages and load voltage space vector variations for the proposed inverter configuration with zero CMV. (c) CMV profile of single stage inverter (left trace), dual inverter (middle trace) and proposed inverter configuration with case-1(right trace). (d) CMV profile of proposed inverter configuration with zero CMV.

TABLE III
COMPARISON OF PROPOSED TOPOLOGY WITH CONVENTIONAL PARALLEL INVERTER AND DUAL INVERTER

Topology	PWM Switching	AC Voltage	F_1	F_2	F_3	F_4
Conventional Parallel Inverter	SPWM	440 V	650 V	1(ref)	YES	NO
	SVPWM	440 V	560 V	1.16	YES	NO
Dual Inverter	Complementary Per phase Balanced	440 V	280 V	2.32	YES	NO
		440 V	325 V	2	NO	YES
Proposed	Case-1	440 V	140 V	4.64	YES	NO
	Case-2	440 V	156 V	4.16	Inverter-1 & 2-NO Inverter-1 & 3-YES	NO
	Case-3	440 V	165 V	3.93	Inverter-2 & 3-YES NO	YES

- 1) F_1 (Feature-1): Minimum DC bus voltage requirement to generate 440 V(L-L) AC.
- 2) F_2 (Feature-2): Converter voltage gain.
- 3) F_3 (Feature-5): Existence of CMV between the inverter modules.
- 4) F_4 (Feature-6): Provision of DC bus grounding.

illustrated in the bottom trace of Fig. 14(b). Moreover, there's a substantial reduction in the DC bus requirement, with a 3.4-fold decrease compared to SVPWM-based conventional parallel inverters and a 1.96-fold decrease compared to per-phase balanced switching-based dual inverter configurations. With the prescribed switching states, the CMVs of Inverter-1 to ground, Inverter-2 to ground, and Inverter-3 to ground, as evident in the left, middle, and right traces of Fig. 14(c), all register as 0, showcasing the successful elimination of CMV through meticulous switching strategies. This achievement not only ensures a robust system but also opens the door to grounding the midpoint of the DC bus capacitor, thereby contributing to the enhanced lifespan of the solar panel. Furthermore, the instantaneous zero CMV observed between Inverters 1 and 2, Inverters 2 and 3, and Inverters 3 and 1, as illustrated in the left, middle, and right traces of Fig. 14(d), guarantees a complete absence of circulating current, enabling the seamless utilization of a common DC source.

F. Comparison of Proposed Configuration With Existing Topologies

The proposed configuration is compared in this subsection with the conventional single stage inverter and dual inverters configurations in-terms of voltage gain and CMV elimination through proper selection of switching states. The experiments have conducted on the single inverter, dual inverter along with the proposed configuration for synthesizing AC voltage with the same DC bus voltage of 100 V. The pole voltage variations in space (X-Y plane) for single inverter, dual inverter and proposed configuration with case-1 is identical as shown in Fig. 15(a) represents the operating DC bus of 100 V. The corresponding synthesized AC voltage space variations (X-Y plot) across the load for single inverter, dual inverter and proposed configuration with case-1 is shown in left, middle and right trace of Fig. 15(a). From Fig. 15(a), it is clearly evident that the proposed configuration can exhibit quadrupled

gain compare single inverter configuration, and twice that of dual inverter configuration. Although the voltage gain is four times compare to conventional single and dual inverter, the common mode voltage exist between the inverter modules similar to single and dual inverter as shown in Fig. 15(c). But as demonstrated in preceding section, the CMV can be nullified in proposed configuration through appropriate selection of switching states as shown in Fig. 15(d) with the approximate 13.5% compromise in voltage gain as shown in Fig. 15(b) compare to maximum achievable gain of four. Subsequently, the comparison Table III is added to showcase the advantages of the proposed configuration over state-of-the-art topologies, covering aspects such as DC bus requirements, voltage gain, the presence of CMV profile, and DC bus grounding. This comparative analysis underscores the unique benefits and superior performance of the proposed topology, demonstrating its potential for practical applications.

IV. CONCLUSION

The hybrid source tri-port inverter proposed in this work is experimentally validated with isolated DC sources for quadrupled voltage gain. It means only 170 V DC bus is required to synthesize the standard AC voltage of 415 V (RMS L-L) reduces the DC bus requirements four times compare to conventional single stage inverters. Further, in this work it is demonstrated that through proper selection of switching states the CMV between the inverters can be eliminated. The eliminated CMV between the inverters provides the flexibility to operate the proposed configuration with common DC bus. Thus the proposed configurable port structure is advantageous for solar PV application wherein the generation and load demand are dynamic in nature.

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