A New 7, 15 and 31-level Modular Reduced Switch Multilevel Inverter With Gating Signal Generation Using Digital Output Pins

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***Abstract*—This paper proposes a reduced switch modular multilevel inverter (RSM-MLI) requiring eight, thirteen, and fifteen switches per phase for 7-level, 15-level, and 31-level output voltages, respectively. For the generation of 7-level, 15-level, and 31-level output voltages, the proposed MLI employs two, three, and four designed modules, each comprising switches, diodes, and a DC source, respectively. The interconnection of modules results in the generation of unipolar staircase voltage. Further, an H-bridge inverter (HBI) facilitates DC-AC conversion. With modular construction, the levels can be easily increased in the proposed topology by adding extra modules. The merits of the proposed topology are highlighted through a comparative analysis. The higher switch count in MLI necessitates the use of multiple digital signal processors (DSPs), thereby complicating the gating circuitry. To simplify the gating requirements, this paper utilizes the digital output pins in a DSP, which are far higher in number than the PWM pins, for gate pulse generation. This negates the needs of multiple DSPs. The operation of the developed experimental prototype of the proposed 7-level, 15-level, and 31-level RSM-MLI, controlled through the digital output pins of a DSP, is analyzed for steady-state and dynamic conditions.**

***Index Terms*—Inverters, modular, multi-level inverters, reduced switch count.**

I. Introduction

MULTI-LEVEL inverters (MLIs) find extensive usage in medium voltage drives, high voltage DC transmission systems, flexible AC transmission systems, and grid integration of renewable energy systems [1], [2]. Recently, MLIs have also been reported for low-power applications [3]. Generally, MLIs comprise of multiple power semiconductor switches, DC source/s, and capacitors. The distinguishing feature of MLI is the availability of output AC voltage with more than two levels. With the increase in voltage levels, the total harmonic distortion (THD) of voltage and current at the inverter output is reduced. Additionally, MLI offers the advantages of reduced voltage stress on switches, lower dv/dt and electromagnetic interference, and switching frequency lesser than that encountered in 2-level inverters [4].

The three basic MLI topologies are: (i) neutral point clamped (NPC) inverter, (ii) flying capacitor (FC) inverter, and (iii) cascaded H-bridge inverter (HBI) [4]. In MLIs, with an increase in output voltage levels, the number of switches and other components (diodes, DC sources and capacitors) also increase. All three topologies necessitate ($2n$–2) switches/phases for n-levels of output voltage. Moreover, clamping diodes are needed in NPC-MLI, and additional capacitors are necessary for FC-MLI. The use of additional capacitors results in increased cost and a challenge for voltage balancing. These traditional topologies need more switches for generating higher voltage levels and consequent increase in circuit complexity, requirement of gate drivers, heat sinks and protection units [5].

Reduced switch count (RSC) MLI topologies have drawn significant attention as they can overcome the demerits of increased switch count associated with the three basic MLI topologies. The evolution of RSC-MLI from a theoretical concept to practical realization is due to reduced switch count and gate driver requirements, increased efficiency and low cost [6]. A detailed survey on RSC-MLI topologies is presented by Vemuganti et al [6]. Different RSC-MLI topologies reported in the literature are modular RSC-MLI [7]–[9], transformer-based RSC-MLI [10], transformer-less RSC-MLI [11], single source RSC-MLI [12], multiple source RSC-MLI [13] unit based RSC-MLI [14], etc. Among these MLI topologies, modular RSC-MLI has gained significant interest due to the additional merits of high modularity and fault-ride-through capability [15]. Moreover, with modularity, the output voltage levels can be easily increased by adding additional modules or units.

Modular RSC-MLI with and without HBI are reported in [16]–[18]. Topologies with H-bridge feature a straightforward and cost-effective construction, providing ($2n$+1) levels for n levels [16]. Further, modular RSC-MLIs with single and multiple DC sources are also reported [12], [17]. Switched capacitor-based RSC-MLI are reported in [19], [20], wherein capacitors are added instead of using multiple DC sources. Such topologies can implement voltage boost action with capacitor switching [19]. This may eliminate the need for a step-up transformer [21]. Moreover, these topologies have self-balancing capability. However, SC-MLIs have the following

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drawbacks.

(a) Modulation complexity, complicated control schemes, increased switching losses, and requirement of higher capacitance [22].
(b) Difficulty in balancing capacitor size and voltage ripple impacts overall efficiency [23].
(c) The process of charging the capacitors in the fundamental units of switched-capacitor systems presents challenge in the form of significant surge in current. This abrupt increase in current, stresses the switches present in the charging path. Increased current stress can lead to wear and tear on switches, potentially reducing their operational lifespan and reliability [24].
(d) Soft start procedures/soft switching techniques can be helpful. However, as outlined in [24], it complicates system implementation. Also, realizing the soft switching technique for SC-MLIs is challenging.
(e) Practical implementations and applications, SC-MLI faces significant challenges in design, operation, and performance, primarily due to its reliance on capacitors, which complicates both design and operational aspects.

To tackle this problem, modular RSC-MLI topologies with multiple DC sources can be used, these topologies are reported [7]–[9]. Reference [7], presents an asymmetrical modular RSC-MLI made up of square T-Type modules. The module facilitates the generation of 17-level output voltage with twelve switches, of which six switches are utilized for forming three bidirectional switches, and three unequal DC sources. Another T-type topology, termed as cross switched T-Type topology, is described by Meraj et al [8]. The module facilitates the generation of 17-level output voltage with ten switches, of which four switches are utilized for forming three bidirectional switches, and three unequal DC sources. Samataei et al [9] have developed E-Type module for asymmetrical modular RSC-MLI, where each module can generate 13-level output voltage using ten switches and four unequal DC sources.

Packed U-cell (PUC) is another RSC-MLI topology reported in [25]–[27]. PUC-MLI utilizes only one DC source and necessitates voltage balancing for the capacitors employed. For 7-level output voltage, PUC-MLI employs a DC source, a capacitor, and six switches. Nonetheless, some inadequacies present in PUC-MLI are (a) not fully modular, (b) limited for the low power application, (c) higher switch rating, and (d) an increase in capacitor rating for extension of the topology [26].

In all MLI topologies, the increase in the number of levels is accompanied by a rise in the number of switches. Consequently, the number of pulse width modulated (PWM) gating signals increases. Generally, the digital signal processors (DSPs) used in power electronics applications have limited PWM pins. Multiple DSPs can be employed for the MLI, but it increases complexity and necessitates communication and synchronization between the DSPs involved.

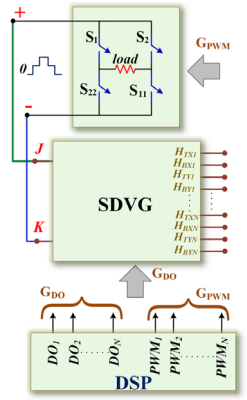
This paper proposes a new modular 7-level, 15-level, and 31-level modular RSC-MLI topology with gate pulse generation using digital output pins of a DSP. Two different modules, made up of switches, diodes, and a DC source, are employed. With the help of a network of these modules, a unipolar staircase voltage is generated. An H-bridge inverter further performs DC-AC conversion on the staircase voltage. The PWM gating signal generation for the modules makes use of the DSP's digital output pins, which are in substantially greater numbers. DC-AC conversion of unipolar staircase voltage is facilitated by an HBI. In HBI, a pair of diagonally opposite pins are ON during the positive half-cycle of output voltage. During the negative-half cycle, the alternate pair of switches is ON. In the proposed RSC-MLI topology, 7-level, 15-level, and 31-level output voltages are respectively generated with eight, thirteen, and fifteen switches per phase and two, three, and four modules per phase. Modular structure easily allows for level expansion. A detailed comparative analysis along with investigations on switch losses for the proposed RSC-MLI are also presented. Lastly, the proposed 7-level, 15-level, and 31-level RSC-MLI operations are validated through experimental studies.

The highlights of the proposed MLI topology are: (a) A new reduced switch modular multilevel inverter topology with the provision for 7, 15, and 31-level output voltage has been developed and its performance is validated experimentally. (b) The gate pulse generation for the proposed MLI has been implemented using general-purpose input output pins of TMS320F28335 DSP, instead of limited PWM pins. (c) The proposed MLI has the advantages of modular construction, absence of storage element, provision to bypass a module if any fault is developed, and thereby providing fault tolerant operation. (d) Assessment of power loss using equivalent circuits and mathematical equations is carried out. (e) A detailed comparative analysis reveals that the proposed MLI topology presents an optimal design with the balance between switch count and total standing voltage (TSV) requirement.

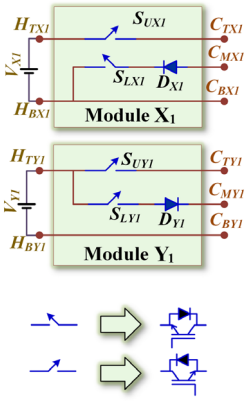
II. Proposed Modular RSC-MLI

The power circuit configuration of the proposed RSC-MLI topology for one phase is illustrated in Fig. 1(a). The power circuit consists of (i) a staircase DC voltage generation (SDVG) unit, and (ii) HBI made up of S_1-S_{11} and S_2-S_{22}. SDVG unit comprises of a network of modules with individual DC sources connected at the input terminals of the module. SDVG unit serves to provide unipolar staircase voltage across its output terminals, denoted by *J* and *K*. HBI, connected across *J* and *K*, performs the DC-AC conversion and thereby facilitates the availability of bipolar supply across the load.

SDVG circuit comprises of modules X and Y. Depending on the output voltage levels, the number of modules X and Y in SDVG unit varies. Fig. 1(b) shows the internal circuit configuration of module X and Y. Each of these modules comprises of two switches and a diode. Considering that A represents the module number, Module X_A comprises of upper switch, X_{UXA}, lower switch, S_{LXA}, diode, D_{XA}, two input terminals, H_{TXA} and H_{BXA}, and three output terminals, C_{TXA}, C_{MXA}, and C_{BXA}. In module X, two connections are provided at H_{BXA}. Connection of C_{BXA} at H_{BXA} facilitates the connection of DC source of the lower connected module in series with

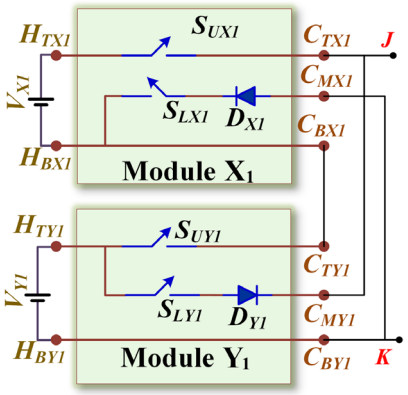


(a)

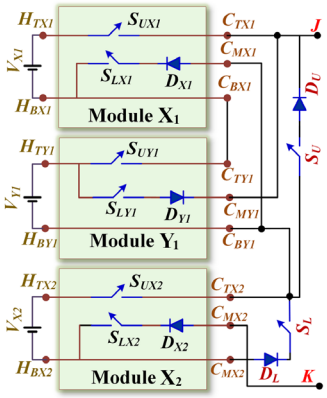


(b)

Fig. 1. Power circuit configuration of (a) proposed modular RSC-MLI, and (b) module X and Y.



(a)



(b)

Fig. 2. SDVG configuration for the proposed (a) 7-level modular RSC-MLI, and (b) 15-level modular RSC-MLI.

V_{XA}. While the connection of C_{MXA} to H_{BXA} through D_{XA}-S_{LXA} is utilized to bypass the lower connected module. S_{UXA} is used to make use of V_{XA}.

Similarly, Module Y_A, where A represents the module number, comprises of upper switch, S_{UYA}, lower switch, S_{LYA}, diode, D_{YA}, two input terminals, H_{TYA} and H_{BYA}, and three output terminals, C_{TYA}, C_{MYA} and C_{BYA}. In module Y, two connections are provided at H_{TYA}. S_{UYA} connecting H_{TYA} to C_{TYA} facilitates provision for series connection of V_{YA} with V_{XA}. The connection of H_{TYA} at C_{MYA} through S_{LYA}-D_{YA} is utilized to bypass module X.

In case of the modules, subscripts L and U respectively indicate lower and upper, whereas subscripts T, M and B correspondingly represent top, middle and bottom. SDVG formed with the cascade connection of one or multiple X and Y modules. As mentioned earlier, the number of X and Y modules in the MLI depend on the required levels of output AC voltage. If the output voltage of SDVG has n levels then the output of HBI has ($2n$+1) levels. The power circuit configuration of SDVG for 7-level, 15-level, and 31-level modular RSC-MLI are shown in Figs. 2 and 3. In the following sub-sections, the operation of the proposed MLI is demonstrated and analyzed for output AC voltage with 7-level, 15-level, and 31-level.

TABLE I
SWITCHING TABLE FOR THE PROPOSED 7-LEVEL MODULAR RSC-MLI

STATE/ MODE	Module								V_{JK}
	X_1		Y_1		X_1		Y_1		
	S_{UX1}	S_{LX1}	S_{UY1}	S_{LY1}	S_{SUX1}	S_{LUX1}	S_{SUY1}	S_{LUY1}	
1	-	-	-	-	-	-	-	-	0
2	-	-	-	1	0	0	V_a	0	V_{Y1}
3	1	1	-	-	0	0	V_a	0	V_{X1}
4	1	-	1	-	0	0	0	0	V_{X1}+V_{Y1}

A. Description of the Proposed 7-Level Modular RSC–MLI

Fig. 2(a) shows the power circuit configuration for the proposed 7-level modular RSC-MLI made up of cascade connection of modules X_1 and Y_1. V_{X1} and V_{Y1} are the DC sources connected across H_{TX1}-H_{BX1} and H_{TY1}-H_{BY1}, which are the input terminals for module X_1 and Y_1, respectively. At the output of SDVG, C_{TX1}-C_{MX1}-C_{BX1} of module X_1 are respectively connected to C_{MY1}-C_{BY1}-C_{TY1} module Y_1. The interconnection of C_{TX1}-C_{MY1} and C_{MX1}-C_{BY1} form the positive and negative terminals of SDVG, respectively indicated as terminals J and K. The switching table for this topology is shown in Table I, where V_{SUX1}-V_{SLX1}-V_{SUY1}-V_{SLY1} are the corresponding voltages

TABLE II
SWITCHING TABLE FOR THE PROPOSED 15-LEVEL MODULAR RSC-MLI

STATE/ MODE	Module								Voltage Across Switches								V_{JK}
	X_1		Y_1		X_2		S_U	S_L	S_{UX1}	S_{LX1}	S_{UY1}	S_{LY1}	S_{UX2}	S_{LX2}	S_U	S_L	
	S_{UX1}	S_{LX1}	S_{UY1}	S_{LY1}	S_{UX2}	S_{LX2}			V_{SUX1}	V_{SLX1}	V_{SUY1}	V_{SLY1}	V_{SUX2}	V_{SLX2}	V_{SU}	V_{SL}	
1	-	-	-	1	-	1	-	1	V_a	0	V_a	0	V_b	0	0	0	V_{Y1}
2	1	1	-	-	-	1	-	1	0	0	V_a	0	V_b	0	0	0	V_{X1}
3	1	-	1	-	-	1	-	1	0	0	0	0	V_b	0	0	0	$V_{X1}+V_{Y1}$
4	-	-	-	-	1	1	1	-	V_e	$-V_g$	V_f	V_a	0	0	0	0	V_{X2}
5	-	-	-	1	1	1	-	-	V_a	0	V_a	0	0	0	0	0	$V_{X1}+V_{X2}$
6	1	1	-	-	1	1	-	-	0	0	V_a	0	0	0	0	0	$V_{X1}+V_{X2}$
7	1	-	1	-	1	1	-	-	0	0	0	0	0	0	0	0	$V_{X1}+V_{X2}+V_{Y1}$

note: $V_a = V_{Y1}$; $V_b = V_{X2}$; $V_e = \frac{5}{6}V_{X1}$; $V_f = \frac{4}{3}V_{Y1}$; $V_g = \frac{V_{Y1}}{3}$

across switches S_{UX1}-S_{LX1}-S_{UY1}-S_{LY1}. When S_{UX1}-S_{LX1} are ON, $V_{JK} = V_{X1}$. Alternately, $V_{JK} = V_{Y1}$ when only S_{LY1} is ON and $V_{JK} = (V_{X1} + V_{Y1})$, the peak DC voltage, when S_{UX1}-S_{UY1} are ON. With all the switches of module turned OFF, $V_{JK} = 0$. This holds true for the proposed topology for all levels. V_{JK} is a DC staircase voltage applied at the input terminals of HBI. With only S_1-S_{11} of HBI ON, AC voltage levels of V_{X1}, V_{Y1} and $(V_{X1} + V_{Y1})$ are obtained. When only S_2-S_{22} of HBI are ON, $-V_{X1}$, $-V_{Y1}$ and $-(V_{X1} + V_{Y1})$ are obtained at the output.

B. Description of the Proposed 15-Level Modular RSC–MLI

Fig. 2(b) demonstrates the power circuit configuration for the proposed 15-level modular RSC-MLI made up with the addition of module X_2 to cascade connection of modules X_1 and Y_1. In addition to V_{X1} and V_{Y1}, a third DC source V_{X2} is included in the circuit. V_{X2} is connected across the input terminals of X_2, H_{TX2}-H_{BX2}. At the output side of SDVG, terminals C_{TX1} is connected to C_{TX2} through a series connection of diode D_U and switch S_U. C_{BY1} is directly connected to C_{TX2}. C_{TX1} forms the positive terminal of SDVG, denoted as terminal *J*. Similarly, C_{MX1}-C_{BY1} are connected to C_{BX2} through the series connection of switch S_L and diode D_L. In this topology, C_{MX2} forms the negative terminal SDVG, denoted by *K*. Moreover, from Fig. 2(b), it can also be observed that C_{BX1}-C_{TY1} are interconnected. S_U and S_L are specifically included to bypass a particular module. For example, when $V_{JK} = V_{X1}$ is to be implemented switch S_L is turned ON so that V_{X2} and V_{Y1} are not included in the circuit. Similarly, S_U is useful as turning it ON can result in the exclusion of V_{X1} and V_{Y1} from the circuit. By controlling the gate pulses to module X_2, $V_{JK} = V_{X2}$ can be obtained. With all the switches of the three modules turned OFF, $V_{JK} = 0$. The diodes, D_L and D_U ensure that the antiparallel diode of S_U and S_L do not conduct, and thereby prevent any undesirable operation. The switching table for this topology is displayed in Table II, where V_{SUX1}-V_{SLX1}-V_{SUY1}-V_{SLY1}-V_{SUX2}-V_{SLX2}-V_{SU}-V_{SL} are the corresponding voltages across switches S_{UX1}-S_{LX1}-S_{UY1}-S_{LY1}-S_{UX2}-S_{LX2}-S_U-S_L. SDVG generates the voltage levels V_{X1}, V_{Y1}, V_{X2}, $(V_{X1} + V_{Y1})$, $(V_{Y1} + V_{X2})$, $(V_{X1} + V_{X2})$, and $(V_{X1} + V_{X2} + V_{Y1})$. For these voltage levels, HBI correspondingly generates AC voltage with the levels of $\pm V_{X1}$, $\pm V_{Y1}$, $\pm V_{X2}$, $\pm(V_{X1} + V_{Y1})$, $\pm(V_{X1} + V_{X2})$, $\pm(V_{Y1} + V_{X2})$, and $\pm(V_{X1} + V_{X2} + V_{Y1})$. Further, 0 V is generated when all the switches of the module network are OFF. In the proposed topology, the increase in levels of voltages from seven to fifteen comes at the cost of one additional module and switches S_U and S_L.

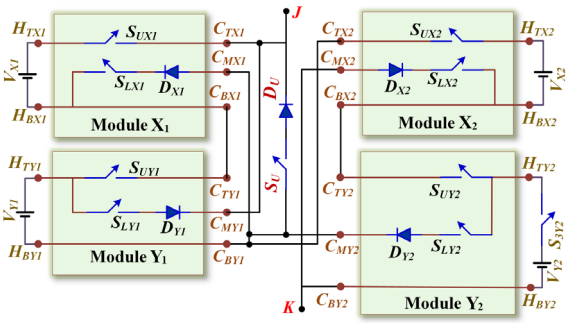


Fig. 3. Power circuit configuration of SDVG for the proposed 31-level modular RSC-MLI.

C. Description of the Proposed 31-Level Modular RSC–MLI

The power circuit configuration for the proposed 31-level modular RSC-MLI is illustrated in Fig. 3. One of the distinguishing features is that a series connection of DC source V_{Y2} and switch S_{3Y2} is connected across the input terminals H_{TY2}-H_{BY2} of module Y_2. At the output of SDVG, interconnection of C_{TX1}-C_{MY1} is connected to that of C_{MX1}-C_{BY1}-C_{MY2} through series connection of S_U-D_U. This interconnection forms the positive terminal of SDVG, indicated as terminal *J*. The negative terminal of SDVG, *K*, is formed by the interconnection of C_{MX2}-C_{BY2}.

In addition to the connections employed at the output

TABLE III
SWITCHING TABLE FOR THE PROPOSED 31-LEVEL MODULAR RSC-MLI

STATE/ MODE	Module								S_{3Y2}	S_U	Voltage Across Switches										V_{JK}
	X_1		Y_1		X_2		Y_2				S_{UX1}	S_{LX1}	S_{UY1}	S_{LY1}	S_{UX2}	S_{LX2}	S_{UY2}	S_{LY2}	S_{3Y2}	S_{16}	
	S_{UX1}	S_{LX1}	S_{UY1}	S_{LY1}	S_{UX2}	S_{LX2}	S_{UY2}	S_{LY2}			V_{SUX1}	V_{SLX2}	V_{SUY1}	V_{SLY1}	V_{SUX2}	V_{SLX2}	V_{SUY2}	V_{SLY2}	V_{S3Y2}	V_{SU}	
1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0
2	-	-	-	1	-	1	*D*	1	-	-	V_a	0	V_a	0	V_d	0	0	0	V_b	0	V_{Y1}
3	1	1	-	-	-	1	*D*	1	-	-	0	0	V_a	0	V_d	0	0	0	V_b	0	V_{X1}
4	1	-	1	-	-	1	*D*	1	-	-	0	0	0	0	V_d	0	0	0	V_b	0	V_3
5	-	-	-	-	-	-	-	1	1	1	V_e	V_g	V_f	V_a	V_b	0	V_b	0	0	0	V_{Y2}
6	-	-	-	1	-	-	-	1	1	-	V_e	0	V_a	0	V_b	0	V_b	0	0	0	V_5
7	1	1	-	-	-	-	-	1	1	-	0	0	V_a	0	V_b	0	V_b	0	0	0	V_6
8	1	-	1	-	-	-	-	1	1	-	0	0	0	0	V_b	0	V_b	0	0	0	V_7
9	-	-	-	-	1	1	-	-	-	1	V_e	V_g	V_f	V_a	0	0	V_b	0	0	0	V_{X2}
10	-	-	-	1	1	1	-	-	-	-	V_a	0	V_a	0	V_b	0	0	0	0	0	V_9
11	1	1	-	-	1	1	0	-	-	-	0	0	V_a	0	0	0	V_b	0	0	0	V_{10}
12	1	-	1	-	1	1	-	-	-	-	0	0	0	0	0	0	V_b	0	0	0	V_{11}
13	-	-	-	-	1	-	-	1	1	1	V_e	V_g	V_f	V_a	0	0	0	0	0	0	V_{12}
14	-	-	-	1	1	-	1	-	1	-	V_a	0	V_a	0	0	0	0	0	0	0	V_{13}
15	1	1	0	0	1	-	1	-	1	-	0	0	V_a	0	0	0	0	0	0	0	V_{14}
16	1	-	1	-	1	-	1	-	1	-	0	0	0	0	0	0	0	0	0	0	V_{15}

note: $V_3 = V_{X1} + V_{Y1}$; $V_5 = V_{Y1} + V_{Y2}$; $V_6 = V_{X1} + V_{Y2}$; $V_7 = V_{X1} + V_{Y2} + V_{Y1}$; $V_9 = V_{X2} + V_{Y1}$; $V_{10} = V_{X2} + V_{X1}$
$V_{11} = V_{X2} + V_{X1} + V_{Y1}$; $V_{12} = V_{X2} + V_{Y2}$; $V_{13} = V_{X2} + V_{Y2} + V_{Y1}$; $V_{14} = V_{X2} + V_{Y2} + V_{X1}$; $V_{15} = V_{X2} + V_{Y2} + V_{X1} + V_{Y1}$
$V_a = V_{Y1}$; $V_b = V_{Y2}$; $V_d = V_{X2}$; $V_e = \frac{5}{6}V_{X1}$; $V_f = \frac{4}{3}V_{Y1}$; $V_g = \frac{V_{Y1}}{3}$

side of SDVG in the proposed 15-level modular RSC-MLI, there exists an interconnection of C_{BX2} with C_{TY2}. As per the switching table shown in Table II, at the output of SDVG unit the possible voltage levels besides the one that can be generated with the 15-level topology are V_{Y2}, ($V_{X1} + V_{Y2}$), ($V_{X2} + V_{Y2}$), ($V_{Y1} + V_{Y2}$), ($V_{X1} + V_{Y1} + V_{Y2}$), ($V_{X1} + V_{X2} + V_{Y2}$), ($V_{X2} + V_{Y1} + V_{Y2}$), and ($V_{X1} + V_{X2} + V_{Y1} + V_{Y2}$). Corresponding AC voltages are obtained at the output of HBI.

D. Switching and Voltage Stress Analysis of Proposed RSC–MLIs

In addition to presenting the switching table for the proposed topology, this study uniquely contributes by incorporating a detailed analysis of the voltage stress across each switch during different voltage levels. The voltage stress data, coupled with the switching table, can have significant implications for both power systems and industrial applications, especially in the manufacturing of inverters for different voltage ratings.

The precise assessment of voltage stress on individual switches is important for ensuring reliable MLI operation, particularly as it scales to higher voltage ratings. A comprehensive understanding of switch voltage stress aids in the design of more resilient and optimized systems. The voltage stress across the switch pair of HBI (S_1-S_{11} and S_2-S_{22}) is not mentioned in the tables given in this section. Nevertheless, when a particular voltage level is applied and either switch pair (S_1-S_{11} or S_2-S_{22}) is in the OFF state, the voltage stress on that pair equals the magnitude of that particular voltage level and the voltage stress on the other pair which is in on-state will be zero. Moreover, with the help of Tables I, II, and III, the total standing voltage of the inverter can be found, which is calculated as part of the comparative analysis given in Section IV. Based on the presented discussion, the mathematical expressions for the number of levels are given as

$$N_{\text{level}} = 2^{(m+1)} - 1 \tag{1}$$

Similarly, for 7-level topology and 15/31 level topology, the number of switches, N_{switch}, can be given as per (2) and (3), respectively. In (2), four additional switches are needed for the H-Bridge inverter. Similarly, in (3), four additional switches and two bypass switches are needed.

$$N_{\text{switch}} = 2m + 4 \tag{2}$$
$$N_{\text{switch}} = 2m + 6 \tag{3}$$

The peak inverse voltage, *PIV* is given as

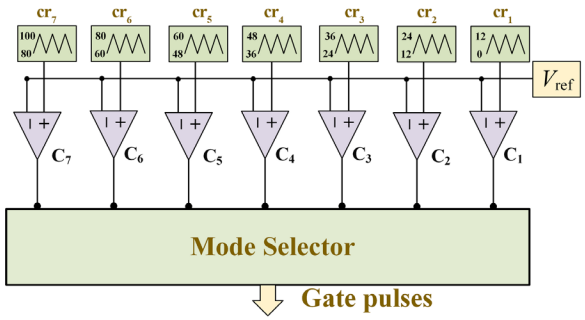


Fig. 4. PD-SPWM modulation technique for the proposed 15-level modular RSC-MLI.

$$PIV = \max\{V_{dc1}, V_{dc2}, \ldots, V_{dcn}\} \quad (4)$$

E. Gating Scheme for the Proposed Modular RSC–MLI

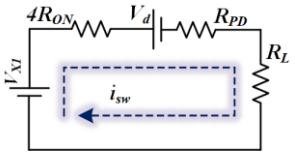
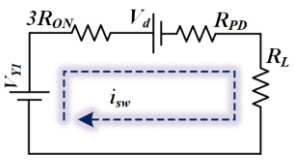
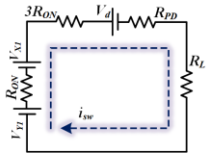
Phase disposition sinusoidal PWM (PD-SPWM), reported in [28], is employed for the proposed modular RSC-MLI. The only difference is that instead of PWM pins of DSP, digital output pins are employed for providing the gating signal to the gate driver. TMS320F28335 DSP has twelve PWM pins and eighty-eight digital output pins. Due to the provision of complementary output, in actual there are only six independent PWM pins. The complementary PWM pins are very much suitable for the 2-level voltage source inverters however, they may not be very much beneficial in case of the MLI. In MLI, for a particular switch, another switch with complementary conduction period may not exist. Hence, individual PWM signals are required.

With limited PWM pins available in a DSP processor, multiple DSPs may be needed. This poses a challenge in terms of increased complexity, component count, need of synchronization and communication between multiple DSPs, etc. Rather by operating the DSP at clock frequency, the digital output pins can be utilized for gate pulse generation. Fig. 4 shows the block diagram representation of PD-SPWM modulation technique for the proposed 15-level modular RSC-MLI. Comparators, C_1 to C_7, individually compare the reference signal, V_{ref}, with level shifted carrier signals, cr_1-cr_7. The outputs of the seven comparators are subsequently fed to the mode selector. The mode selector generates switching pulses for each of the twelve switches employed in the proposed 15-level modular RSC-MLI. Mode selector generates individual gate pulses based on the switching table provided in Table II. Similarly, mode selector can be designed for generating individual gate pulses for the proposed 7-level and 31-level MLI based on Table I and III, respectively.

III. Loss Analysis

The efficiency of MLI deteriorates mainly due to the conduction and switching losses occurring in the employed switches. The ON-state resistance of the IGBTs, R_{ON}, anti-parallel diode, R_{AD}, and power diode, R_{PD}, are mainly responsible

TABLE IV
Equivalent Circuits of the Proposed 7-Level Modular RSC-MLI

Equivalent Circuit	V_{JK} /Instantaneous Current/ Instantaneous Conduction Loss
	$\pm V_{X1}$ $\frac{V_{X1} - V_d}{4R_{ON} + R_{PD} + R_L}$ $i_{sw}^2(4R_{ON} + R_{PD})$
	$\pm V_{Y1}$ $\frac{V_{Y1} - V_d}{3R_{ON} + R_{PD} + R_L}$ $i_{sw}^2(3R_{ON} + R_{PD})$
	$\pm(V_{X1} + V_{Y1})$ $\frac{V_{X1} + V_{Y1} - V_d}{4R_{ON} + R_L}$ $i_{sw}^2(4R_{ON})$

for the conduction losses [29]. For determining conduction losses occurring in the proposed 7-level modular RSC-MLI, equivalent circuit is developed for each switching state as shown in Table IV. The conduction and switching losses for the proposed MLI are mathematically expressed by (5)-(13), where i indicates the instantaneous current flowing through the equivalent circuit, P_{Ci} and P_{Ca} indicate instantaneous and average conduction loss for the particular switching state, R_L is the load resistance, t_n is the time period for which the nth switch state is active, and T is the total time period for one cycle. The total conduction loss over one cycle, P_{CiT}, can be computed as the summation of P_a over the entire cycle. P_{CiT} can be mathematically expressed as in (5), where S is the switching state [29].

Switching losses, other major detrimental factor for efficiency, are caused due to the energy consumed in turning a switch ON or OFF. When the switch is in a state of partial conduction, neither completely turned ON nor OFF, leading to voltage and current overlap within the switch. This results in switching losses. For a switch, the average value of switching losses during the turn ON period, P_{swON}, can be mathematically expressed as shown in (6), [17], (7), (8), and (9), where f_{sf} is switching frequency, t_{ON} is period of transition that starts at t_a and ends at t_b, v_{SwON} and i_{SwON} are the switch voltage and current during t_{ON}, V_{swOFF} is the switch voltage before t_a, I_{swON} is the switch current after t_b, and V' is the voltage across the switch when it is in OFF state.

Similarly, the switching losses during the transition from turn ON to OFF, P_{swOFF}, can be mathematically expressed by (10)-(11), where t_{OFF} is period of transition that starts at t_a' and ends at t_b', v_{SwOFF} and i_{SwOFF} are the switch voltage and current during t_{OFF}, V_{swON} is the switch voltage before t_a', and i'' is the

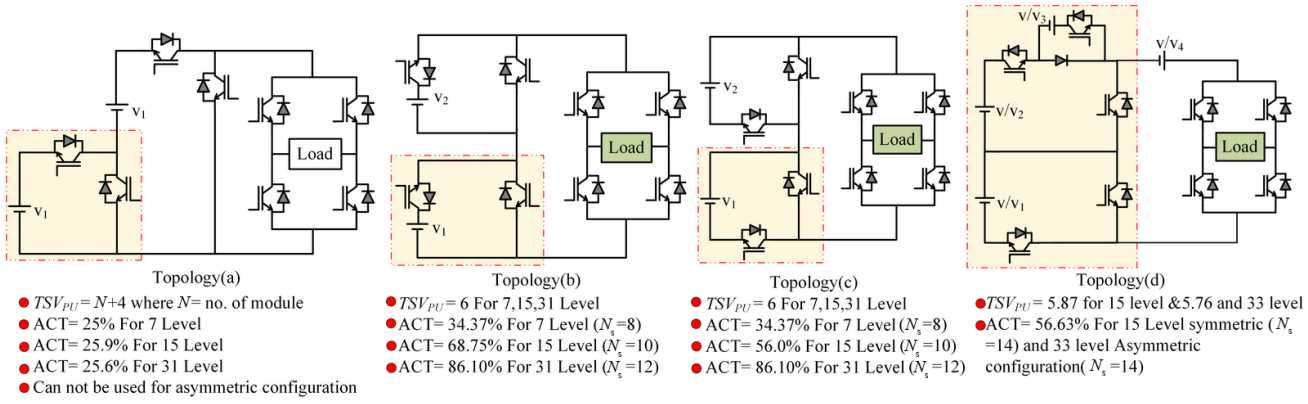


Fig. 5. Four different MLI topologies similar to the proposed topology.

TABLE V
COMPARISON OF THE PROPOSED MODULAR RSC-MLI WITH EARLIER REPORTED TOPOLOGIES

PT	N_L	N_S	N_{GD}	N_D	N_C	N_{DC}	Modular	TSV_{PU}
[30]	31	14	14	2	4	2	Yes	6.0
[31]	31	18	18	2	4	2	Yes	5.6
[32]	31	16	16	2	4	2	Yes	5.6
PT	**31**	**14**	**14**	**4**	**0**	**4**	**Yes**	**5.8**
[33]	15	8	8	8	0	4	Yes	7
[34]	15	16	16	0	0	3	Yes	1.9
[35]	15	12	11	0	0	4	No	5.1
PT	**15**	**12**	**12**	**3**	**0**	**3**	**Yes**	**4.7**
[36]	7	12	11	0	2	1	No	5.3
[37]	7	8	8	0	0	2	No	5.3
[19]	7	11	11	3	3	1	yes	5.0
[38]	7	13	13	4	3	1	yes	5.7
PT	**7**	**8**	**8**	**2**	**0**	**2**	**Yes**	**4.6**

switch current during ON state. The leakage current of the switch is neglected as it has significantly lower magnitude than I_{swON}.

$$P_{CiT} = \sum_{S=0}^{4} P_{Ca}(S) \tag{5}$$

$$P_{swON} = f_{sf} \int_{t_0}^{t_s} v_{SwON}(t)\, i_{SwON}(t)\, dt \tag{6}$$

$$P_{swON} = f_{sf}\{m_i t_{ON}^2 (V' - 2m_v t_a/2)\} + f_{sf}\{(m_v m_i t_a^2 - V' t_a) m_i t_{ON}\} - f_{sf}\{(m_v m_i t_{ON}^3/3\} \tag{7}$$

$$m_v = V_{swOFF}/t_{ON} \tag{8}$$

$$m_i = I_{swON}/t_{ON} \tag{9}$$

$$P_{swOFF} = f_{sf} \int_0^{t_{OFF}} v_{SwOFF}(t)\, i_{SwOFF}(t) dt \tag{10}$$

$$P_{swOFF} = f_{sf}\{m_v' t_{OFF}^2 (i'' - 2m_i')/2\} + f_{sf}\{(m_i' t_a^2 + i'' t_a') m_v' t_{OFF}\} - f_{sf}\{(m_v' m_i' t_{OFF}^3/3\} \tag{11}$$

$$m_v' = V_{swOFF}/t_{OFF} \tag{12}$$

$$m_i' = I_{swON}/t_{OFF} \tag{13}$$

IV. COMPARATIVE ANALYSIS

Table V presents a comparison between the proposed topology and the earlier reported ones in terms of the number of levels, N_L, number of switches, N_S, number of gate-drivers, N_{GD}, number of diodes, N_D, number of capacitors, N_C, number of DC sources, N_{DC}, and total standing voltage per unit, TSV_{PU}. In this table, PT indicates the proposed topology. Additionally, the comparative analysis also includes whether the topology is modular or not. Moreover, in Table V, the topologies are clubbed together based on N_L.

From the comparison presented, for generating 31-level [30]–[32] make use of two DC sources and four capacitors. Reference [30] uses a lesser number of switches than [31] and [32]. The proposed topology without the aid of any capacitor produces 31 levels. On the other hand, to obtain a 15-level output voltage, [33] makes use of the least number of switches but TSV_{PU} is very high. Reference [34] makes use of a higher number of switches but it's TSV_{PU} is minimum. On the other hand, the topology reported in [35] requires one less switch as compared to the proposed topology for generating 15 levels. However, the topology from [35] needs four DC sources for the same voltage levels. Also, this topology is not modular. Topologies presented in [19], [36]–[38], produce 7-level output voltages. Out of these topologies, only the topologies presented in [19] and [38] are modular. However, they require a higher number of switches and three capacitors. References [36], [37] are having the same TSV_{PU}. However, the topology reported in [36] requires an additional four switches and three capacitors as compared to that reported in [37], which makes use of only two DC sources and eight switches. However, the TSV_{PU} for switches in the topology presented in [37] is higher than the proposed topology. The proposed topology necessitates fewer switches and avoids using any passive elements, which enhances compatibility and reduces the cost of the inverter.

Fig. 5 depicts four different MLI topologies, a, b, c, and d, presented in [39], [40], [41], and [42], respectively. These

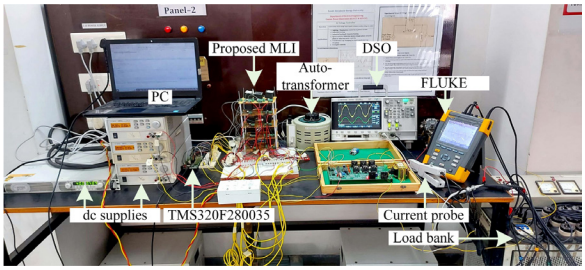


Fig. 6. Hardware set-up for the proposed modular RSC-MLI.

four topologies seem to be similar to the proposed topology. Topologies a, b, c, d, and the proposed topology are compared based on the average conduction time (ACT) of each switch during one output AC voltage. Higher ACT results in increased conduction losses and consequently increased heating of switches. This can cause thermal stress and reliability issues. ACT for proposed topology is 34.37%, 57.16%, and 84.17% for 7, 15, and 31 levels of output voltage, respectively. Topology a has a lesser value of ACT, however, TSV_{PU} is higher. TSV_{PU} increases as the number of modules increase with the number of levels. Also, as only symmetric configuration is possible in Topology a, adding one module (comprising of DC source and two switches) will result in a mere increment in the number of output voltage levels by two. Topologies b and c require the same number of components to produce the same number of voltage levels. However, due to the different placement of switches, ACT is different though TSV_{PU} is the same. Topology d has lesser TSV_{PU} and ACT but it makes use of a higher number of switches and DC sources. The proposed MLI topology may require more switches compared to Topologies b and c, but it has a lesser value of TSV_{PU}.

TSV and switch count are important indices that directly or indirectly relate to the total cost of design and implementation. Usually, lower TSV indicates switches with lower voltage withstand capacity can be utilized and cost can be reduced and vice versa. Likewise, reducing the switch count for the same number of levels reduces total cost. However, in some cases, TSV will be higher, which increases the cost per switch. Topologies b and c have a lower switch count than the proposed MLI. However, their TSV is higher than the proposed topology. On the other hand, topology presented in d involves lower TSV than the proposed MLI but at the cost of increased switch count.

V. Experimental Results and Discussions

For experimental validation, laboratory prototype model for the proposed 7-level, 15-level, and 31-level MLI topology was developed. Fig. 6 shows photograph of the developed experimental prototype. For the 7-level MLI, the two employed isolated DC power supplies are configured such that V_{X1} = 40 V and V_{Y1} = 30 V. Similarly, for 15- level MLI, the three isolated dc power supplies are required. They are configured such that V_{X1} = 35 V, V_{Y1} = 25 V, and V_{X2} = 15 V. In case of 31-level MLI, four isolated DC power supplies are configured

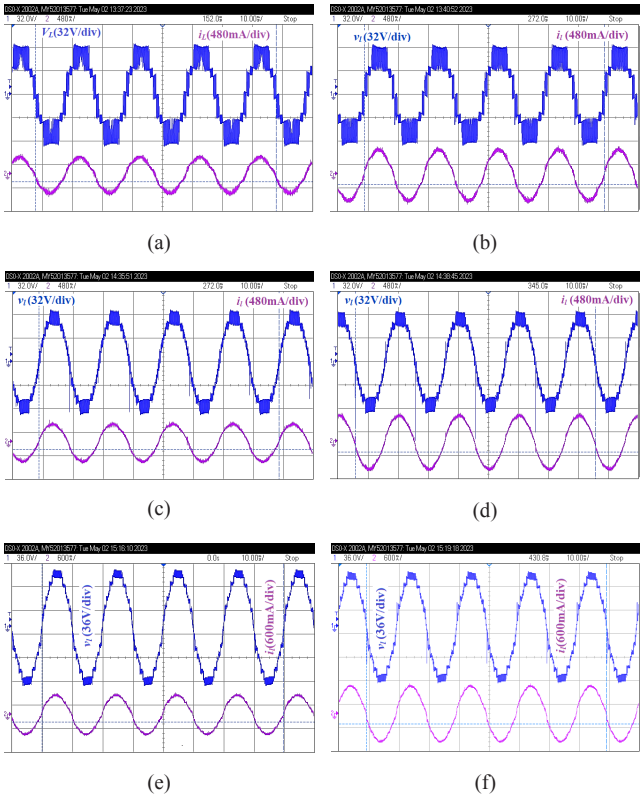


Fig. 7. Performance of (a) 7-level MLI with Load-I, (b) 7-level MLI with Load-II, (c) 15-level MLI with Load-I, (d) 15-level MLI with Load-II, (e) 31-level MLI with Load-I, and (f) 31-level MLI with Load-II under steady-state.

so that V_{X1} = 40 V, V_{Y1} = 25 V, V_{X2} = 20 V, and V_{Y2} = 10 V. The gate driver circuit is implemented using IC TLP250. To generate gate pulses, a level-shifted PWM technique is implemented with TMS320F28335 DSP. Digital storage oscilloscope Agilent-make DSO-X-2002A is employed for recording the waveforms. Power quality analyzer PHA5850 is used for THD measurement. Also, Load-I (comprising of series combination of 165 Ω resistor and 20 mH inductor) and Load-II (comprising of series combination of 110 Ω resistor and 20 mH) are used in the study.

Fig. 7 illustrates the steady-state performance of the proposed 7-level, 15-level and 31-level modular RSC-MLI topology for Load–I and Load–II. In this case, the modulation index is 0.95. The steady-state performance of 7-level modular RSC-MLI for Load–I and Load–II are shown in Fig. 7(a) and (b), respectively. For this 7-level topology, V_{X1} = 40 V and V_{Y1} = 30 V. When supplying Load–I, the rms value of load voltage, v_l, is measured as 45.39 V. Also, the rms value of load current, i_l, is recorded as 0.264 A. %THD for v_l and i_l are observed to be 6.5 and 5.0. In this case, ±28.58, ±36.20, ±66.68 and 0 V are observed to be the seven levels of v_l. When the load is increased from Load–I to Load–II, under the new steady-state, the rms value of i_l increases from 0.264 A to 0.378 A. Now, v_l is observed to have a rms value of 43.96 V.

Fig. 7(c) and (d) show the steady-state performance of 15-level modular RSC-MLI for Load–I and Load–II, respectively. Similar to the earlier case, the modulation index

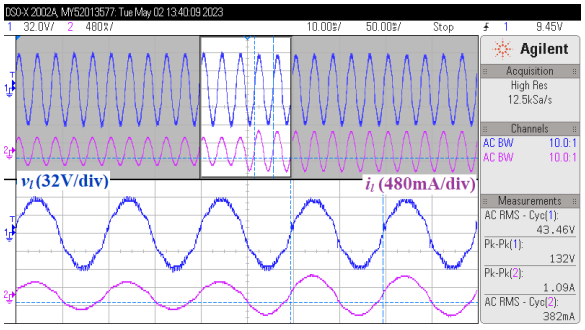


Fig. 8. Performance of 7-level MLI during change in load from Load–I to Load–II.

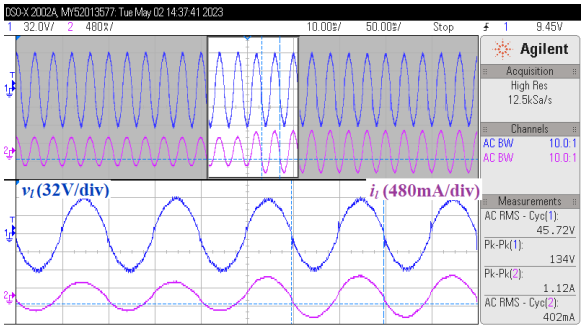


Fig. 9. Performance of 15-level MLI during change in load from Load–I to Load–II.

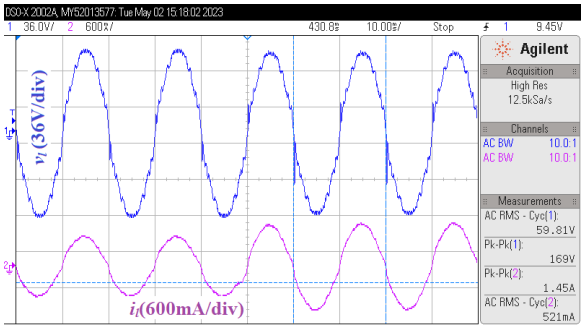


Fig. 10. Performance of 31-level MLI during the change in load from Load–I to Load–II.

is 0.95. For 15-level modular RSC-MLI feeding Load–I, the rms values of v_l and i_l are measured as 46.68 V and 0.278 A, respectively. The corresponding %THD is found to be 5.7 and 4.9. It is to be noted that in this case V_{X1} = 35 V, V_{Y1} = 25 V, and V_{X2} = 15 V. Now with the increase in load from Load–I to Load–II, the rms value of i_l at the new steady-state is 0.399 A. Consequently, the rms value of v_l is reduced to 45.48 V. In v_l, ±12.6, ±22.5, ±30.6, ±34.2, ±43.2, ±54.3, ±72 and 0 V are observed as the fifteen levels.

The steady-state performance of 31-level modular RSC-MLI for Load–I and Load–II are respectively demonstrated in Fig. 7(e) and (f). As for the other topologies, the modulation index is 0.95. For 31-level modular RSC-MLI feeding Load–I, the measurements show v_l and i_l to have the rms values of 60.92 V and 0.360 A, respectively. Correspondingly, %THD is measured to be 5.2 and 4.5. As mentioned earlier, for this topology V_{X1} = 40 V, V_{Y1} = 25 V, V_{X2} = 20 V, V_{Y2} = 10 V. The rise in load from Load–I to Load–II leads to an increased steady-state rms value of i_l. Compared to the rms value of 0.36 A, now the rms value of i_l is observed as 0.514 A. The rms value of v_l is measured as 58.79 V. The dynamic performance of the proposed topology has been evaluated to verify its ability to function under sudden changes in loading conditions. The dynamic performance of the proposed 7-level, 15-level and 31-level modular RSC-MLI is analyzed under the change in load from Load–I to Load–II.

Figs. 8 to 10 illustrates v_l and i_l for 7-level, 15-level and 31-level modular RSC-MLI during change in load from Load–I to Load–II. For all the three topologies, the increase in load from Load–I to Load–II results in increase in i_l. However, with the increase in i_l, the on-state voltage drop across the switches increases, which results in minor reduction in v_l. This can be observed in case of all the three proposed MLI topologies. Thus, any increment in i_l would results in increased on-state voltage drop across the switches and consequent reduction in rms value of v_l. The reverse is also true. Further, Figs. 8-10, confirm the satisfactory operation of the proposed topologies during the load change, with no abnormal behavior observed.

VI. Conclusion

In this paper, a modular RSC-MLI for 7-level, 15-Level, and 31-level output voltage is proposed. A discussion on modules developed, the power structure of the proposed MLI topologies, the theory of operation, and the primary approach for modulation are presented. The formulation of switch losses is also presented. Phase disposition level-shifted PWM technique is utilized for gate pulse generation. Limited PWM pins are available in a DSP, which may not suffice for an MLI. To overcome this, the gating signals are generated at the digital output pins, which are in substantially higher numbers, are used instead of the PWM pins. Thereby, the need to use multiple DSPs and associated complexity is avoided. The modular construction of the proposed topology easily allows for increasing the levels by adding modules. The merits of the proposed topology are highlighted through a comparative analysis. From the comparative analysis, inference can be drawn that the proposed modular RSC-MLI topologies can provide staircase voltage with higher power quality while simultaneously decreasing the number of components, the total cost, and higher compatibility as no passive elements are involved. Finally, the proposed 7-level, 15-Level, and 31-level modular RSC-MLI topologies are assessed experimentally under steady-state and dynamic load change to validate the presented theory.

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