

Twelve-Step Voltage Source Inverter: A Three-Phase Six-Levels Inverter Using Planar Transformers

Haitham KANAKRI, Euzeli Cipriano DOS SANTOS JR., and Maher RIZKALLA

Abstract—Multi-level inverters (MLIs) are becoming increasingly popular in high-speed motor drive systems for modern electric aircraft applications. However, two significant limitations are associated with current MLIs technology: (1) the high switching losses due to the high carrier switching frequency and (2) the complex modulation schemes required to maximize the DC source utilization. Consequently, the development of new topologies to mitigate these limitations is imperative for the rapid advancement of future electric aircraft systems. This paper introduces a six-level twelve-step inverter (TSI) that utilizes twelve switches and three planar high-frequency transformers. Implementing the proposed configuration ensures maximum DC source utilization, with a peak phase voltage of $5V_{dc}/3$. The proposed solution presents less semiconductor losses than the conventional MLIs, surpassing conventional MLIs, associated with neutral point clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB). Experimental results demonstrate the TSI's operation under static and dynamic conditions and its capability to function in three different modes: three-step, six-step, and twelve-step operations. The paper also offers a comprehensive design of the proposed planar transformer, supported by theoretical analysis, finite element analysis (FEA), and experimental validation.

Index Terms—Finite element analysis (FEA), multilevel inverters, planar transform design, six-level output voltage, three-phase inverter, twelve-step inverter.

NOMENCLATURE

A_c	Transformer's core cross sectional area (cm^2).
A_t	PCB copper trace cross-sectional area in (mils^2).
$A_{t[\text{cm}^2]}$	PCB copper trace cross-sectional area in (cm^2).
A_p	Area product (cm^4).
B_m	Maximum flux density (T).
f	Operating frequency in (Hz).
i_1	Phase-u load current.
i_2	Phase-v load current.
i_3	Phase-w load current.

J	Current density in (A/cm^2).
k	Constant related to conductor current density specified by IPC-221A standard for outer and inner PCB layers.
K_f	Waveform coefficient.
K_u	Transformer window utilization factor.
n	Transformer turns ratio.
P_o	Transformer output power.
P_t	Transformer total handling power.
S_x	Switch x , where $x = \{1, a, 2, b, 3, c\}$.
\bar{S}_x	Complementary of switch x .
TSI	Twelve-step inverter.
V_{dc}	DC input voltage.
v_{un}	Phase u to neutral n voltage.
v_{vn}	Phase v to neutral n voltage.
v_{wn}	Phase w to neutral n voltage.
v_{ac}	The primary voltage of transformer-1.
v_{ba}	The primary voltage of transformer-2.
v_{cb}	The primary voltage of transformer-3.
v'_{ac}	The secondary voltage of transformer-1.
v'_{ba}	The secondary voltage of transformer-2.
v'_{cb}	The secondary voltage of transformer-3.
W_a	Transformer core window area (cm^2).
η	Transformer efficiency (%).
ΔT	Temperature rise ($^\circ\text{C}$).
Φ	Magnetic flux (Weber).

I. INTRODUCTION

THE growing interest in DC-AC converters for applications that demand minimal harmonic distortion has prompted engineers to operate at higher switching frequencies [1]. However, the selection of an operating frequency is notably constrained by the specific type of switching device employed within a given application, such as MOSFETs or IGBTs. Indeed, increased switching frequencies can lead to higher losses, consequently placing restrictions on the overall system performance. Multilevel PWM inverters (MLI) are commonly employed in applications requiring minimal harmonic distortion, including motor drive systems and grid-tie inverters [2]. Common topologies include neutral-point clamped (NPC) [3], flying capacitor (FC) [4]–[6] and cascaded multi-cells (CHB) configurations with separate DC sources [1], [4]. While PWM inverters can produce an output current that closely resembles a sine wave with minimal harmonic distortion [7], [8], they come with some drawbacks. These include complex

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strategies for an optimized PWM and converter design in order to reduce the switching losses [9], [10], increased weight and volume for heat sink requirements [11], acoustic noise [12], and issues related to electromagnetic interference (EMI) [12], [13]. Additionally, PWM inverters suffer from the use of multiple DC-link capacitors, particularly in the case of the NPC topology. When only one DC source is available, without appropriate modulation and control strategies, there wouldn't be assurance that the capacitor voltages will reach the desired levels, potentially leading to asymmetric output voltages [2]. Consequently, the use of feedback controllers with specific PWM approaches becomes necessary, thereby increasing the complexity of the system [2].

Due to the substantial demand for high-power inverters with medium voltage levels, there has been rapid evolution in the need for new MLIs with reduced switching losses [14]. MLIs can be categorized into two types: 1) carrier-based variable duty cycle PWM inverters, such as the NPC, FC, and CHB inverters [1], and 2) fixed duty cycle PWM inverters, such as the six-step inverter [15]. Although the six-step inverter may introduce higher low-frequency distortions, its low operating frequency becomes appealing when the size and volume of the controlled voltage source become critical factors [15]. For instance, in aerospace applications, the electrically powered high-lift system that uses high-speed permanent magnet motor of 60000 RPM connected to the air compressor and integrated into the aircraft wings structure [16]–[18]. Moreover, these applications prioritize high power density, with typical power/mass ratios reaching 4 kW/kg [19].

The six-step inverter refers to a three-phase DC-AC converter built using six IGBTs operating with a 50% duty cycle, does not have high-frequency variable duty-cycle PWM gate signals. The authors in [15] proposed a control scheme for the six-step operation of permanent magnet synchronous machine (PMSM) with current control, ensuring its enhanced dynamic performance. Similarly, the authors in [20] utilized squarewave inverter operation for a three-phase motor drive system, in order to increase voltage utilization and achieve higher efficiency compared to that of the PWM operation [21]. The authors of [22] showed that the six-step operation can achieve a higher power density and lower switching frequency compared to PWM operation. In [13], the authors proposed an 18-step inverter, comprising 12 IGBTs, 36 power diodes, and three DC link capacitors to achieve an output voltage of seven levels. However, the high number of components and the adoption of a modified PWM scheme to further decrease the low-order harmonics in the output current elevate the complexity of control. Although this topology offers the advantage of a single DC source, it still uses multiple DC link capacitors, leading to increased system costs and size.

Transformer based multi-level inverters (Tr-MLI) [23] are commonly utilized to increase voltage levels for high-power and high-voltage applications. They offer capacitor free and diode-free topologies, facilitating voltage boosting with straight forward control [24]. The multilevel cascaded H-bridge inverter, proposed in [25] for medium-voltage applications,

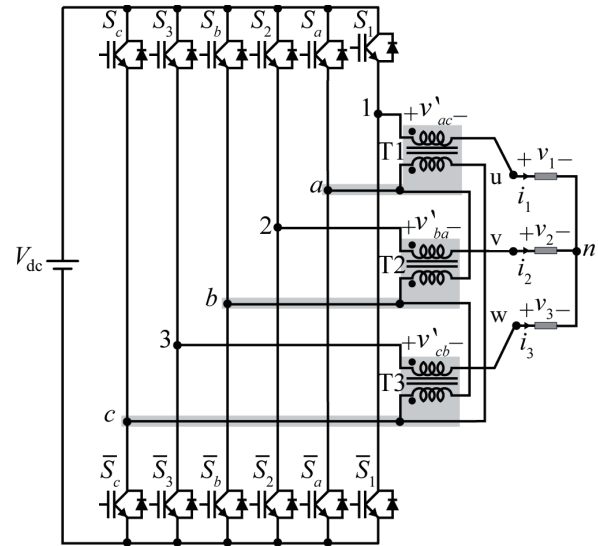


Fig. 1. The proposed twelve-step voltage source inverter (TSI).

improves the system efficiency and reduces component count. Tr-MLIs are preferred in motor drive applications due to their use of a single DC source, mitigating the power balance issues inherent in conventional MLIs [26]. The emergence of planar magnetic technology has enabled the incorporation of multiple transformers in converter structures without compromising overall converter size and efficiency [27]. Indeed, planar magnetic technology shows promise in meeting the escalating demands for high-power density and low-profile converters [28]. Various applications, such as modern electric aircraft [29], automotive industry such as electric vehicles, servers, aerospace, and military applications [28], integrate planar transformers in their structures to achieve high-power density and streamlined profile products. A twelve-step three-phase six-level inverter (TSI) published by the authors of this work is introduced in [30]. Fig. 1 illustrates the proposed topology. Notably, the proposed configuration offers several key features: (1) complete elimination of the DC link capacitors, resolving voltage balance issues, (2) utilization of a single DC source, (3) reducing inverter semiconductor losses, (4) simplifying switching and control algorithm, and (5) reducing the overall size of the inverter due to the use of high-frequency planar transformers. Additionally, the proposed topology provides the highest number of levels at the output voltage per number of DC sources ($L / S_{dc} = 6 / 1$) among all other MLI topologies. It stands as a candidate for high-speed motor drive systems, particularly with permanent magnet synchronous machines (PMSM) when operating at very high frequencies, where the use of PWM MLIs is constrained by high-switching losses.

After this introduction, Section II highlights the novelty and applications of the proposed topology, Section III presents the modeling and operating principles, Section IV discusses the design of the proposed planar transformers, Section V provides detailed simulations and experimental results, Section VI presents the efficiency analysis and comparison with the current MLIs topologies, and finally, Section VII concludes the proposed work.

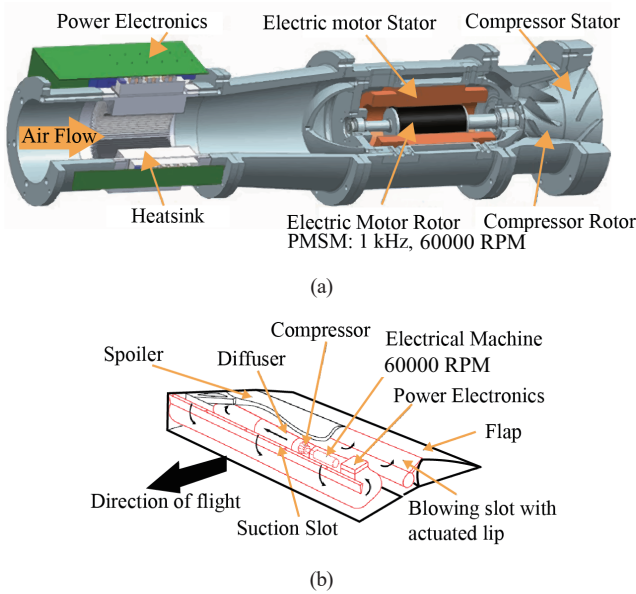


Fig. 2. (a) Integrated prototype of electrically powered high-lift system adapted from [12]. (b) Drawing shows the power active high-lift system integrated into a wing of an aircraft, adapted from [14].

II. NOVELTY AND APPLICATIONS OF THE PROPOSED TOPOLOGY

While transformer-based inverters are a well-established technology [31], the proposed configuration stands out for its ability to operate over a wide range of fundamental frequencies. The innovative design of the high-frequency planar transformer enables the operation at exceptionally high efficiency. This transformer design incorporates a balanced winding configuration, winding with simple construction, and reduces the construction cost. Applications such as electrically powered high-lift systems in aircrafts are particularly suitable for the proposed topology. Electric aircraft utilizes high-speed motors to drive aircraft compressors, as depicted in Fig. 2(a) [17], [18]. High-speed permanent magnet synchronous machines (PMSM) are typically integrated into the aircraft wings and compressor assemblies, operating at high fundamental frequencies exceeding 60000 RPM [17], [18]. The use of traditional MLIs for such applications is limited due to high switching losses. The number of switching components for a typical MLI topology increases with the number of levels, consequently increasing the size and cost of the drive system. This limitation is particularly critical for electric aircraft applications, as the power electronics drive system must be integrated into the aircraft wings, as shown in Fig. 2(b). Some key features of the proposed configuration include uniform voltage levels at the output and the equivalence of phase and line voltages in terms of the number of levels. Moreover, the phase voltages surpass the DC-link voltage, which allows higher current and consequently increases motor torque.

III. MODELING AND OPERATION OF THE PROPOSED TWELVE-STEP INVERTER (TSI)

The inverter, depicted in Fig. 3(a), is comprised of twelve

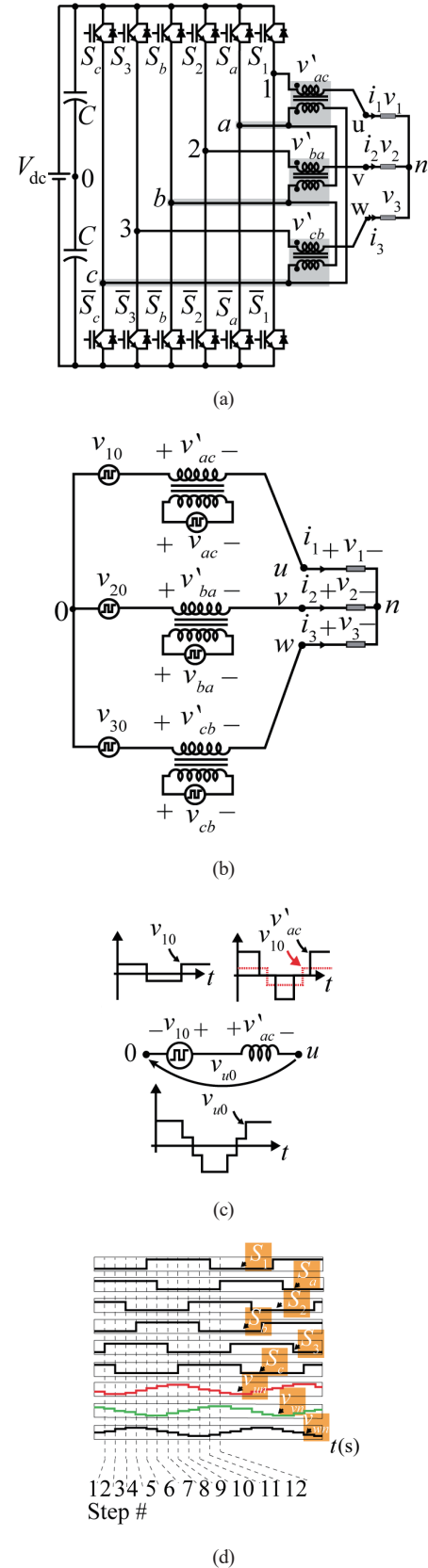


Fig. 3. (a) Proposed topology of twelve-step three-phase six-level inverter (TSI), the DC-link capacitors C are utilized exclusively for modeling purposes and are not required for the system's operation. (b) TSI equivalent circuit. (c) TSI main voltages for phase-u. (d) Three-phase six-level phase load voltage waveform in twelve-steps.

TABLE I
TABLE OF VARIABLES INDICATING THE OPERATION OF THE PROPOSED
TOPOLOGY IN TWELVE STEPS

Step	S_1	S_2	S_3	S_4	S_5	S_6	Starting	Ending
1	0	1	1	0	0	1	0°	30°
2	0	1	1	0	1	1	30°	60°
3	0	1	1	0	1	0	60°	90°
4	0	1	0	0	1	0	90°	120°
5	0	1	0	1	1	0	120°	150°
6	1	1	0	1	1	0	150°	180°
7	1	0	0	1	1	0	180°	210°
8	1	0	0	1	0	0	210°	240°
9	1	0	0	1	0	1	240°	270°
10	1	0	1	1	0	1	270°	300°
11	1	0	1	0	0	1	300°	330°
12	0	0	1	0	0	1	330°	360°

insulated gate bipolar transistors (IGBTs), twelve freewheeling diodes, three high-frequency planar transformers, and a single DC-link voltage source. Notably, the design does not necessitate any additional voltage divider capacitors. The DC-link capacitors shown in Fig. 3(a) are utilized exclusively for modeling purposes and are not required for the system's operation. The primary side of the transformers is connected in delta arrangement, while the secondary side is linked to the Y-load and inverter legs. The innovative topology produces six distinctive levels at the output voltage, namely, $5V_{dc}/3$, $4V_{dc}/3$, $V_{dc}/3$, $-V_{dc}/3$, $-4V_{dc}/3$, and $-5V_{dc}/3$, resulting in a comprehensive twelve-step waveform, as illustrated in Fig. 3(d). Remarkably, the peak-to-peak amplitude of the output phase voltage is $3.33V_{dc}$, a significant increase when compared to the conventional six-step inverter with a peak-to-peak phase voltage of $1.33V_{dc}$. For further clarity, the equivalent circuit of the TSI topology is illustrated in Fig. 3(b). The analysis of the six-level load phase voltage v_{un} based on the proposed switching pattern is presented in Table I and Table II. Table II shows the switching pattern to obtain the six-level output phase voltage. Table I also details the switching pattern of the twelve-step action used to generate the six-level waveform. The load phase voltages are 120° apart. The step size of each twelve-step action is 30°, for example, step-1 is located between 0° and 30°, step-2 is located between 30° and 60° and so on till step-12 which is located between 330° and 360°. The resultant pole voltages applied to the load are derived as follows:

$$v_{10} = v'_{ac} + v_{un} + v_{n0} \quad (1)$$

$$v_{20} = v'_{ba} + v_{vn} + v_{n0} \quad (2)$$

$$v_{30} = v'_{cb} + v_{wn} + v_{n0} \quad (3)$$

where the voltages v'_{ac} , v'_{ba} , v'_{cb} are the secondary voltages of the transformers connected to phase u, v, and w, respectively. If the number of turns of each transformer is n , (1)-(3) become:

$$v_{10} = nv_{ac} + v_{un} + v_{n0} \quad (4)$$

$$v_{20} = nv_{ba} + v_{vn} + v_{n0} \quad (5)$$

$$v_{30} = nv_{cb} + v_{wn} + v_{n0} \quad (6)$$

where $v_{ac} = v_{a0} - v_{c0}$, $v_{ba} = v_{b0} - v_{a0}$, $v_{cb} = v_{c0} - v_{b0}$. Notice that

TABLE II
THE PHASE AND LINE VOLTAGES OF THE PROPOSED TOPOLOGY IN TWELVE STEPS

Step	v_{un}	v_{vn}	v_{wn}	v_{uv}	v_{vw}	v_{wu}
1	$-V_{dc}/3$	$(5V_{dc})/3$	$-(4V_{dc})/3$	$-3V_{dc}$	$2V_{dc}$	V_{dc}
2	$-(2V_{dc})/3$	$(4V_{dc})/3$	$-(2V_{dc})/3$	$-3V_{dc}$	V_{dc}	$2V_{dc}$
3	$-(5V_{dc})/3$	$(4V_{dc})/3$	$V_{dc}/3$	$-2V_{dc}$	$-V_{dc}$	$3V_{dc}$
4	$-(4V_{dc})/3$	$(2V_{dc})/3$	$(2V_{dc})/3$	$-V_{dc}$	$-2V_{dc}$	$3V_{dc}$
5	$-(4V_{dc})/3$	$-V_{dc}/3$	$(5V_{dc})/3$	V_{dc}	$-3V_{dc}$	$2V_{dc}$
6	$-(2V_{dc})/3$	$-(2V_{dc})/3$	$(4V_{dc})/3$	$2V_{dc}$	$-3V_{dc}$	V_{dc}
7	$V_{dc}/3$	$-(5V_{dc})/3$	$(4V_{dc})/3$	$3V_{dc}$	$-2V_{dc}$	$-V_{dc}$
8	$(2V_{dc})/3$	$-(4V_{dc})/3$	$(2V_{dc})/3$	$3V_{dc}$	$-V_{dc}$	$-2V_{dc}$
9	$(5V_{dc})/3$	$-(4V_{dc})/3$	$-V_{dc}/3$	$2V_{dc}$	V_{dc}	$-3V_{dc}$
10	$(4V_{dc})/3$	$-(2V_{dc})/3$	$-(2V_{dc})/3$	V_{dc}	$2V_{dc}$	$-3V_{dc}$
11	$(4V_{dc})/3$	$V_{dc}/3$	$-(5V_{dc})/3$	$-V_{dc}$	$3V_{dc}$	$-2V_{dc}$
12	$(2V_{dc})/3$	$(2V_{dc})/3$	$-(4V_{dc})/3$	$-2V_{dc}$	$3V_{dc}$	$-V_{dc}$

the load phase voltages can be written in terms of the pole voltages v_{10} , v_{a0} , v_{20} , v_{b0} , v_{30} , and v_{c0} . Then the phase load voltages become:

$$v_{un} = v_{10} - nv_{ac} - v_{n0} \quad (7)$$

$$v_{vn} = v_{20} - nv_{ba} - v_{n0} \quad (8)$$

$$v_{wn} = v_{30} - nv_{cb} - v_{n0} \quad (9)$$

For a three-phase balanced system and assuming, $n = 1$,

$$v_{n0} = \frac{1}{3}(v_{10} + v_{20} + v_{30}) \quad (10)$$

Substituting (10) in (7)-(9), it yields:

$$v_{un} = \frac{2}{3}v_{10} - v_{a0} - \frac{1}{3}v_{20} - \frac{1}{3}v_{30} + v_{c0} \quad (11)$$

$$v_{vn} = \frac{2}{3}v_{20} - v_{b0} - \frac{1}{3}v_{30} - \frac{1}{3}v_{10} + v_{a0} \quad (12)$$

$$v_{wn} = \frac{2}{3}v_{30} - v_{c0} - \frac{1}{3}v_{10} - \frac{1}{3}v_{20} + v_{b0} \quad (13)$$

Since each pole voltage is defined by the state of the switches S_j (with $j = 1, a, 2, b, 3, c$) following $v_{j0} = (2S_j - 1)(V_{dc}/2)$, the connection of the high-frequency transformers allows each pole voltage seen by the three-phase load (v_{u0} , v_{v0} , v_{w0}) to be:

$$v_{u0} = v_{10} + v_{c0} - v_{a0} \quad (14)$$

$$v_{v0} = v_{20} + v_{a0} - v_{b0} \quad (15)$$

$$v_{w0} = v_{30} + v_{b0} - v_{c0} \quad (16)$$

It is possible to select the gate signals for each phase so that the voltages v_{u0} , v_{v0} , v_{w0} have four levels as presented schematically in Fig. 3(c). Finally, the line voltages can be given in terms of the pole voltages as follows in (17)-(19):

$$v_{uv} = v_{10} - v_{20} + v_{b0} + v_{c0} - 2v_{a0} \quad (17)$$

$$v_{vw} = v_{20} - v_{30} + v_{a0} + v_{c0} - 2v_{b0} \quad (18)$$

$$v_{wu} = v_{30} - v_{10} + v_{a0} + v_{b0} - 2v_{c0} \quad (19)$$

IV. PLANAR TRANSFORMER DESIGN

In contrast to the traditional transformers with large

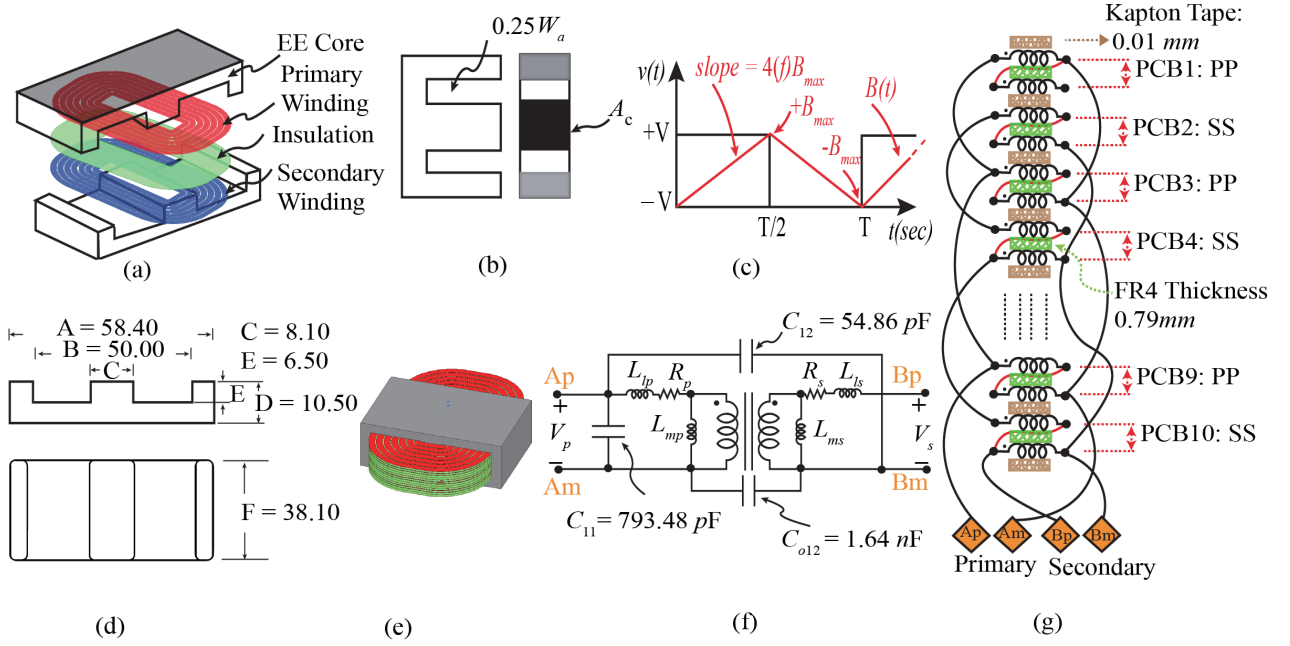


Fig. 4. (a) Typical EE-planar transformer showing the EE-core, primary winding, insulation and secondary winding layers. (b) The E core section of EE-core shows the window area W_a definition and the core cross-sectional area A_c . (c) Graphical representation of (28) and the $K_f = 4.0$ factor for square voltage input type of shape. (d) Ferroxcube E58/11/38-3F4 selected core with dimensions in mm indicated by letters A, B, C, D, E and F. (e) 3D view of the proposed transformer in Ansys MAXWEL simulation software. (f) Equivalent circuit model of the proposed transformer with the intra and inter capacitance values. (g) The main connections and layer arrangement of the proposed transformer.

core heights, planar transformers offer a compact design solution, as highlighted in [32]. Their integration into power electronics inverters and the power conversion process is attributed to their high-power density, superior performance, and cost-effectiveness. Advancements in planar magnetics technology have been facilitated by the use of low-profile ferrite cores, enabling operation at high frequencies, often in the range of several tens of kilohertz [33].

The increased adoption of planar transformers in power electronics inverters is not solely due to the core height and ferrite material; factors such as cost-effectiveness, mechanical robustness, and improved thermal responses contribute significantly to their popularity [33]. The precise construction of planar transformers, with each primary and secondary turn positioned meticulously within the core according to PCB layouts, facilitates better control over leakage inductance. This has rendered planar transformers particularly valuable in various converter families, including resonant LLC converters [32]. Standardizing insulating materials ensures consistent capacitance between layers, leading to enhanced predictability in the design and transformer performance [32], [34]. The typical structure of an EE-core planar transformer, as shown in Fig. 4(a), comprises the EE-core, primary and secondary windings, and insulation layers. Designing a planar transformer necessitates adherence to specific design constraints. Notably, these constraints include satisfying the output power requirements, meeting voltage regulation limits, and ensuring minimum efficiency and maximum permissible temperature rise [32]. Conventionally employed methodologies for designing conventional transformers, such as the area product A_p , which involves the product of the core window area W_a and

TABLE III
TSI PLANAR TRANSFORMER DESIGN REQUIREMENTS

Design Parameter	Value
Output Power P_o /kW	3.5
Output Current I_o /A	1.50
Frequency f /kHz	5
Efficiency η /%	98
Temperature rise ΔT /°C	10
Flux density B_m /mT	300
Turns Ratio n	1:1
Primary Voltage/V	130

the core cross-sectional area A_c (as depicted in Fig. 4(b)), and the core geometry K_g coefficient, are also applicable to planar transformer design. Both methodologies influence several critical design parameters, including power handling capacity, regulation capability, transformer size, weight, surface area, current density, and geometry [32]. In this study, the authors have adopted the area product methodology for its analytical design, primarily due to the availability of specific parameters in the core manufacturer's data sheet. While both methodologies yield similar design outcomes, the area product is preferred for its suitability in analytical design processes. Subsequent to the analytical analysis, the design is further validated using finite element analysis solver in Ansys Maxwell to verify its performance in the proposed twelve-step inverter. The design parameters for the planar transformer in the twelve-step inverter are summarized in Table III. The design process starts with the computation of the total power handling capability of the transformer, as outlined in (20), (21), and (22). Adhering to

the IPC-221A standard of printed circuit boards, the minimum width and thickness of conductors must be determined based on the current-carrying capacity and the maximum permissible conductor temperature.

$$P_{in} = \frac{P_o}{\eta} = \frac{3.5 \times 10^3}{0.98} = 3.57 \text{ kW} \quad (20)$$

$$P_t = P_o \left(\frac{1}{\eta} + 1 \right) \quad (21)$$

$$P_t = 3.5 \times 10^3 \times \left(\frac{1}{0.98} + 1 \right) = 7.07 \text{ kW} \quad (22)$$

$$I = k\Delta T^{0.024} A_t^{0.725} \quad (23)$$

where I is the current in amperes, A_t is the cross sectional area of the copper trace in mils^2 , ΔT is the temperature rise in $^\circ\text{C}$ and k is a constant determined by the type of PCB layer: $k = 0.048$ for outer layers and $k = 0.024$ for inner layers. The conductor's permissible temperature rise is defined as the difference between the maximum safe operating temperature of the printed board laminate material and maximum temperature of the thermal environment to which the printed board will be subjected [35]. In our design, we considered inner layers with maximum temperature rise of 10°C . Therefore, the minimum cross-sectional area of copper trace is equal to: 267.3 mils^2 or 0.0017 cm^2 . The current density J of the conductor defined as the total current divided by the cross sectional area of the conductor is given as:

$$J = \frac{I}{A_{t, [\text{cm}^2]}} \quad (24)$$

$$J = \frac{1.5}{0.0017} = 857.7 \text{ A/cm}^2 \quad (25)$$

Next, the area product A_p is calculated, which is the power handling capability of the core for the transformer:

$$A_p = \frac{P_t \times 10^4}{K_t K_u f A_c B_w J} \quad (26)$$

where K_f is the waveform coefficient.

$$K_f = \begin{cases} 4.0 & \text{for a square-wave} \\ 4.44 & \text{for a sine wave} \end{cases}$$

The coefficient of 4.0 is well explained by Faraday's law where:

$$v = n \frac{d\Phi}{dt} \quad (27)$$

Since $\Phi = BA_c$, (27) can be rewritten as:

$$v = nA_c \frac{dB(t)}{dt} \quad (28)$$

The slope of the $B(t)$ curve shown in Fig. 4(c) equals to:

$$\frac{dB(t)}{dt} = 4.0B_{\max}f \quad (29)$$

TABLE IV
PROPOSED PLANAR TRANSFORMER PARAMETERS

Parameter	Value
Magnetizing Inductance / μH	848.22
Leakage Inductance / μH @ 5kHz	0.197
dc Resistance / $\text{m}\Omega$	62.23
AC Resistance / $\text{m}\Omega$ @ 5kHz	165
C_{11} /pF	793.48
C_{12} /pF	54.86
C_{o12} /nF	1.64

Consequently, (28) can be simplified to:

$$V_{\text{average}} = 4.0B_{\max} N A_c f \quad (30)$$

The same principle applies for the sine-wave type of voltage excitation and the factor 4.44 can be justified in the same manner. The core window utilization factor, K_w , is assumed to be 0.128 or 12.8% for the cost and weight consideration. The cross-sectional area of the core $A_c = 3.08 \text{ cm}^2$ is selected based on the relationship between the current density and area product provided in [32]. Combining (22), (26) and the design information given in Table III, the area product is:

$$A_p = \frac{3.5 \times 10^3 \times 10^4}{4.2 \times 0.128 \times 5000 \times 3.08 \times 0.3 \times 857.7} = 17.25 \text{ cm}^4 \quad (31)$$

The commercially available core that is close to the calculated area product was found to be E58/11/38 as given by the Ferroxcube company. The material is selected to be 3F4 that satisfies our maximum flux density of 0.33 T. The shape of this core is shown in Fig. 4(d) with the dimensions indicated in the same figure.

The area product for the selected core A_p which is the power handling capability of the transformer core can be calculated as follows:

$$A_p = W_a A_c = 16.80 \text{ cm}^2 \quad (32)$$

where $W_a = 5.447 \text{ cm}^2$ is the window area, $A_c = 3.08 \text{ cm}^2$ is the cross-sectional area of the EE-core and indicated in Fig. 4(b). Next, the number of primary turns can be calculated using Faraday's law. Given that the primary voltage $V_p = 130 \text{ V}$, the number of turns can be given by:

$$N_p = \frac{V_p \times 10^4}{K_f B_m f A_c} = 70 \quad (33)$$

The proposed design is first created using Ansys PEmag, then imported to Ansys Maxwell for electromagnetic simulations. The proposed transformer 3D geometry is shown in Fig. 4(e). An equivalent circuit model is developed based on the work published in [34], and the finite element analysis is used to extract the parameters of the equivalent circuit model. The stray capacitances are found to be: intra capacitance $C_{11} = 793.48 \text{ pF}$, and both inter capacitance $C_{12} = 54.86 \text{ pF}$, $C_{o12} = 1.64 \text{ nF}$. A complete summary of the transformer parameters

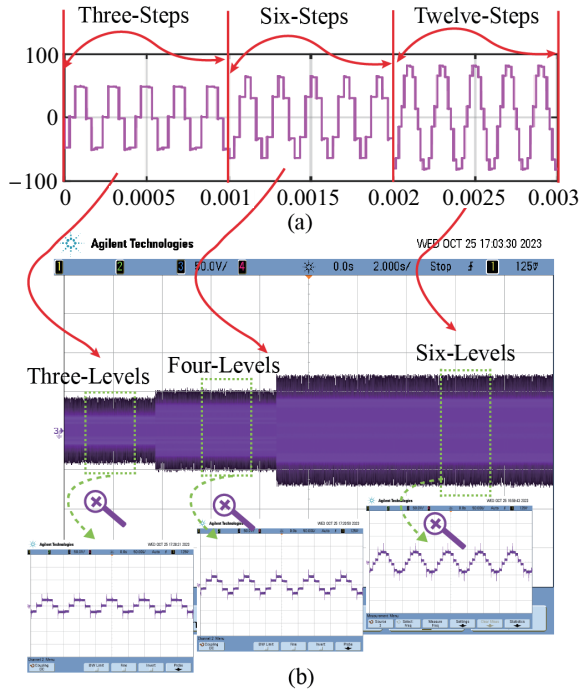


Fig. 6. Transient of the phase voltage with three, four, and six levels: (a) simulation and (b) experimental results.

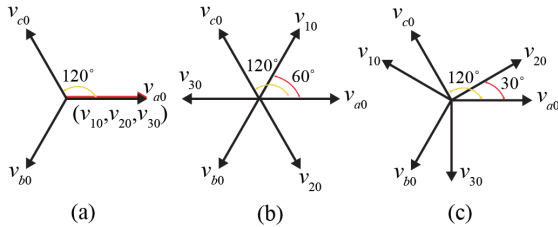


Fig. 7. Phasor diagram for different modes of operation: (a) three steps, (b) six steps, (c) twelve steps.

simulation and experimental validation of the twelve-step inverter featuring the proposed EE planar transformer. Operating at an input voltage of 25 V and a load resistor of 66 Ω , the setup operates at a frequency of 5 kHz. The Microchip dspic33ck256mp508 microcontroller is responsible for generating the necessary digital gate signals, ensuring precise phase shifts between the legs. The construction of the inverter utilizes the BSM75GB60DLC IGBT module. The complete setup configuration is visually depicted in Fig. 5(a), emphasizing the arrangement of the three planar transformers illustrated in Fig. 5(b). Using Ansys Maxwell and Ansys Twin-Builder under identical test conditions, the simulation yielded conclusive results. As depicted in Fig. 5(c), the TSI main voltages for phase u are showcased, specifically highlighting v_{10} at the top, v_{ac} in the middle, and v_{u0} at the bottom. The corresponding experimental verification results are presented in Fig. 5(f), featuring v_{10} at the top, v_{ac} in the middle, and v_{u0} at the bottom. Furthermore, Fig. 5(d) exhibits the phase voltages (v_{un} on top, v_{vn} in the middle, and v_{wn} at the bottom), with the corresponding experimental validation displayed in Fig. 5(g).

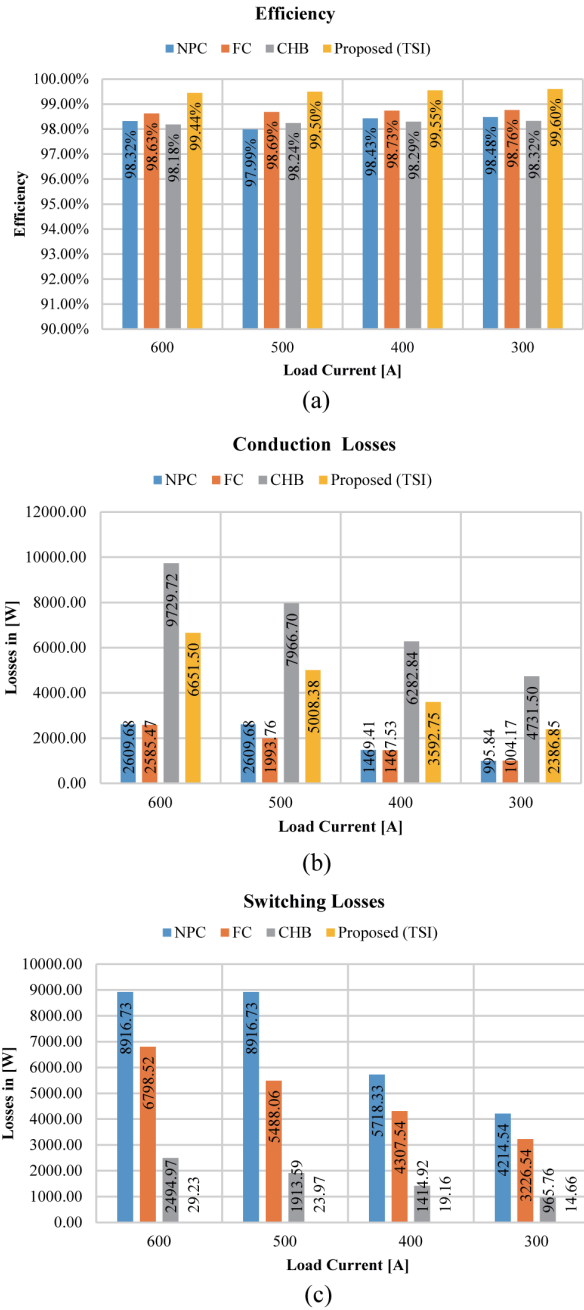


Fig. 8. Comparison between the proposed inverter and other multi-levels inverters. (a) Efficiency analysis. (b) Conduction losses. (c) Switching losses.

Providing a comprehensive representation of the phase and DC currents, Fig. 5(e) and Fig. 5(h) present a visual depiction from top to bottom, including i_{un} (first), i_{vn} (second), i_{wn} (third), and i_{dc} (fourth), all validated through simulation and experimental analysis. To evaluate the effectiveness of the proposed topology under dynamic conditions, replicating a startup ramp on the voltage to reduce the inrush current of PMSM, the inverter was tested to transition between three-steps, six-steps, and twelve-steps operation modes. As depicted in Fig. 6(a), the output phase voltage is precisely controlled to ensure three, four, and six voltage levels. The transition between the various

TABLE V
COMPARISON OF COMPONENT COUNT IN PROPOSED AND EXISTING THREE-PHASE INVERTERS TECHNOLOGY

Configuration	IGBTs	Diodes	Cap	DC Sources	TR	Total
NPC	12	18	2	1	0	33
FC	12	12	3	1	0	28
CHB	12	12	0	3	0	27
[13]	12	36	3	1	0	52
Proposed	12	12	0	1	3	28

operational modes is experimentally verified, as demonstrated in Fig. 6(b). This precise control is achieved by adjusting the phase shift applied to each inverter leg as illustrated in Fig. 7. Through the implementation of the proposed method, the configuration effectively demonstrates its ability to drive Permanent Magnet Synchronous Motors (PMSM) with instantaneous current control. Additionally, this method can be effectively utilized to establish constant V/Hz speed control of PMSM [37].

VI. EFFICIENCY ANALYSIS AND COMPARISON WITH EXISTING TECHNOLOGIES

This section evaluates the efficiency of the proposed inverter by calculating switching and conduction losses, assuming ideal transformers in this study. The switching frequency (F_s) is maintained at 20 kHz, and the fundamental frequency (F_0) at 60 Hz. The load power factor (pf) is unity to ensure that the maximum active power is delivered to the load. This condition is applied to all inverters, including NPC, FC, CHB, and the proposed topology.

The proposed converter is compared against the current technologies: specifically, three-phase twelve-switch NPC, FC, and CHB converters. All converters utilize the same IGBT switch, Infineon FF600R12ME4, with a voltage rating of 1200 V, a current rating of 600 A, and a maximum junction temperature of 150 °C. The numerical evaluation of converter losses is conducted using the PSIM thermal module. This module dynamically assesses the switching and conduction losses by identifying switching instants and conduction periods, summing the losses over a fundamental period. A comparison of efficiency for the proposed converter and the NPC, FC, and CHB converters is illustrated in Fig. 8(a). The efficiency of the proposed converter and other topologies remains high for lower load current, with a maximum efficiency of 99.60% recorded for the proposed converter at a power factor of one. However, existing technologies NPC, FC, and CHB exhibit lower efficiency compared to the proposed converter under higher load conditions. Nevertheless, the proposed converter maintains a high efficiency of 99% for all load conditions. Fig. 8(b) illustrates the conduction loss breakdowns and compares them with the proposed converter and the NPC, FC, and CHB converters. Similarly, Fig. 8(c) presents the same information but for the switching loss breakdowns. Fig. 8(c) indicates that the proposed converter exhibits the minimum switching losses compared to all other topologies under

various loading conditions, thereby enhancing the overall converter efficiency. The proposed inverter has been compared against existing three-phase inverter technologies in terms of the total number of components used to build each converter, as summarized in Table V. The proposed topology uses fewer components compared to the Neutral Point Clamped (NPC) inverter and the topology proposed in [13]. Additionally, it uses the same number of components as the Flying Capacitor (FC) inverter but without the need for electrolytic capacitors. The reduction in the number of components not only decreases system losses but also reduces the production cost of the inverter. This contributes to enhancing the efficiency and cost-effectiveness, making the proposed inverter an attractive solution for modern power electronics applications.

VII. CONCLUSION

This paper presents an inverter that addresses the limitations of existing multi-level inverter (MLI) technologies for applications where high fundamental frequency is required. These limitations include high switching losses due to a high carrier switching frequency and the complexity of modulation schemes necessary to maximize source utilization. The proposed inverter increases the utilization of the DC source, offering a peak phase voltage of $5V_{dc} / 3$, which consistently remains higher than the DC link voltage. Operating with higher efficiency over a wide range of frequencies, the proposed inverter outperforms the current MLIs, including neutral point clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB), all of which exhibit lower efficiency at the same fundamental frequency. The paper presents a comprehensive design and analysis of the proposed planar transformers, including layer arrangements, materials, and connections. Detailed experimental and simulation results are provided to validate the overall operation and efficiency of the proposed inverter.

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