

# A Constant Common Mode Voltage Single-Phase Five-Level Transformerless PV Inverter Considering the Effect of Switch Device Junction Capacitance

MLN VITAL, Venu SONTI, Yam P. SIWAKOTI, Sze Sing LEE, and Sachin JAIN

**Abstract**—Constant common mode voltage (CCMV) is critical in Solar Photovoltaic (SPV) systems. Maintaining CCMV further eliminates the voltage transitions across the parasitic capacitance of the PV panel, making it a low-frequency output voltage waveform. This further reduces the CMC and leakage current in the SPV systems. This paper presents a CCMV switched capacitor PV inverter configuration that maintains a low-frequency terminal voltage while considering the effect of switch device junction capacitance (SDJC). Thus, the proposed configuration eliminates the transitions in the common mode and terminal voltage due to the SDJC. The two switched capacitors employed in the proposed configuration are charged and discharged within each switching period, supporting the self-charge balance feature apart from low voltage and RMS current rating, reducing its size and value. Further, the proposed system effectively utilizes the PV source as switch capacitors and the DC-bus buffer capacitor across the PV source comes in parallel in each switching period. The proposed configuration can also operate at lower modulation indices, generating three levels with CCMV. A new mathematical analysis considering SDJC is given for the derivation of expression for CMV and terminal voltage, which is further verified using simulation and experimental results.

**Index Terms**—Five-level inverter common mode voltage, switched capacitor, transformerless PV inverter, leakage current.

## I. INTRODUCTION

IN recent times, transformerless PV inverters (TPVIs) [1]–[12] which eliminates the transformer between PV source and grid have earned some interest among researchers worldwide. Due to the absence of galvanic isolation in the system, TPVIs have advantages like reduced weight, reduced power

conversion stages, high efficiency, and reduced cost. However, alleviating common mode current (CMC) and leakage current flowing through the parasitic capacitance in the PV systems remains a critical issue that must be taken care of during the inverter design [1]. The flow of CMC and leakage current in the TPVI creates serious concerns like distortion of grid current, increased conducted and radiated EMI issues, additional losses in PV panels, deterioration of PV panel characteristics, etc. Due to this, it is very critical to minimize or maintain the magnitude of CMC and leakage currents flowing in the TPVI below the prescribed limit. One such limit for leakage current is mentioned in the German standard VDE0126-1-1 [13].

The CMC and leakage current flowing in the TPVI are mainly due to the high-frequency transitions (HFTs) in the common mode voltage (CMV) [13]. Thus, it is essential to eliminate such HFTs in CMV to minimize the CMC and leakage currents. Therefore, controlling the magnitude of CMC and leakage current by maintaining the constant common mode voltage (CCMV) [13] is vital in TPVI systems. Maintaining the CCMV eliminates the common mode current and reduces the leakage current. This can be attributed to the fact that for a CCMV, the voltage across the PV panel parasitic capacitance will be low-frequency [14] in nature. This voltage across the PV panel parasitic capacitance is normally termed as the terminal voltage. The PV panel parasitic capacitance normally offers high impedance to the low-frequency terminal voltage, which reduces the magnitude of the leakage current. Apart from the minimization of CMC and leakage, the harmonic free current with low THD needs to be injected into the grid. Thus, there is a requirement of multi-level inverter topology with CCMV. In the literature, the researchers have provided various solutions for addressing the above-mentioned concerns.

Xiaoqiang *et al.* [15] given an interesting five-level TPVI topology to tackle the issue of terminal and common mode voltage (TCMV) transitions. The given multi-level topology has two individual H5 cascaded inverters. The given topology generates five levels output voltage by using ten switches and two independent symmetrical PV sources. The given topology suffers from the adverse effects of switch device junction capacitance (SDJC), resulting in HFTs in the common mode voltage (CMV). Further, no analysis on CMV, while taking into account the effect of the SDJC is given. Also, the given topology requires two independent symmetrical PV sources with equal operating voltage to obtain the five levels in the

---

Manuscript received October 13, 2023; revised April 24, 2024; accepted May 25, 2024. Date of publication September 30, 2024; date of current version June 11, 2024. No funding was received to assist with the preparation of this manuscript. (Corresponding author: Sachin Jain.)

MLN Vital, V. Sonti, and S. Jain are with the Department of Electrical Engineering, National Institute of Technology Raipur, Raipur 492010, India (e-mail: mlnvital@gmail.com; svnu.ee@nitrr.ac.in; sjain.ee@nitrr.ac.in).

Y. P. Siwakoti is with the Faculty of Engineering and Information Technology, University of Technology Sydney, Sydney, NSW 2007, Australia (e-mail: yam.siwakoti@uts.edu.au).

S. S. Lee is with the Newcastle University in Singapore, Singapore 567739 (e-mail: ss.lee@ieee.org).

Digital Object Identifier 10.24295/CPSSPEA.2024.00010

inverter output voltage.

Sathik *et al.* [16] given another interesting five-level inverter topology for addressing the issue of leakage current in TPVIs. The given five-level inverter uses nine power semiconductor devices and two switched capacitors to obtain the five levels in the inverter output voltage with a single PV source. The given topology has the benefit of twice the voltage-boosting capability with effective PV source utilization. However, the presence of diodes in the five-level inverter limits the reactive power capability of the given configuration. Further, the given topology suffers from the problem of SDJC at zero voltage level. Due to the SDJC, the TCMV have different voltage values both during active and zero state. Different voltage values leads to high-frequency switching transitions in TCMV. Further, the given solution reduces the CMC and leakage currents by minimizing the transitions in the CMV, but does not completely eliminate it.

Another interesting five-level inverter topology with CCMV is given by Xiaonan *et al.* [17]. The given five-level TPVI topology uses twelve switches, two flying capacitors and a single PV source for the generation of five-level output voltage. The given topology reduces the leakage current by maintaining CCMV. But special care or strategy is required to maintain  $V_{pv}/4$  (one-fourth of DC bus or PV voltage) across the flying capacitor. Thus, a complex control circuit is always required to charge the flying capacitors. Bharath *et al.* [18] given another interesting inverter topology with five-level output with the alleviation of leakage current in PV systems. The given inverter uses nine semiconductor devices and two switched capacitors to obtain the five-level output with CCMV. However, the switched capacitors used in the five-level inverter do not charge for a period of  $60^\circ$  of output voltage. In other words, the longest discharge period for the switched capacitors is  $60^\circ$ . Due to high discharge time, the size of switched capacitors required would be very large. In the given topology, the switched capacitors also draw high charging currents from the PV source and there is no self-charge balancing feature for the switched capacitors. Also, in the given five-level inverter, the PV source remains idle for a period of  $120^\circ$  in the inverter output voltage. As a result, the given five-level inverter has less DC bus voltage utilization. In addition to this, the size of the buffer capacitor required at the output of the PV source will be large. Also, the given five-level inverter will not work for the modulation index less than 0.5 because of the absence of charging state for capacitors during 0 voltage level and may limit its operation for a stand-alone system.

Based on the above there is a requirement of the five-level inverter topology, which has below features:

1. Should maintain a CCMV for all the output voltage levels by taking the effect of SDJC into account.
2. Should require a low value and low voltage rating switched capacitors.
3. PWM strategy should be such that the inherent self-charge balancing property for switch capacitors should be there.
4. PV source should be utilized during each switching period  $T_s$  in the complete fundamental period  $T_g$ . This also

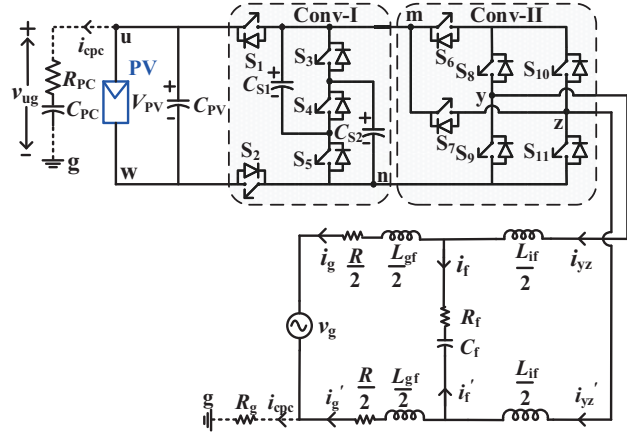


Fig. 1. Circuit schematic of proposed five-level inverter used for the alleviation of the leakage current.

results in a low PV voltage ripple leading to its maximum utilization.

5. Inverter should be able to operate for all modulation index with CCMV.

The given manuscript proposes the solution for CCMV five-level PV inverter topology with all the above-given features. Further in this manuscript, the expression for TCMV using the switching function including the SDJC effect is also presented. The complete manuscript is divided into six sections. Section II gives details of the operation of the proposed five-level TPVI topology. Section III gives the details of the effect of SDJC on CMV in the proposed five-level TPVI topology. The analysis of TCMV for the proposed five-level TPVI topology is discussed in Section IV. The simulation and experimental results of the proposed five-level TPVI topology is discussed in Section V and Section VI.

## II. WORKING PRINCIPLE AND OPERATION OF PROPOSED FIVE-LEVEL INVERTER

Fig. 1 shows the circuit schematic of the proposed five-level inverter. The proposed five-level inverter is developed by cascading two converter units namely Conv-I and Conv-II. The Conv-II [19] shown in Fig. 1 is a three-level inverter. By cascading the Conv-I with Conv-II, the number of levels in the output voltage of the proposed inverter is extended from three to five. Apart from increased number of levels in output voltage, the proposed five-level inverter also alleviates the leakage current by maintaining CCMV during all five levels in inverter output voltage.

The Conv-I constitutes of five switches  $S_1$  to  $S_5$  and two switched capacitors,  $C_{S1}$  and  $C_{S2}$ . Among the five switches,  $S_1$  and  $S_2$  are called decoupling switches. These switches connect and disconnect the PV source to input terminals (*i.e.*, the terminal points “m” and “n”) of the Conv-II. To generate a voltage value of  $V_{pv}$  in Conv-I the switch  $S_4$  along with the decoupling switches  $S_1$  and  $S_2$  are turned ON. When three switches are turned ON for the voltage level  $V_{pv}$  at Conv-I output, the two switched capacitors,  $C_{S1}$  and  $C_{S2}$  are connected

in series and their series connection comes in parallel with the input PV source. The switched capacitors are charged with input PV source when connected across it. Thus, the overall buffer capacitor value across the PV source increases during the voltage level  $V_{PV}$  at Conv-I output. The voltage level  $V_{PV}/2$  in Conv-I is generated by turning ON the other pair of switches  $S_3$ , and  $S_5$  and rest of the other switches in Conv-I are turned OFF. When switches  $S_3$ , and  $S_5$  are turned ON, the switched capacitors,  $C_{S1}$  and  $C_{S2}$  with an equal voltage of  $V_{PV}/2$  are connected in parallel to generate a voltage level of  $V_{PV}/2$ . Thus, the switches,  $S_3$  and  $S_5$  in Conv-I, operate in complementary mode to the switches,  $S_1$ ,  $S_2$ , and  $S_4$  to generate two voltage levels of  $V_{PV}/2$  and  $V_{PV}$  respectively.

The input terminals (“m” and “n”) of the Conv-II become the output terminals of the Conv-I [19]. Thus, the Conv-II gets its input from Conv-I. The Conv-II converts the generated voltage levels in Conv-I into required AC at the inverter output voltage, apart from generating 0 level at the inverter output voltage. The Conv-II is a H6 [19] inverter formed by the six switches,  $S_6$  to  $S_{11}$ . The Conv-I output voltage levels of  $+V_{PV}$  and  $+V_{PV}/2$  get converted into inverter output voltage  $v_{yz}$  with  $+V_{PV}$  and  $+V_{PV}/2$  values respectively by turning ON the switches,  $S_6$ ,  $S_8$  and  $S_{11}$  in the Conv-II. Similarly, Conv-I output voltage levels of  $+V_{PV}$  and  $+V_{PV}/2$  get converted into inverter output voltage  $v_{yz}$  with  $-V_{PV}$  and  $-V_{PV}/2$  values, respectively by turning ON the switches,  $S_7$  and  $S_9$  in the Conv-II. During the 0 voltage level, the switches  $S_8$  and  $S_{10}$  in Conv-II are turned ON to freewheel output current through these switches. Thus, during the levels of 0 and  $\pm V_{PV}$  across the inverter output, the two identical switched capacitors,  $C_{S1}$  and  $C_{S2}$  are charged in series by input PV source with an equal voltage of  $V_{PV}/2$ . This further helps in reducing PV voltage ripple. During the voltage level of  $V_{PV}/2$  at Conv-I output, the two switched capacitors,  $C_{S1}$  and  $C_{S2}$  are connected in parallel across the output load. The switched capacitors are discharged when connected in parallel with output load. Thus, in each switching period of the inverter the switch capacitors are charged and discharged simultaneously. This further helps in reducing the size and current rating of the switched capacitor. Above all, it further supports the effective utilization of the PV source, as 0 or  $\pm V_{PV}$  inverter output voltage levels exist in each switching period of the output voltage cycle.

Since, the switch capacitors are discharged at the voltage levels of  $\pm V_{PV}/2$ , the value of current flowing through the switched capacitors,  $C_{S1}$  and  $C_{S2}$  will be less in the proposed inverter. The parallel operation of the switched capacitors  $C_{S1}$  and  $C_{S2}$  during discharge further supports in reducing its current rating. This action helps in minimizing both voltage and current ripple in switched capacitors. Further, during the voltage levels 0 and  $\pm V_{PV}$ , the buffer capacitor  $C_{PV}$  (across the PV source) comes in parallel to the series connected switched capacitors  $C_{S1}$  and  $C_{S2}$ . As a result, the current ripple in the switched and buffer capacitors during the voltage levels 0 and  $\pm V_{PV}$  is minimized. In this way, the proposed topology using switched capacitors  $C_{S1}$  and  $C_{S2}$  generates five levels in the inverter output voltage. Further, the charging and discharging current of the switch capacitors is less, apart from less voltage

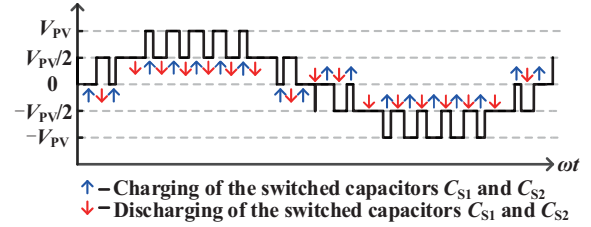


Fig. 2. Output voltage waveform of five-level inverter along with the charging and discharging of the switched capacitors  $C_{S1}$  and  $C_{S2}$ .

ripple. Apart from the less voltage ripple and less charging and discharging current, the switched capacitors  $C_{S1}$  and  $C_{S2}$  have self-charge balance property. Fig. 2 shows the waveform of the output voltage of the five-level inverter along with the charging and discharging of the switched capacitors  $C_{S1}$  and  $C_{S2}$ . From Fig. 2, it can be observed that the two switched capacitors  $C_{S1}$  and  $C_{S2}$  are charged in one voltage level and discharged in the subsequent output voltage level. This pattern will continue for the entire cycle of the output voltage. So, for any required output voltage, the two switched capacitors  $C_{S1}$  and  $C_{S2}$  have a self-charge balancing feature. Further, due to subsequent charging and discharging of the switched capacitors, the longest discharge period for the switched capacitors  $C_{S1}$  and  $C_{S2}$  is the switching time period. Due to this, the size of the switched capacitors  $C_{S1}$  and  $C_{S2}$  will be very less [18]. Therefore, by increasing the switching frequency, the size of switched capacitors  $C_{S1}$  and  $C_{S2}$  along with their current spike magnitude can be reduced further. Also, the two switched capacitors  $C_{S1}$  and  $C_{S2}$  are discharged in parallel during the voltage levels  $\pm V_{PV}/2$ . This results in the reduction of the value of switched capacitors to half. Further, due to the charging of switched capacitors  $C_{S1}$  and  $C_{S2}$  during the 0 voltage level, the proposed inverter can generate three levels ( $\pm V_{PV}/2$  and 0) for the lower modulation indices. Therefore, the proposed topology can be even operated at lower modulation indices.

The Conv-II output terminals are connected to grid  $v_g$  through a filter as shown in Fig. 1. The LCL filter is used to smoothen the inverter output current. The terms  $L_{if}$  and  $L_{gf}$  in the LCL filter refer to the filter inductor at the inverter and grid side respectively. The term  $C_f$  represents the filter capacitor. The terms  $R_f$ ,  $R$  and  $R_g$  represent the damping resistor in the filter, filter resistor, and the ground resistor respectively. The terms  $i_{yz}$ ,  $i_g$  and  $i_f$  denote the inverter output current, grid current and the filter shunt branch current respectively. The series combination of parasitic capacitance  $C_{pc}$  and resistance  $R_{pc}$  of the PV source is connected between the PV “u” and ground “g” terminal nodes as shown in Fig. 1. The parasitic resistance and capacitance are denoted by terms  $R_{pc}$  and  $C_{pc}$  respectively. The  $i_{cpc}$  is the current flowing through this parasitic branch. The voltage  $v_{ug}$  is called the terminal voltage of the PV source. The terminal voltage is a function of the common mode and the grid voltage. The common mode is the average of the inverter pole voltages [20]–[21]. Usually while calculating the inverter pole voltages, the effect of the junction capacitance across power semiconductor switches

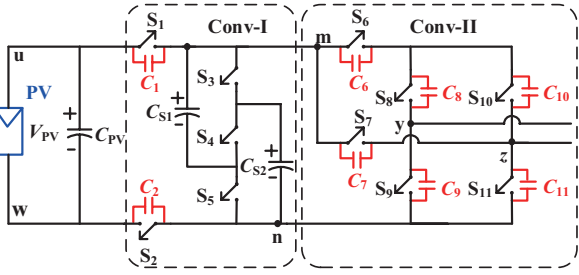


Fig. 3. Circuit of the proposed five-level inverter along with SDJC.

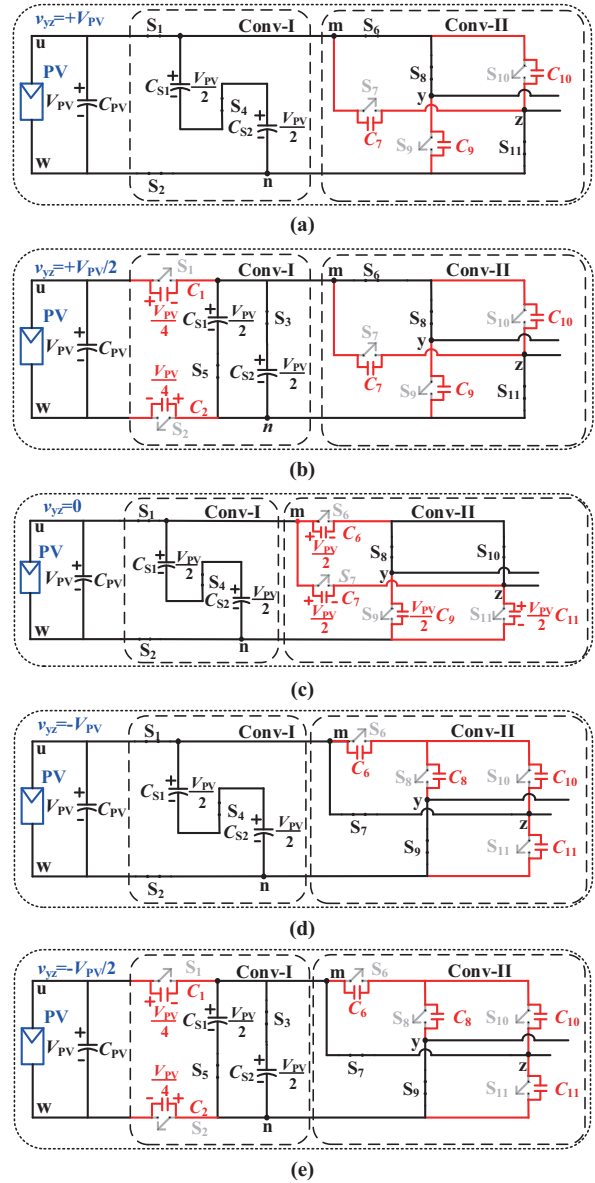
TABLE I  
SWITCHING STATES OF THE SWITCHES ALONG WITH THE POLE VOLTAGE,  
OUTPUT VOLTAGE AND COMMONMODE VOLTAGE

Switching states of the switches	$V_{yw}$	$V_{zw}$	$V_{yz}$	$V_{cm}$
$S_1, S_2, S_4, S_6, S_8$ and $S_{11}$ are turned ON $S_3, S_5, S_7, S_9$ and $S_{10}$ are turned OFF	$V_{PV}$	0	$+V_{PV}$	$V_{PV}/2$
$S_3, S_5, S_6, S_8$ and $S_{11}$ are turned ON $S_1, S_2, S_4, S_7, S_9$ and $S_{10}$ are turned OFF	$3V_{PV}/4$	$V_{PV}/4$	$+V_{PV}/2$	$V_{PV}/2$
$S_1, S_2, S_4, S_8$ and $S_{10}$ are turned ON $S_3, S_5, S_6, S_7, S_9$ and $S_{11}$ are turned OFF	$V_{PV}/2$	$V_{PV}/2$	0	$V_{PV}/2$
$S_3, S_5, S_7$ and $S_9$ are turned ON $S_1, S_2, S_4, S_6, S_8, S_{10}$ and $S_{11}$ are turned OFF	$V_{PV}/4$	$3V_{PV}/4$	$-V_{PV}/2$	$V_{PV}/2$
$S_1, S_2, S_4, S_7$ and $S_9$ are turned ON $S_3, S_5, S_6, S_8, S_{10}$ and $S_{11}$ are turned OFF	0	$V_{PV}$	$-V_{PV}$	$V_{PV}/2$

that are in the turn OFF state is neglected. But practically, it can affect inverter pole voltages during the turn OFF condition typically in DC decoupled configuration [15]. The transitions in the TCMV waveforms, can be attributed to the effect of SDJC during the turn-off state. The proposed DC decoupled five-level inverter using PWM technique eliminates this effect and restricts the HFTs in the TCMV. Due to the absence of these HFTs, the proposed five-level inverter with the given PWM technique generates a low-frequency terminal voltage and CCMV. The low-frequency terminal voltage reduces the magnitude of the leakage current due to high impedance value of parasitic capacitance in the PV system. Thus, the proposed topology attenuates leakage current magnitude in the PV systems. The magnitude of leakage current is further alleviated due to the additional restriction of transitions in the TCMV because of SDJC effect. The details of restriction of transitions in the TCMV due to SDJC is explained in the next section.

### III. EFFECT OF SWITCH DEVICE JUNCTION CAPACITANCE ON CMV IN THE PROPOSED FIVE-LEVEL MLI

The proposed solution, as discussed, alleviates the both leakage and common mode current. This is obtained by maintaining the low-frequency terminal voltage and CCMV by considering the effect of the SDJC for the DC decoupled configuration. The effect of SDJC on TCMV will exist, whenever the corresponding switch is turned OFF. Fig. 3 shows the circuit of the proposed five-level inverter along with their

Fig. 4. Modes of operation of the of proposed five-level inverter for the voltage levels: (a)  $+V_{PV}$ , (b)  $+V_{PV}/2$ , (c) 0, (d)  $-V_{PV}$ , and (e)  $-V_{PV}/2$  along with their SDJC.

SDJC. The term  $C_i$  denotes the junction capacitance across switch  $S_i$ , where  $i=1,2,\dots,11$ . The SDJC are shown in the red color of Fig. 3. In Conv-I, the series connected device junction capacitors  $C_3$  and  $C_4$  comes in parallel to the switched capacitor  $C_{S1}$  and the series connected device junction capacitors  $C_4$  and  $C_5$  comes in parallel to the switched capacitor  $C_{S2}$  during circuit operation. As the values of these device junction capacitors are very small when compared with switched capacitors  $C_{S1}$  and  $C_{S2}$ , their effect in the circuit can be neglected as can be observed in Fig. 3. The effect of SDJC on the proposed inverter topology need to be analyzed for all the output voltage levels.

Fig. 4 shows the different modes of operation of the proposed inverter considering their SDJC. For simplicity, the value of the SDJC is assumed to be equal. The effect of SDJC on the

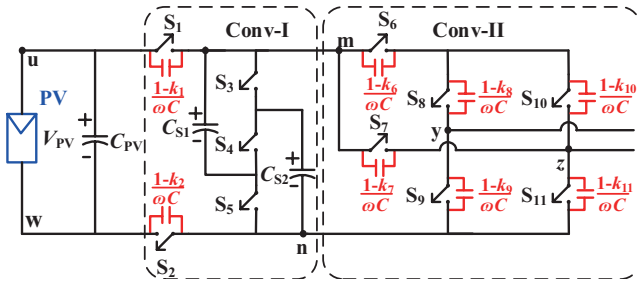


Fig. 5. Circuit diagram of the proposed five-level inverter along with the switching function incorporated SDJC.

CMV which is the average of two pole voltages  $v_{yw}$  and  $v_{zw}$  can be obtained by observing the magnitude of pole voltages  $v_{yw}$  and  $v_{zw}$  for each output voltage level. Table I shows the switching states of the individual switches along with the pole voltages  $v_{yw}$ ,  $v_{zw}$ , output voltage  $v_{yz}$  and common mode voltage  $v_{cm}$ . During the output voltage levels  $+V_{PV}$  and  $-V_{PV}$  as shown in Fig. 4(a) and (d), the value CMV  $V_{cm}$  is equal to  $V_{PV}/2$ . For the output voltage levels  $+V_{PV}/2$  and  $-V_{PV}/2$  shown in Fig. 4(b) and (e), due to the turn OFF the switches  $S_1$  and  $S_2$  in Conv-I, a voltage of  $V_{PV}/4$  is appeared across the SDJC  $C_1$  and  $C_2$ . Therefore, the pole voltages  $v_{yw}$  and  $v_{zw}$  will attain the values  $3V_{PV}/4$  and  $V_{PV}/4$  for the output voltage  $+V_{PV}/2$  and the pole voltages  $v_{yw}$  and  $v_{zw}$  will attain the values  $V_{PV}/4$  and  $3V_{PV}/4$  for the output voltage  $-V_{PV}/2$ . This helps in retaining the value of the CMV to  $V_{PV}/2$ . During the 0 voltage level as shown in Fig. 4(c), a pair of series combinations of the SDJC ( $C_6$ ,  $C_9$ ) and ( $C_7$ ,  $C_{11}$ ) comes in parallel with the source. This results in the equal pole voltages of  $V_{PV}/2$  for the  $v_{yw}$  and  $v_{zw}$  as can be seen in Fig. 4(c). Therefore, for the 0 voltage level also, the value of CMV is retained to  $V_{PV}/2$  in the proposed configuration. Thus, the proposed system maintains the CMV to the value of  $V_{PV}/2$  without being affected by the presence of SDJC. Further, the effect of SDJC on CMV and terminal voltage can also be analyzed using mathematical analysis. A mathematical analysis-based switching function concept incorporating the effect of SDJC is given in the next section.

#### IV. ANALYSIS OF TERMINAL AND COMMON MODE VOLTAGE

For alleviation of CMC and leakage current through PV system parasitic capacitance, the nature of the TCMV needs to be studied. For analyzing the nature of TCMV, the switching function concept [20]–[21] is used, which also includes the effect of SDJC. Fig. 5 shows the circuit diagram of the proposed five-level inverter along with the switching function incorporated SDJC. The binary variable  $k_i$  represents the switching state for the switch  $S_i$  where  $i=1,2,\dots,11$ , will have a value of either 1 or 0 representing the turn ON and turn OFF of the switch. The impedance of SDJC during the turn-on state ( $k_i = 1$ ) is zero and its effect is neglected. However, during the turn-off state of switch  $S_i$  the corresponding binary variable  $k_i$  is equal to 0. As a result, an impedance due to SDJC  $C_i$  will appear across the switch  $S_i$ . For simplicity,  $C_i$  is taken as  $C$  for all the values of

$i$ . In Conv-I, the expression for the voltages  $v_{mm}$ ,  $v_{um}$  and  $v_{nw}$  is given by (1) and (2).

$$v_{mm} = V_{PV} (k_1 k_2) + \frac{V_{PV}}{2} (k_3 k_5) \quad (1)$$

$$v_{um} = v_{nw} = \frac{v_{mm} - V_{PV} (k_1 k_2)}{2} \quad (2)$$

In Conv-II using the circuit analysis, the expression for the voltages  $v_{yn}$  and  $v_{zn}$  are given by

$$v_{yn} = \frac{v_{mm} (1 - k_9)}{Den} \quad (3)$$

$$v_{zn} = \frac{v_{mm} (1 - k_6)}{1 + \frac{(1 - k_7)}{(1 - k_{11})}} + \frac{v_{mm} k_6 \left[ \frac{Num1}{Den1} \right]}{1 + \frac{k_c}{(1 - k_{11})}} \quad (4)$$

$$Den = (1 - k_9) + (1 - k_8) + k_a + k_b + \frac{k_b [k_a + (1 - k_9) + (1 - k_8)]}{(1 - k_{11}) + k_c} \quad (5)$$

$$Num1 = [k_c + (1 - k_{11})][k_a + (1 - k_8) + (1 - k_9)] \quad (6)$$

$$Den1 = [k_c + (1 - k_{11})][k_a + (1 - k_8) + (1 - k_9)] + k_b [k_c + (1 - k_{11}) + k_a + (1 - k_8) + (1 - k_9)] \quad (7)$$

where,

$$k_a = \frac{(1 - k_6)(1 - k_{10})}{(1 - k_6) + (1 - k_7) + (1 - k_{10})} \quad (8)$$

$$k_b = \frac{(1 - k_6)(1 - k_7)}{(1 - k_6) + (1 - k_7) + (1 - k_{10})} \quad (9)$$

$$k_c = \frac{(1 - k_7)(1 - k_{10})}{(1 - k_6) + (1 - k_7) + (1 - k_{10})} \quad (10)$$

The expressions for the pole voltages  $v_{yw}$  and  $v_{zw}$  are given by

$$\begin{cases} v_{yw} = v_{yn} + v_{nw} \\ v_{zw} = v_{zn} + v_{nw} \end{cases} \quad (11)$$

The expression for the output voltage  $v_{yz}$  is given by

$$v_{yz} = v_{yw} - v_{zw} \quad (12)$$

The expression for the CMV  $v_{cm}$  is given by

$$v_{cm} = \frac{v_{yw} + v_{zw}}{2} \quad (13)$$

From Fig. 1, the expression for  $v_{yg}$  in terms of  $v_{yw}$ ,  $V_{PV}$  and  $v_{ug}$  is given by

$$v_{yg} = v_{yw} - V_{PV} + v_{ug} \quad (14)$$

Similarly, the expression for  $v_{zg}$  in terms of  $v_{zw}$ ,  $V_{PV}$  and  $v_{ug}$  is given by

$$v_{zg} = v_{zw} - V_{PV} + v_{ug} \quad (15)$$

Adding (14) and (15) gives

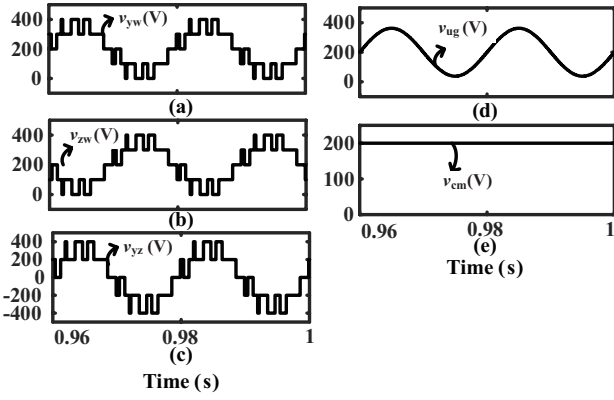


Fig. 6. Analytical waveforms of (a) pole voltage  $v_{yw}$ , (b) pole voltage  $v_{zw}$ , (c) output voltage  $v_{yz}$ , (d) terminal voltage  $v_{Ug}$ , (e) CMV  $v_{cm}$  for the proposed five-level inverter.

TABLE II  
SIMULATION PARAMETERS

Parameter	Value	Parameter	Value
$V_{PV}$	400 V	$C_f$	0.1 $\mu$ F
$f_{sw}$	5 kHz	$R_f$	0.1 $\Omega$
$v_g$	325 V	$C_{pc}$	200 nF
$f_g$	50 Hz	$R_{pc}$	1 $\Omega$
$L_{if}$	4 mH	$R_{pc}$	0.1 $\Omega$
$L_{gf}$	4 mH	$C_{PV}$	1000 $\mu$ F
$R$	0.01 $\Omega$	$C_{S1}, C_{S2}$	1000 $\mu$ F

$$v_{yg} + v_{zg} = v_{yw} + v_{zw} - 2V_{PV} + 2v_{Ug} \quad (16)$$

The expression for  $v_{yg}$  and  $v_{zg}$  in terms of  $v_g$  is given by [20]–[21].

$$v_{yg} + v_{zg} = v_g \quad (17)$$

Equating (16) and (17) gives

$$v_{Ug} = 0.5v_g + V_{PV} - 0.5v_{yw} - 0.5v_{zw} \quad (18)$$

The analytical waveforms of pole voltages  $v_{yw}$  and  $v_{zw}$ , output voltage  $v_{yz}$ , terminal voltage  $v_{Ug}$  and CMV  $v_{cm}$  are obtained using (3)–(13) and (18). The derived expressions are plotted using MATLAB software. The parameters used for obtaining the analytical waveforms are:  $V_{PV} = 400$  V, grid voltage  $v_g = 230$  V (RMS), grid frequency  $f_g = 50$  Hz, and switching frequency  $f_{sw} = 500$  Hz. Here, the switching frequency is taken very low to show the switching transitions in the pole voltages and output voltage clearly [20]–[21]. Fig. 6 shows the analytical waveforms of (a) pole voltage  $v_{yw}$ , (b) pole voltage  $v_{zw}$ , (c) output voltage  $v_{yz}$ , (d) terminal voltage  $v_{Ug}$  and (e) CMV  $v_{cm}$  for the proposed five-level inverter. From Fig. 6(a) and (b), it can be observed that there are three levels 0,  $V_{PV}/2$  and  $V_{PV}$  in the pole voltages  $v_{yw}$  and  $v_{zw}$ . From Fig. 6(c), it can be observed that there are five levels in the output voltage  $v_{yz}$ . For CCMV waveform shown in Fig. 6(e), the

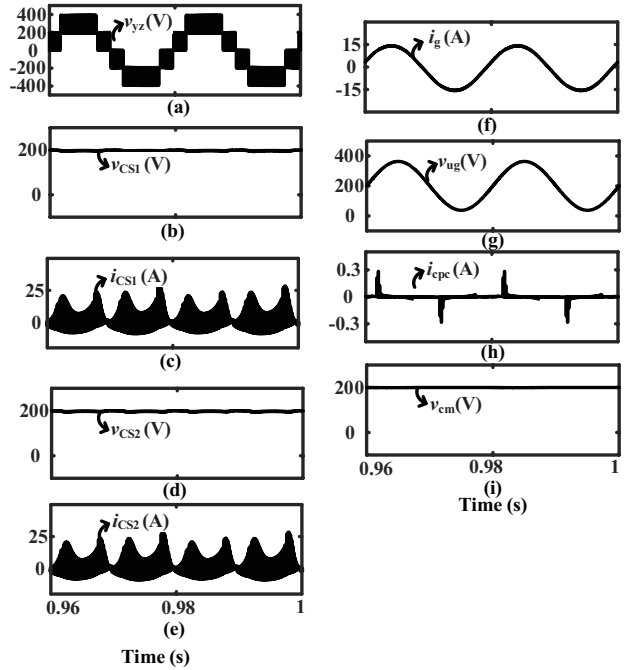


Fig. 7. Simulation waveforms of (a) output voltage  $v_{yz}$ , (b) voltage across switched capacitor  $C_{S1}$   $v_{CS1}$ , (c) current flowing through the switched capacitor  $C_{S1}$   $i_{CS1}$ , (d) voltage across switched capacitor  $C_{S2}$   $v_{CS2}$ , (e) current flowing through the switched capacitor  $C_{S2}$   $i_{CS2}$ , (f) grid current  $i_g$ , (g) terminal voltage  $v_{Ug}$ , (h) leakage current  $i_{pc}$ , (i)  $v_{cm}$  for the proposed five-level inverter.

nature of terminal voltage waveform is purely low-frequency sinusoidal waveform with DC offset as shown in Fig. 6(d). The low frequency terminal voltage can be attributed to the constant value of CMV  $v_{cm}$  around 200 V as can be observed from Fig. 6(e).

## V. SIMULATION RESULTS

In order to validate the performance of the proposed five-level inverter simulation is done in MATLAB using the POWERSIM block sets. Table II presents the parameters that are considered for carrying simulation. Fig. 7 shows the simulation waveforms of the proposed five-level inverter. From Fig. 7(a), the output voltage  $v_{yz}$  having step waveform with transitions between 0 to  $V_{PV}/2$  and  $V_{PV}/2$  to  $V_{PV}$  can be observed. This result in lower THD of the output voltage in the proposed topology when compared to the topology proposed in [20]–[21]. Fig. 7(b)–(e) show the waveforms of voltage across and the current through the switched capacitors  $C_{S1}$  and  $C_{S2}$ . From Fig. 7(b) and (d), it can be observed that the switched capacitors  $C_{S1}$  and  $C_{S2}$  are charged to 200 V (*i.e.*, half of the DC bus voltage  $V_{PV}$ ). The voltage ripple obtained from plots in Fig. 7(b) and (d) is around 3%. The currents  $i_{CS1}$  and  $i_{CS2}$  flowing through the switched capacitors  $C_{S1}$  and  $C_{S2}$  are shown in Fig. 7(c) and (e).

The RMS value of the current flowing through the capacitors is 7 A. As said earlier, there is low voltage and current ripple in the switched capacitors  $C_{S1}$  and  $C_{S2}$ . Fig. 7(f) shows the grid current waveform  $i_g$  having sinusoidal nature. Fig. 7(g) shows

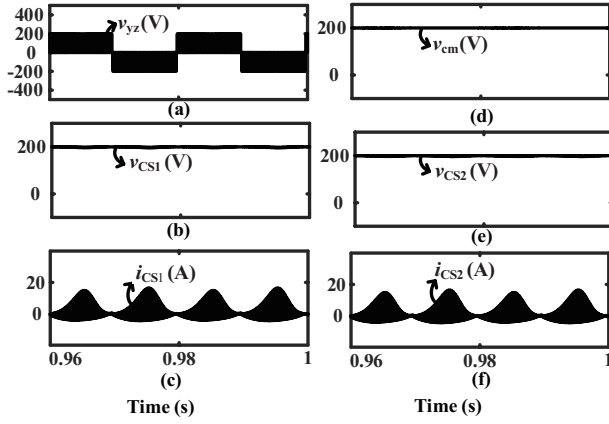


Fig. 8. Simulation waveforms of (a) output voltage  $v_{yz}$ , (b) voltage across switched capacitor  $C_{S1}$   $v_{CS1}$ , (c) current flowing through the switched capacitor  $C_{S1}$   $i_{CS1}$ , (d) CMV  $v_{cm}$ , (e) voltage across switched capacitor  $C_{S2}$   $v_{CS2}$ , (f) current flowing through the switched capacitor  $C_{S2}$   $i_{CS2}$  of the proposed inverter for modulation index less than 0.5.

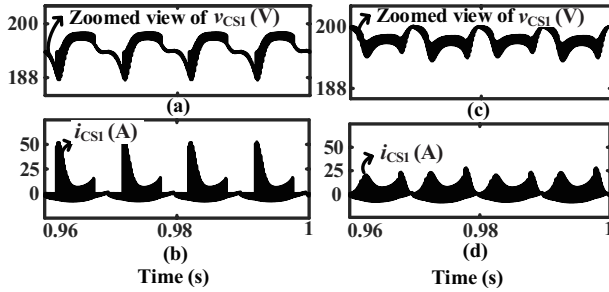


Fig. 9. Simulation waveforms of (a) zoomed view of voltage across switched capacitor  $v_{CS1}$ , (b) current flowing through the switched capacitor  $i_{CS1}$  for the inverter [18], (c) zoomed view of voltage across switched capacitor  $v_{CS1}$ , (d) current flowing through the switched capacitor  $i_{CS1}$  for the proposed inverter.

the terminal voltage waveform  $v_{yz}$ . The terminal voltage  $v_{ug}$  is a low-frequency sinusoidal signal. The low frequency nature of terminal voltage results in high impedance of parasitic capacitance resulting in low value of leakage current  $i_{cpc}$  as shown in Fig. 7(h). The leakage current RMS value is around 0.02 A. From Fig. 7(i), it can be observed that the value of CMV  $v_{cm}$  is maintained constant at around 200 V for all the output voltage levels. The proposed topology can also be operated for a modulation indices less than or equal to 0.5. Fig. 8 shows the simulation waveforms of the proposed system with the modulation index of 0.405. The proposed inverter output voltage waveform for the given modulation index  $m_a$  equal to 0.405 is shown in Fig. 8(a). The output voltage of the proposed five-level inverter has three levels:  $+V_{pv}/2$ , 0 and  $-V_{pv}/2$ .

Figs. 8(b) and (e) shows the voltage waveforms across the switched capacitors  $C_{S1}$  and  $C_{S2}$  for the given modulation index  $m_a$  equal to 0.405. As the charging of the series connected switched capacitors  $C_{S1}$  and  $C_{S2}$  occurs during the 0 output voltage level, the switched capacitors  $C_{S1}$  and  $C_{S2}$  are able to generate the output voltage levels of  $\pm V_{pv}/2$ . Thus, the proposed inverter even can be operated in the lower modulation index. Fig. 8(c) and (f) show the waveforms of

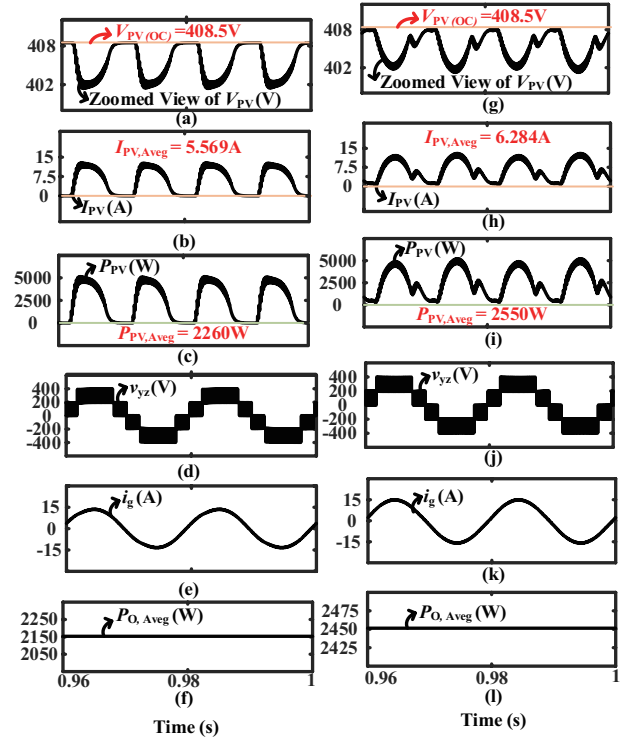


Fig. 10. Simulation waveforms of (a) voltage across the buffer capacitor  $C_{pv}$ , (b) current through the buffer capacitor  $C_{pv}$ , (c) power delivered by the buffer capacitor  $C_{pv}$ , (d) five-level output voltage of the inverter, (e) grid current, (f) average power delivered by the source for the five-level inverter proposed in [18], (g) voltage across the buffer capacitor  $C_{pv}$ , (h) current through the buffer capacitor  $C_{pv}$ , (i) power delivered by the buffer capacitor  $C_{pv}$ , (j) five-level output voltage of the inverter, (k) grid current, (l) average power delivered by the source for the proposed five-level inverter.

the current flowing through the switched capacitors. The peak value of the ripple current is around 15.5 A. Fig. 8(d) shows the CMV waveform of the of the proposed five-level inverter for a modulation index less than 0.5. From the subplot, it can be observed even at the lower modulation index also, the CMV is clamped to  $V_{pv}/2$ . Fig. 9 shows the waveforms of the zoomed view of voltage across the switched capacitor  $v_{CS1}$  and the switched capacitor current  $i_{CS1}$  for the five-level inverter topology proposed in [18] and proposed five-level inverter. The voltage ripple of switched capacitors used in the proposed topology is around 3%, whereas the voltage ripple of switched capacitors used in the topology proposed in [18] is around 6%.

Therefore, the proposed topology has less voltage ripple in the switched capacitor with less charging and discharging currents. In the five-level inverter proposed in [18], the capacitor is not charged for a period of  $60^\circ$  in each cycle of the output voltage. This results in high charging and discharging currents of the switched capacitors. However, the strategy of charging the switch capacitor in each switching cycle reduces magnitude of the charging and discharging currents through it.

Thus, the magnitude of the inrush current in the proposed configuration is minimum during operation and at starting can be minimized by using precharged capacitors. The peak value of currents in the switched capacitors is around 25 A for

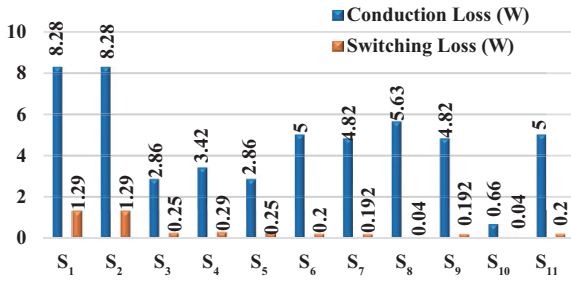


Fig. 11. The conduction loss and switching loss of the switches  $S_1$ - $S_{11}$  used in the proposed five-level inverter.

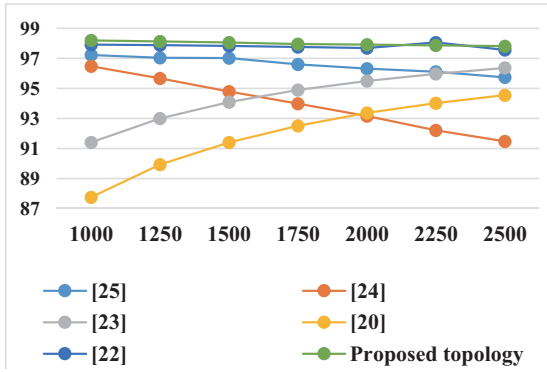


Fig. 12. The efficiency (%) of the proposed five-level inverter and other existing five-level TPVI topologies for the power levels from 1000 W to 2500 W.

the proposed five-level inverter. The peak value of switched capacitor current is around 50 A for the five-level inverter proposed in [18]. The RMS value of currents in the switched capacitors is around 7 A in the proposed five-level inverter. The RMS value of switched capacitor current is around 8.2 A for the five-level inverter proposed in [18]. Due to high value of RMS current, ripple voltage across the capacitor and required capacity of switch capacitor is high in the five-level inverter proposed in [18] compared to the proposed five-level inverter topology.

Further, to compare the PV source utilization, the simulation is done for proposed configuration and configuration given in [18] under identical conditions. In the simulation intentionally, the low value of the PV buffer capacitor of 1000  $\mu$ F is kept across the PV source. The simulation of both systems is done in identical conditions. Fig. 10(a)-(c) and (j)-(i) show the waveforms of the output voltage, current, and power of the PV source for the five-level inverter [18] and proposed inverter. The voltage ripple in the PV source is lower in the proposed system, as shown in Fig. 10(a) and (g). Further, the PV source operates near the open circuit voltage in [18], due to the long 60° (approximately 3.33 ms) discharging period. The operation of the PV source at open circuit voltage can be verified by the zero PV current and power as shown in Fig. 10(b) and (c), respectively. Same is not true for the proposed configuration. PV power does not have zero value supporting effective utilization of the PV source when compared with

TABLE III  
COMPARISON OF PROPOSED FIVE-LEVEL INVERTER WITH OTHER TPVI TOPOLOGIES

Topology	A	B	C	Remarks
[13] H9 Inverter	3	9	1	Require nine switches for maintaining the CCMV in a three-level inverter. The given configuration have transitions in the CMV to SDJC effect.
[13] H10 Inverter	3	10	1	Require ten switches for maintaining the CCMV in a three-level inverter. The given configuration have transitions in the CMV to SDJC effect.
[26]	5	12	2	Require more filter elements. Require two independent PV sources for obtaining five levels in the inverter output voltage.
[27]	5	11	2	Require two independent PV sources for obtaining five levels in the inverter output voltage. The PV source with higher voltage is underutilized.
[15]	5	10	2	Require two independent PV sources for obtaining five levels in the inverter output voltage. The topology suffers from the SDJC effect.
[21]	5	8	2	Require two independent PV sources for obtaining five levels in the inverter output voltage. The PV utilization is poor. The commonmode voltage is not constant. The THD of the inverter output voltage is high.
[18]	5	9	1	Switched capacitors were used to obtain five levels in the inverter output voltage. The charging and discharging currents of the switched capacitor is high. The value of switched capacitor required is large. The PV utilization is poor.
[17]	5	12	1	Complex control circuitry with sensors is required for balancing the capacitors. Switched capacitors were used to obtain five levels in the inverter output voltage. The charging and discharging currents of the switched capacitor is less. The value of switched capacitor required is small.
Proposed	5	11	1	The PV utilization is good. Doesn't require complex control circuitry, the switched capacitors have the self-charge balancing feature. The SDJC effect doesn't affect the common mode voltage.

A-Number of levels in the output voltage, B-Number of power semiconductor devices used, C-Number of independent PV sources required.

another inverter [18]. Further, higher average PV source current and power values can also be verified. Thus, the proposed configuration utilizes the PV source more effectively in comparison to the configuration proposed in [18], as shown in Fig. 10(c) and (i). Fig.10(d)-(f) show the waveforms of output voltage  $v_{yz}$ , grid current  $i_g$  and average output power of inverter  $P_{O, Aveg}$  of the five-level inverter [18] and proposed inverter. From Fig. 10(e), it can be observed that the average

TABLE IV  
COMPARISON OF PROPOSED FIVE-LEVEL INVERTER WITH OTHER TPVI TOPOLOGIES

Parameter	Value
$V_{PV}$	100 V
$f_{sw}$	5 kHz
$f_g$	50 Hz
$L$	2 mH
$C$	1 $\mu$ H
$R_{load}$	50 $\Omega$
$C_{S1}, C_{S2}$	1000 $\mu$ F

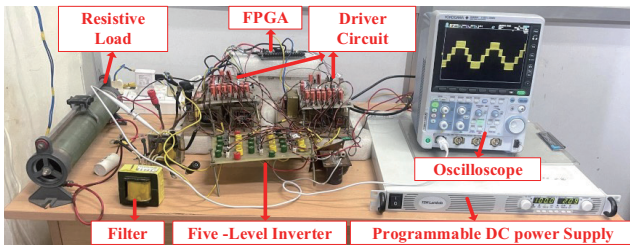


Fig. 13. Photograph of the experimental setup.

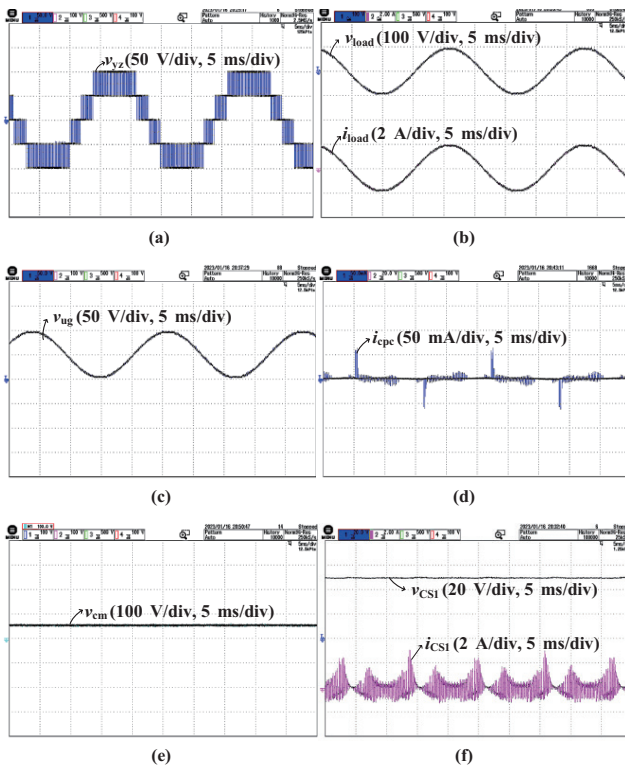


Fig. 14. Experimental waveforms of (a) output voltage  $v_{yz}$ , (b) voltage across the resistive load  $v_{load}$  and current flowing through the resistive load  $i_{load}$ , (c) terminal voltage  $v_{ug}$ , (d) leakage current  $i_{cpc}$ , (e) CMV  $v_{cm}$ , (f) voltage across switched capacitor  $C_{S1}$   $v_{CS1}$ , current flowing through the switched capacitor  $C_{S1}$   $i_{CS1}$  for the proposed five-level inverter.

output power is less in the inverter [18] when compared to the proposed inverter.

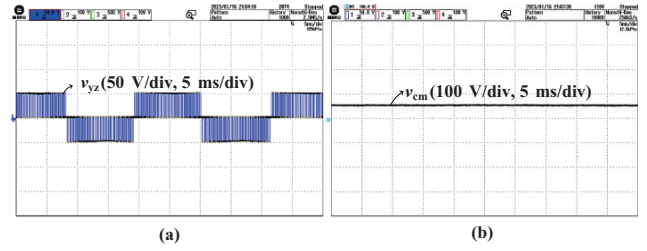


Fig. 15. Experimental waveforms of (a) output voltage  $v_{yz}$  and (b) CMV  $v_{cm}$  of the proposed five-level inverter for modulation index less than 0.5.

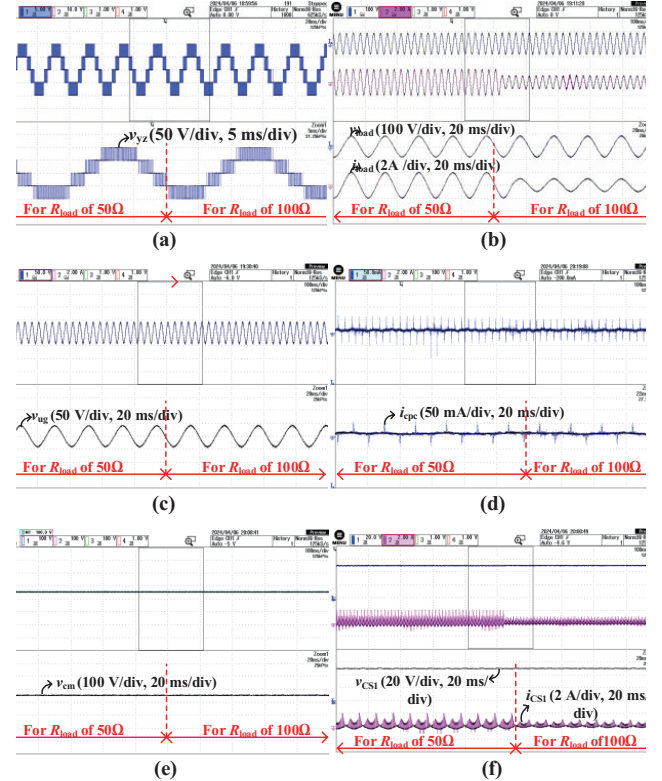


Fig. 16. Experimental waveforms of (a) output voltage  $v_{yz}$ , (b) voltage across the load  $v_{load}$ , current flowing through the load  $i_{load}$ , (c) terminal voltage  $v_{ug}$ , (d) leakage current  $i_{cpc}$ , (e) CMV  $v_{cm}$ , (f) voltage across switched capacitor  $C_{S1}$   $v_{CS1}$ , current flowing through the switched capacitor  $C_{S1}$   $i_{CS1}$  for the proposed five-level inverter with step change in the load  $R_{load}$  from 50  $\Omega$  to 100  $\Omega$ .

Further, the simulation was done to determine the efficiency of the proposed configuration. Fig. 11 shows the switching and conduction losses for all the switches employed in the proposed configuration. The proposed inverter is also compared with the other TPVI topologies with five-level output that exist in the literature. The efficiency plot for the proposed configuration along with other existing five-level TPVI is given in Fig. 12 for the power varying from 1000 W to 2500 W. A thorough examination of losses is conducted using PLECS software for all the topologies shown in Fig. 12. In this analysis, each topology is simulated for a system with approximately 2.5 kW power and a frequency of 50 Hz, operated at a switching frequency of 5 kHz within the PLECS environment. The switch and diode models employed for loss analysis in PLECS

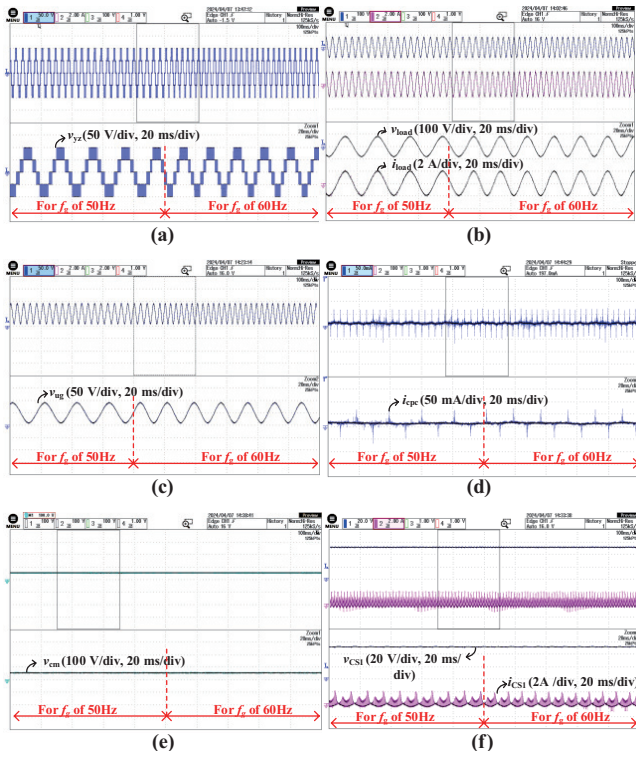


Fig. 17. Experimental waveforms of (a) output voltage  $v_{yz}$ , (b) voltage across the load  $v_{load}$ , current flowing through the load  $i_{load}$ , (c) terminal voltage  $v_{ug}$ , (d) leakage current  $i_{cpc}$ , (e) CMV  $v_{cm}$ , (f) voltage across switched capacitor  $C_{S1}$   $v_{CS1}$ , current flowing through the switched capacitor  $C_{S1}$   $i_{CS1}$  for the proposed five-level inverter with variable line frequency  $f_g$  from 50 Hz to 60 Hz.

are IGW30N60T\_IGBT and IGW30N60T, respectively for all the topologies. From Fig. 12, it can be observed that the efficiency of the proposed inverter is approximately around 98% over wide range of output power. Also from the Fig.12, it can be observed that the proposed topology has better efficiency compared to the other existing five-level TPVI topologies. Table III shows the comparison of the proposed five-level inverter with other existing TPVI topologies. Since the proposed topology comes under the family of symmetrical inductor-based inverters, only such topologies are considered for comparison. The merits of the proposed five-level topologies can be observed in Table III.

## VI. EXPERIMENTAL RESULTS

In order to further validate the proposed five-level inverter, an experimental prototype is developed. The parameters used for obtaining the experimental waveforms shown in Table IV. The programmable DC power supply were used instead of PV panels [20]–[21]. The pulses for the five-level inverter were generated using Basys 3 FPGA board. The MOSFETs IRF 640 were used as switches in the proposed five-level inverter. The driver IC HCPL 3120 is used to drive these switches. The output of the proposed five-level inverter is connected to a resistive load  $R_{load}$  via an LC filter [20]–[21]. The photograph of the experimental setup is shown in Fig. 13. Fig. 14 shows the experimental of (a) output voltage  $v_{yz}$ , (b) voltage  $v_{load}$

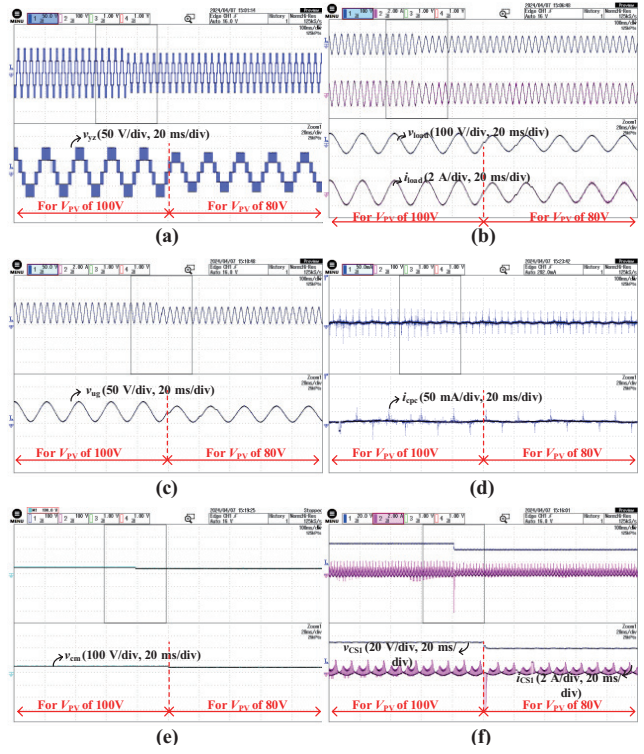


Fig. 18. Experimental waveforms of (a) output voltage  $v_{yz}$ , (b) voltage across the load  $v_{load}$ , current flowing through the load  $i_{load}$ , (c) terminal voltage  $v_{ug}$ , (d) leakage current  $i_{cpc}$ , (e) CMV  $v_{cm}$ , (f) voltage across switched capacitor  $C_{S1}$   $v_{CS1}$ , current flowing through the switched capacitor  $C_{S1}$   $i_{CS1}$  for the proposed five-level inverter with step change in the input voltage  $V_{PV}$  from 100 V to 80 V.

across the resistive load, and current  $i_{load}$  through the resistive load, (c) terminal voltage  $v_{ug}$ , (d) leakage current  $i_{cpc}$ , (e) CMV  $v_{cm}$ , (f) voltage  $v_{CS1}$  across switched capacitor  $C_{S1}$  and current  $i_{CS1}$  through the switched capacitor  $C_{S1}$  for the proposed five-level inverter. Fig. 15 shows the experimental waveforms of (a) output voltage  $v_{yz}$  and (b) CMV  $v_{cm}$  of the proposed five-level inverter for modulation index less than 0.5. The experimental waveforms obtained from the hardware setup exactly matches with the simulation results. This further justifies the operation of proposed five-level inverter. The experimental results were also taken in dynamic operating conditions like step change in the load, variable line frequency, step change in the input voltage. Fig. 16 shows the experimental waveforms of output voltage  $v_{yz}$ , voltage across the load  $v_{load}$ , current flowing through the load  $i_{load}$ , terminal voltage  $v_{ug}$ , leakage current  $i_{cpc}$ , CMV  $v_{cm}$  and voltage across switched capacitor  $C_{S1}$   $v_{CS1}$ , current flowing through the switched capacitor  $C_{S1}$   $i_{CS1}$  for the proposed five-level inverter with step change in the load  $R_{load}$  from 50  $\Omega$  to 100  $\Omega$ . Fig. 17 shows the experimental waveforms of output voltage  $v_{yz}$ , voltage across the load  $v_{load}$ , current flowing through the load  $i_{load}$ , terminal voltage  $v_{ug}$ , leakage current  $i_{cpc}$ , CMV  $v_{cm}$  and voltage across switched capacitor  $C_{S1}$   $v_{CS1}$ , current flowing through the switched capacitor  $C_{S1}$   $i_{CS1}$  for the proposed five-level inverter with variable line frequency  $f_g$  from 50 Hz to 60 Hz. Fig. 18 shows the shows the experimental waveforms of output voltage  $v_{yz}$ , voltage across the load  $v_{load}$ , current flowing through the load  $i_{load}$ , terminal voltage  $v_{ug}$ , leakage

current  $i_{cpc}$ , CMV  $v_{cm}$  and voltage across switched capacitor  $C_{S1}$   $v_{CS1}$ , current flowing through the switched capacitor  $C_{S1}$   $i_{CS1}$  for the proposed five-level inverter with step change in the input voltage  $V_{PV}$  from 100 V to 80 V. During all these dynamic operating conditions, the proposed five-level inverter is operating successfully.

## VII. CONCLUSION

A five-level transformerless inverter for the alleviation of the leakage current in the PV systems by considering the effect of SDJC is proposed in this paper. The proposed topology generates five levels in the inverter output voltage by using two switched capacitors. The switched capacitors discharge for the voltage levels  $\pm V_{pv}/2$  and charges for the remaining voltage levels. The switched capacitors in the proposed topology have less charging and discharging currents. The switched capacitors in the five-level inverter also have low voltage and current ripples. The two switched capacitors used in the five-level inverter have self-charge balance feature. Due to subsequent charging and discharging in the switching periods, the size of switched capacitors used in the five-level inverter will be less. Also, the two switched capacitors used in the proposed five-level inverter are discharged in parallel. This results in the reduction of the switched capacitor value to half. The proposed five-level inverter also minimizes the ripple in the buffer capacitor of the PV panel. Further, the proposed five-level inverter effectively utilizes the PV source as the series connected switch capacitors, and the DC bus buffer capacitor across the PV source comes in parallel in each switching period. The proposed five-level also generate three levels in the output voltage for the lower modulation index. In addition to the above discussed, the proposed five-level inverter maintains CCMV by taking into account the effect of SDJC. This helps in alleviating the CMC and leakage current in the PV systems. As a result, the size of common mode chokes and EMI filters required at the output of five-level inverter may be minimized.

## REFERENCES

- [1] N. V. Kurdkandi, M. G. Marangalu, O. Husev, A. Aghaie, Md. R. Islam, Y. P. Siwakoti, K. M. Muttaqi, and S. H. Hosseini, "A new seven-level transformer-less grid-tied inverter with leakage current limitation and voltage boosting feature," in *IEEE Journal of Emerging and Selected Topics in Industrial Electronics*, vol. 4, no. 1, pp. 228–241, Jan. 2023.
- [2] H. Tian, M. Chen, G. Liang, and X. Xiao, "A single-phase transformer-less common-ground type PV inverter with active power decoupling," in *IEEE Transactions on Industrial Electronics*, vol. 70, no. 4, pp. 3762–3772, Apr. 2023.
- [3] A. M. Mahfuz-Ur-Rahman, M. R. Islam, K. M. Muttaqi, M. A. Rahman, and D. Sutanto, "An advanced modulation technique for transformerless grid connected inverter circuits used in solar photovoltaic systems," in *IEEE Transactions on Industrial Electronics*, vol. 70, no. 4, pp. 3878–3887, Apr. 2023.
- [4] A. Srivastava and J. Seshadrinath, "A single-phase seven-level tripleboost inverter for grid-connected transformerless PV applications," in *IEEE Transactions on Industrial Electronics*, vol. 70, no. 9, pp. 9004–9015, Sept. 2023.
- [5] X. Zhu, H. Wang, R. Sun, H. Wang, X. Deng, and X. Yue, "Leakage current suppression of single-phase five-level inverter for transformerless photovoltaic system," in *IEEE Transactions on Industrial Electronics*, vol. 68, no. 11, pp. 10422–10435, Nov. 2021.
- [6] Z. Yao and Y. Zhang, "A doubly grounded transformerless PV grid-connected inverter without shoot-through problem," in *IEEE Transactions on Industrial Electronics*, vol. 68, no. 8, pp. 6905–6916, Aug. 2021.
- [7] H. K. Jahan, "A new transformerless inverter with leakage current limiting and voltage boosting capabilities for grid-connected PV applications," in *IEEE Transactions on Industrial Electronics*, vol. 67, no. 12, pp. 10542–10551, Dec. 2020.
- [8] H. Xiao, R. Wang, L. Zhou, Y. Liu, W. Hua, and M. Cheng, "Resonance network structuring method for zero-voltage-transition transformerless inverters," in *IEEE Transactions on Industrial Electronics*, vol. 69, no. 9, pp. 8905–8914, Sept. 2022.
- [9] I. Günsal, D. A. Stone, and M. P. Foster, "Suppressing leakage current for cascaded H-bridge inverters in renewable energy and storage systems," in *IEEE Transactions on Industrial Electronics*, vol. 68, no. 11, pp. 11035–11043, Nov. 2021.
- [10] Y. Liu, Y. Zhou, B. Guo, H. Wang, M. Su, X. Liang, and X. Pan, "Bimodal transformerless inverter with three switches," in *IEEE Transactions on Industrial Electronics*, vol. 69, no. 9, pp. 8972–8983, Sept. 2022.
- [11] F. Akbar, H. Cha, and H. -G. Kim, "Novel virtual-ground single-stage single-inductor transformerless buck-boost inverter," in *IEEE Transactions on Industrial Electronics*, vol. 68, no. 8, pp. 6927–6938, Aug. 2021.
- [12] N. Vosoughi, S. H. Hosseini, and M. Sabahi, "A new single-phase transformerless grid-connected inverter with boosting ability and common ground feature," in *IEEE Transactions on Industrial Electronics*, vol. 67, no. 11, pp. 9313–9325, Nov. 2020.
- [13] S. Jahan, M. F. Kibria, S. P. Biswas, M. R. Islam, M. A. Rahman, and K. M. Muttaqi, "H9 and H10 transformer-less solar photovoltaic inverters for leakage current suppression and harmonic current reduction," in *IEEE Transactions on Industry Applications*, vol. 59, no. 2, pp. 2446–2457, Mar.-Apr. 2023.
- [14] V. Sonti, S. Jain, V. Agarwal, and S. Bhattacharya, "Terminal voltage analysis for the transformerless PV inverter topologies in a single-phase system," in *IET Renewable Power Generation*, vol. 13, no. 15, pp. 2723–2739, Nov. 2019.
- [15] X. Guo and X. Jia, "Hardware-based cascaded topology and modulation strategy with leakage current reduction for transformerless PV systems," in *IEEE Transactions on Industrial Electronics*, vol. 63, no. 12, pp. 7823–7832, Dec. 2016.
- [16] M. J. Sathik, N. Sandeep, D. J. Almakhlles, and U. R. Yaragatti, "A five-level boosting inverter for PV application," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 4, pp. 5016–5025, Aug. 2021.
- [17] X. Zhu, H. Wang, W. Zhang, H. Wang, X. Deng, and X. Yue, "A single-phase five-level transformer-less PV inverter for leakage current reduction," in *IEEE Transactions on Industrial Electronics*, vol. 69, no. 4, pp. 3546–3555, Apr. 2022.
- [18] G. V. Bharath, A. Hota, and V. Agarwal, "A new family of 1- $\phi$  five-level transformerless inverters for solar PV applications," in *IEEE Transactions on Industry Applications*, vol. 56, no. 1, pp. 561–569, Jan.-Feb. 2020.
- [19] L. Zhang, K. Sun, Y. Xing, and M. Xing, "H6 transformerless full-bridge PV grid-tied inverters," in *IEEE Transactions on Power Electronics*, vol. 29, no. 3, pp. 1229–1238, Mar. 2014.
- [20] V. Sonti, S. Jain, and S. Bhattacharya, "Analysis of the modulation strategy for the minimization of the leakage current in the PV grid-connected cascaded multilevel inverter," in *IEEE Transactions on Power Electronics*, vol. 32, no. 2, pp. 1156–1169, Feb. 2017.
- [21] S. Jain and V. Sonti, "A highly efficient and reliable inverter configuration based cascaded multilevel inverter for PV systems," in *IEEE Transactions on Industrial Electronics*, vol. 64, no. 4, pp. 2865–2875, Apr. 2017.
- [22] X. Zhu, H. Wang, W. Zhang, H. Wang, X. Deng, and X. Yue, "A novel single-phase five-level transformer-less photovoltaic (PV) inverter," in *CES Transactions on Electrical Machines and Systems*, vol. 4, no. 4, pp. 329–338, Dec. 2020.
- [23] A. Jakhar and N. Sandeep, "Five-level common-ground-type boosting

inverter with lesser capacitor-stored energy,” in *IEEE Transactions on Power Electronics*, vol. 38, no. 12, pp. 15121–15125, Dec. 2023.

- [24] S. Kumari, A. K. Verma, S. N. U. R. Yaragatti, and H. R. Pota, “A five-level transformer-less inverter with self-voltage balancing and boosting ability,” in *IEEE Transactions on Industry Applications*, vol. 57, no. 6, pp. 6237–6245, Nov–Dec. 2021.
- [25] V. Anand, V. Singh, J. Sathik, and D. Almakhlles, “Single-stage five-level common ground transformerless inverter with extendable structure for centralized photovoltaics,” in *CSEE Journal of Power and Energy Systems*, vol. 9, no. 1, pp. 37–49, Jan. 2023.
- [26] M. Shahabadini, N. Moeini, M. Bahrami-Fard, and H. Iman-Eini, “HER-IC-based cascaded H-bridge inverter for leakage current suppression in PV systems,” in *IEEE Transactions on Power Electronics*, vol. 38, no. 3, pp. 4005–4014, Mar. 2023.
- [27] V. Hosseinkhani and M. Sarvi, “A new five-level inverter with reduced leakage current for photovoltaic system applications,” in *Protection and Control of Modern Power Systems*, vol. 7, no. 2, pp. 1–13, Apr. 2022.



Solar PV applications.

**MLN Vital** received his B.Tech. degree in Electrical and Electronics Engineering from JNTU, Hyderabad in the year 2008 and M.Tech. degree in Power Electronics from VIT university, Vellore in the year 2010. He is currently doing part-time Ph.D. at National Institute of Technology (NIT) Raipur. His areas of interest include multilevel inverter applications for



National Institute of Technology Raipur, India. His research interests include the grid-connected inverter for renewable energy generation.

**Venu Sonti** received B.Tech. degree in Electrical and Electronics Engineering from the Koneru Lakshmaiah College of Engineering, Guntur, India in the year 2011 and M.Tech. degree in Power Electronics and Drives from the National Institute of Technology Warangal, Warangal, India in the year 2013 and Ph.D. degree from National Institute of Technology Warangal, India. Currently, he is working as an Assistant Professor in



**Yam P. Siwakoti** received the B.Tech. degree in electrical engineering from the National Institute of Technology, Hamirpur, India, in 2005, the master's degree in electrical power engineering from the Norwegian University of Science and Technology, Trondheim, Norway, and Kathmandu University, Dhulikhel, Nepal, in 2010, and the Ph.D. degree in electronic engineering from Macquarie University, Sydney, NSW, Australia, in 2014. During 2014–2016, he was a Postdoctoral Fellow with the Department of Energy Technology, Aalborg University, Aalborg, Denmark. During 2017–2018, he was a Visiting Scientist with the Fraunhofer Institute for Solar Energy Systems, Freiburg, Germany. His research was the recipient of the series of awards including the most prestigious Friedrich Wilhelm Bessel Research Award from Alexander von Humboldt Foundation, Germany, in 2022, and the Green Talent Award from the Federal Ministry of Education and Research, Germany, in 2016. Dr. Siwakoti is currently an Associate Professor with the Faculty of Engineering and Information Technology, University of Technology Sydney. He is an Associate Editor for *IEEE Transactions on Power Electronics*, *IEEE Transactions on Industrial Electronics* and *IEEE Journal of Emerging and Selected Topics in Power Electronics*.



**Sze Sing Lee** received the B.Eng. (with Hons.) and Ph.D. degrees in electrical engineering from Universiti Sains Malaysia, George Town, Malaysia, in 2010 and 2013, respectively. From 2014 to 2019, he was a Lecturer/Assistant Professor with the University of Southampton Malaysia Campus, Gelang Patah, Malaysia. From 2018 to 2019, he was a Visiting Research Professor with Ajou University, Suwon, South Korea. He is currently an Assistant Professor with Newcastle University, Singapore. He is also a Chartered Engineer registered with the Engineering Council, U.K. His research interests include power converter/inverter topologies and their control strategies. Dr. Lee is also an Associate Editor for *IEEE Transactions on Industrial Electronics* and *IEEE Access*, and a Guest Associate Editor of *IEEE Transactions on Power Electronics*.



**Sachin Jain** received the B.E. degree in electrical engineering from the Bhilai Institute of Technology, Bhilai, India, in 2000, the M. Tech. degree in integrated power systems from the Visvesvaraya National Institute of Technology, Nagpur, India, in 2002, and the Ph.D. degree in power electronics from the Indian Institute of Technology, Bombay, Mumbai, India, in 2007. He is currently working as an Associate Professor with the National Institute of Technology, Raipur, India. Before joining NIT-RR, he had worked with NIT-Warangal as an Associate Professor and the Solar Energy Business Group of Schneider Electric as a Senior Design Engineer in the Research and Development Department, Bangalore. His research interests include power electronics applications in nonconventional energy conditioning, power quality, and distributed generation.