Optimized PI Gain in UPQC Control Based on Improved Zero Attracting Normalized LMS

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***Abstract*—An Improved Reweighted Zero Attracting Normalized Least Mean Square (IRZA-NLMS) based control scheme is applied in 4-wire Unified Power Quality Conditioner (UPQC) to mitigate current and voltage-based power quality issues. The IRZA-NLMS algorithm has increased efficiency with regard to exploratory rate, steady-state error, and overcoming the drawbacks of NLMS techniques. To raise convergence rate of active signals, the IRZA-NLMS algorithm uses an efficient threshold-based gain function and involvement of zero attracting term is used to determine the inactive signals to their optimum zero stage. In addition to IRZA-NLMS algorithm, a Self-Adaptive Multi Population Rao (SAMP-Rao) optimization is employed to evolve gains of the proportional integral (PI) controller. The SAMP- Rao increases diversity of solution search by splitting total considered population into sub-population groups, each of which searches for the optimal solution in a search space, ensuring that no single individual is trapped in a local minima and allowing for better exploration and exploitation search. The Integral Time Absolute Error objective function is used to optimize the gains of PI controller of DC and AC link voltage. In laboratory environment, the prescribed method is implemented through Micro-lab box processor with MATLAB interface.**

***Index Terms*—Harmonics, least mean square, local minima, optimization, PI gains, reactive components, voltage sag.**

I. Introduction

THE electrical utility companies must provide uninterrupted power with sinusoidal constant voltage magnitude to the customers [1]. This is increasingly more challenging as the number of non-linear loads and their scale is gradually growing [2]. Nonlinear appliances that depend on power electronics switches are commonly utilized in users and industrial usage of all utilities around world [3]. Due to the nonlinear property of the power electronics switches, causes surges in power quality issues such as harmonic, voltage inconstancy, noise, electric devices heating and redundant neutral currents in the 4-wire system [4]. Furthermore, the entire load on an electrical system is never considered balanced in distribution system [5]. Traditional passive filters have been employed in the past to mitigate these known power quality (PQ) issues [6].

But these have some restrictions such as fixed compensation, enormous size, difficulty in tuning dependency filter parameters and resonance with source impedance have awakened the requirement for active power filters (APF) and hybrid power filters [7]–[9]. The unified power quality conditioner (UPQC) is a hybrid active power filter concurrently it can perform the functionality of series and shunt APFs [10], [11]. The series APF provides the compensating duty, when the supply voltage unbalances, voltage harmonic and voltage imbalances happen, while shunt APF mitigates for current-related harmonics, load unbalancing and neutral compensation of current [12]. The PQ mitigation capability of UPQC is mainly determined by the generation of reference signal and compensation control algorithm [13].

Many literatures have presented several adaptive filtering techniques for generation of reference signals, fundamental active, reactive and harmonic components extraction [14]. Especially, adaptive filtering-based least mean square (LMS) and its modified versions have been commonly used, due to their low complexity and simple implementation in power quality areas for its improvement [15]. However, because traditional LMS algorithms are sensitive to scaling of their training input waves, choosing an appropriate step size to guarantee stability is difficult [16]. An enhanced normalized least mean square (NLMS) algorithm has been proposed to resolve this issue by normalizing strength of training input signals [17]. Using NLMS, improved efficiency can be obtained in a steady state. Another effective zero attracting (ZA) method has been anticipated using addition of ZA term into the iterations of LMS algorithm, which speeds up the initializing state and convergence rate [18]. However, the ZA-LMS algorithm is extremely complex and is still susceptible to input signal filtering [19]. The ZA techniques were consequently implemented in NLMS algorithm to achieve ZA-NLMS algorithm [20]. Further, to increase performance of ZA-NLMS technique, reweighted ZA-NLMS (RZA-NLMS) method is reported [21] which improves stability. An improved reweighted zero attracting (IRZA) based algorithm is proposed in [22] to overcome PQ problems posed due to non-linear loading and sudden starting of induction motor. The algorithm removes DC offset from load current while preserving motor's unbalanced loading and starting. The authors are encouraged by the comprehensive IRZA literature study to de-

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velop an IRZA and NLMS algorithm-based control that mitigates PQ issues and keeps harmonics within the standard limits of the UPQC system. The convergence rate is accelerated by the IRZA-NLMS and has a lower mean square error than usual LMS [23]. With the aid of theoretical inspection, IRZA-NLMS is better on any loads both transient dynamic and steady-state performance for any system when compared to normalized LMS. It provides harmonics elimination of nonlinear loads and voltage regulation under load-varying conditions.

Estimation of fundamental parameters from the adaptive filtering techniques is necessary for UPQC control algorithm design. Apart from fundamental estimation, some studies have shown that proportional integral (PI) controller also plays a major part in the reference signal generation in UPQC controller [24]. The PI controller is designed to settle DC link and load terminal voltage at their respective level. To get the required voltage level in any control technique, tuning PI controller parameters is an essential requirement [25]. The studies proposed advanced optimization algorithms for different meta-heuristic algorithms to address PI design flaws and enhance its performance. Certain meta-heuristic algorithms are well accepted such as particle swarm optimization (PSO), harmony search algorithm (HSA) and ant colony optimization (ACO), etc [26]. In the last decade, numerous special meta-heuristic algorithms have been proposed such as crisscross optimization, galaxy-based search algorithm, lion optimization, teaching learning based optimization (TLBO), Jaya algorithm, Rao algorithm, etc. The GA depends on selection operator, population size, probability of crossover and mutation, etc; ABC is determined by number of scout bees, onlooker bees, employed bees, its limit, and other factors; PSO relies on its inertia weight, social and cognitive parameter; HSA is controlled by the number of improvisations, the rate of harmonic memory consideration, and other factors [27]. Similarly, each algorithm has its benefits and drawbacks but most of the optimization (except TLBO, Jaya, and Rao algorithms) depends on their control parametric specification with other controlling parameters. Accurate tuning of control-specific parameters in the algorithm is a lengthy procedure that raises computational efforts. Due to this reason R. V. Rao proposed the "Rao" algorithm, which is a specific type and parameter-less optimization technique [28]. The advanced methods of optimization depend on multi-population search mechanism employed to maximize the variety of searches by splitting the overall population into several subgroup population categories [29]. However, the incorrect subpopulation category number may lose diversity of search method. To avert these challenges, self-adaptive multi population (SAMP) algorithm and simple Rao algorithm are integrated to obtain benefits of the multi-population search process in basic Rao algorithms [30]. New SAMP-Rao techniques are adaptive to alter the population of subgroups. This tracks the intensity of the search process' exploration and exploitation based on best fitness value.

This paper introduces a 3-phase 4-wire UPQC for distribution system and an IRZA-based NLMS control for PQ mitigation. The series APF of the UPQC system is regulated to preserve voltage stability and to compensate for sag in supply voltage, harmonic and load terminal voltage imbalance. While, to reduce the supply current from harmonics, reactive power and neutral current, shunt APF section of UPQC is operated. The DC link and AC terminal voltage are held constant by IRZA-NLMS control algorithm through shunt and series APF respectively. The control algorithm IRZA-NLMS is easy to implement and has high convergence speed, less dynamic oscillation and low steady-state error. A new variable zero-attracting parameter was used by this algorithm in the zero-attracting term. It also solves the disadvantage of the gradient descent method by employing a new variable step size in the gradient correction term to reduce converge time and trade-off steady state miss compensation. To optimize the gain value of PI at DC and AC bus voltages, the SAMP-Rao algorithm was utilized, it is a specific and parameterless optimization approach. An unconstrained optimization based on ITAE has been developed with voltage errors of DC and AC bus. Gains of PI are determined by SAMP-Rao algorithm on ITAE problem. The main goal is to get the optimized PI gains from SAMP-Rao optimization, PCC voltage regulation and power quality improvement under connected nonlinear loads using IRZA-NLMS algorithm in UPQC.

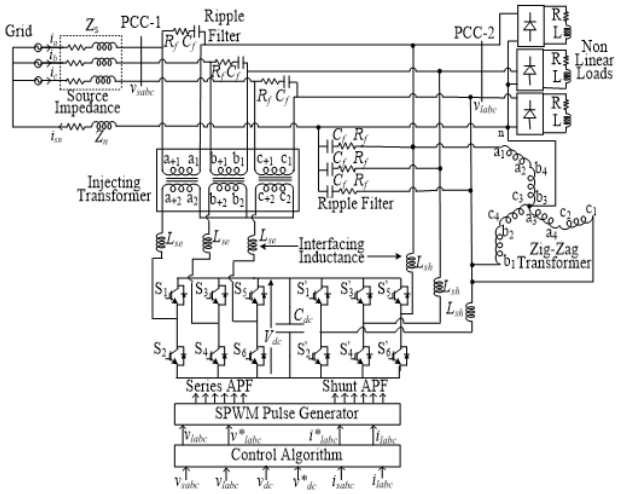


Fig. 1. Schematic diagram of 3-phase 4-wire UPQC.

II. Description of Power Circuit Diagram

The 3-phase, 4-wire UPQC device with zig-zag transformer for maintaining neutral current compensation to nonlinear load is schematically depicted in Fig. 1. In 4-wire system, the Z_s signifies line impedance of source side, whereas Z_n denotes the neutral line impedance.

It comprises voltage-controlled 3-leg converter employed as series and shunt-connected power filter. A common C_{dc} capacitor is attached to DC link voltage (V_{dc}) of both power filters. Shunt APF is linked through the load terminal which makes the load voltage ideally balanced and sinusoidal with the desired magnitude at PCC-2. The APF series is connected by a 3-phase injection transformer between the supply and the load terminal.

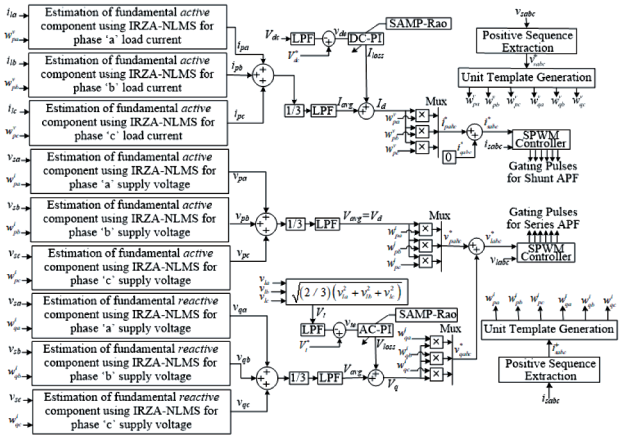


Fig. 2. Control arrangement of reference signal generation for UPQC using IRZA-NLMS algorithm.

As said in Fig. 1, main windings of injection transformers are connected to a star connection, and the secondary side windings are joined in series to supply system. A ripple filter (R_f, C_f) is taken across secondary winding of series transformer to get rid of high-frequency switching ripple content. Similar R_f, C_f filter of same value is also connected across each leg of the shunt APF to eliminate switching noise. The circuit variables used for simulation work are depicted in Appendix A1.

III. Control Scheme

Control arrangement designed for 4-wire UPQC controller is depicted in Fig. 2. Load currents (i_{labc}), supply voltage (v_{sabc}) source currents (i_{sabc}) and dc-link voltage (V_{dc}) are the sensed feedback signals employed for generation of reference signal to shunt APF. Similarly, the load voltages (v_{labc}), supply voltage (v_{sabc}) and source currents (i_{sabc}) are sensed for deriving the gate pulses for series APF. Finally, these reference signals are taken to create switching pulses for IGBT switches. Control algorithm consists of the IRZA-NLMS algorithm for estimating the basic active and reactive components; detection of positive sequence components for unit template generation; unit template generation determination; generation of grid reference supply current and generation of load reference voltage. The control scheme includes the generation of reference signals for both VSC. Furthermore, to acquire the best gains of PI-controller in UPQC controller scheme, SAMP-Rao optimization technique is used to obtain values.

A. Reference Signals Estimation for Both VSC

Reference signal generation for both VSC begins with IRZA-NLMS algorithm. It is utilized to detect fundamental active and reactive components of disturbed load current and supply voltages. Later on, unit template generation through estimation of positive sequence components from the source end signals.

1. Fundamental Active and Reactive Components Estimation Using IRZA-NLMS

An idea behind in IRZA-NLMS algorithm is the use of reweighted zero-attracting (ZA) term and normalized LMS. The NLMS consecrates an actual time-changing step size and a reweighted ZA term for each adaptive filter coefficient that adapts by a logarithmic amount of input vector. The various step sizes and reweighted ZA aid in increasing the convergence rate along with mean square error of steady-state by using the specific gains of each input signal. The IRZA-NLMS has the fastest convergence rate and optimal performance in the steady state compared to traditional LMS, NLMS, etc. Here the IRZA-NLMS procedure is employed to determine fundamental active load current component (i_{pa}) from polluted load current (i_{la}) at n^{th} sample for "phase *a*" which is estimated as

$$i_{pa}(n+1)=i_{pa}(n)+\frac{2}{w_{pa}^{v\,T}(n)w_{pa}^{v}(n)+\dfrac{\gamma}{\left|e_{pa}(n)\right|+\delta}}e_{pa}(n)w_{pa}^{v}(n)-\frac{\rho\,\mathrm{sgn}\left[i_{pa}(n)\right]}{1+\varepsilon\left|i_{pa}(n)\right|}$$
$$e_{pa}(n)=i_{la}(n)-w_{pa}^{v}(n)i_{pa}(n) \tag{1}$$

where e_{pa} is error between desired and actual output for phase *a* of system. The term $(2/(w^{v}_{pa}{}^{T}(n)\ldots))$ is an NLMS which is a positive constant that governs convergence speed. While NLMS method can improve the LMS algorithm's estimate performance, it is unable to make use of the sparse multipath sparsity feature. So, to solve this issue, the ZA approach is applied and included in the algorithm. ZA parameter called ρ is used to balance estimating behavior and sparsity penalty; it must be minimal to prevent diving by zero. To rapidly attract non-dominant channel taps to zero, use the zero attractor $\rho\mathrm{sgn}[i_{pa}(n)]$. Even gradient noise amplification that LMS invokes can be lessened by the NLMS and IRZA algorithms. The constants γ, ε and δ are the positive constants that help reduce the gradient noise. Only certain signals of magnitude comparable to $1/\varepsilon$ are influenced by the reweighted zero attractor and there is no shrinkage used on signals. The IRZA-NLMS bias terms can be reduced in this manner. Similarly, other two fundamental active load current component phases i_{pb} and i_{pc} are also achieved.

The fundamental active voltage component (v_{pa}) from the supply voltage at n^{th} sample for "phase *a*" is computed as

$$v_{pa}(n+1)=v_{pa}(n)+\frac{2}{w_{pa}^{i\,T}(n)w_{pa}^{i}(n)+\dfrac{\gamma}{\left|e_{pa}(n)\right|+\delta}}e_{pa}(n)w_{pa}^{i}(n)-\frac{\rho\,\mathrm{sgn}\left[v_{pa}(n)\right]}{1+\varepsilon\left|v_{pa}(n)\right|}$$
$$e_{pa}(n)=v_{sa}(n)-w_{pa}^{i}(n)v_{pa}(n) \tag{2}$$

Likewise, the fundamental active voltage component of remaining phases (v_{pb}, v_{pc}) is also computed by using the similar approach. Now the fundamental reactive voltage component (v_{qa}) from the supply voltage at n^{th} sample for "phase *a*" is computed as

$$v_{qa}(n+1)=v_{qa}(n)+\frac{2}{w_{qa}^{i\,T}(n)w_{qa}^{i}(n)+\dfrac{\gamma}{\left|e_{qa}(n)\right|+\delta}}e_{qa}(n)w_{qa}^{i}(n)-\frac{\rho\,\mathrm{sgn}\left[v_{qa}(n)\right]}{1+\varepsilon\left|v_{qa}(n)\right|}$$
$$e_{qa}(n)=v_{sa}(n)-w_{qa}^{i}(n)v_{qa}(n) \tag{3}$$

Also, the reactive voltage components of remaining two phases (v_{qb}, v_{qc}) are similarly computed with the same approach. As in Fig. 2, average active components of voltage (V_d), reactive voltage quantity (V_{avg}), and active current quantity (I_{avg}) will be used to produce further internal signals.

2. Positive Sequence Estimation for Unit Template Generation

During voltage harmonics situations, the positive sequence grid voltage is essential for the accurate estimate of synchronization unit vector. The methods for finding the positive sequence quantity at all harmonics present in source signals vary. The transformations mentioned in [31] are used to get the positive sequence quantity from the source end. Therefore, using a symmetrical quantity method, symmetrical-phasor components (V_a^+, V_b^+, V_c^+) of a 3-phase source voltage are obtained. Fig. 2 indicates the positive sequence voltages (V_{sabc}^+) are retrieved from source voltage which are primarily sensed to produce synchronized unit templates for the Shunt APF. In similar ways, the positive sequence current (i_{sabc}^+) is acquired to get synchronized unit vector for series active power filter.

3. Estimation of Unit Templates

PCC-1 voltage magnitude (V_s) as seen in Fig. 1 is essential for minimizing the components of loss under different PQ conditions. Unit templates of in-phase weight signals ($w_{pa}^v, w_{pb}^v, w_{pc}^v$) and quadrature weight signals ($w_{qa}^v, w_{qb}^v, w_{qc}^v$) are obligatory to create symmetrical components from PCC-1 voltages [17], [22].

Similarly, unit templates of in-phase weight signals ($w_{pa}^i, w_{pb}^i, w_{pc}^i$) and quadrature weight signals ($w_{qa}^i, w_{qb}^i, w_{qc}^i$) from source current are developed with peak magnitude current (I_s) acquired at PCC-1 for Series APF.

4. Reference Source Current Estimation for the Grid

To eliminate DC voltage fluctuation, a PI controller is widely utilized. The PI controller input is an error between the actual capacitor voltage and targets. Its output is applied to the reference current component in the active components to create a new reference current component. So, for source current, the total active components current (I_d) is estimated as the average sum of all phases active components [$I_{avg} = \left(i_{pa} + i_{pb} + i_{pc}\right)/3$] of load current and active loss components (I_{loss}) of current needed to stabilize the DC link capacitor (C_{dc}).

$$I_d = I_{avg} + I_{loss} \tag{4}$$

Also, the I_{loss} is known as current loss components that meet the losses in the UPQC system, and it is calculated as follows using the PI output at the DC link bus.

$$I_{loss}(t) = I_{loss}(t-1) + k_{pd}\left[V_{de}(t) - V_{de}(t-1)\right] + k_{id}V_{de}(t) \tag{5}$$

where, at time instant t current loss term $I_{loss}(t)$ is an active part of source current, k_{pd} and k_{id} are the PI-gains. The V_{de} is an input parameter for PI-controller, obtained when reference dc link voltage (V_{dc}^*) is subtracted from the actual (V_{dc}) dc-bus voltage.

A 3-phase reference supply current is obtained by taking product of active components of source current with unit vectors. So, only active components contribute to generation of reference source currents. Therefore, active reference currents ($i_{pa}^*, i_{pb}^*, i_{pc}^*$) for source are

$$i_{pa}^* = I_d \times w_{pa}^v,\ i_{pb}^* = I_d \times w_{pb}^v,\ i_{pc}^* = I_d \times w_{pc}^v \tag{6}$$

The 3-phase source current is considered zero for the reactive quantity. Because of the absence of zero sequence components in the system, reference source current should be in phase with grid voltage. Therefore, the reference supply currents ($i_{sa}^*, i_{sb}^*, i_{sc}^*$) for each phase are calculated as the sum of active and reactive respective components.

$$i_{sa}^* = i_{pa}^* + 0,\ i_{sb}^* = i_{pb}^* + 0,\ i_{sc}^* = i_{pc}^* + 0 \tag{7}$$

The 3-phase source reference current (i_{sabc}^*) is associated with the detected actual source currents (i_{sabc}) and is set as input to a sinusoidal pulse width modulation (SPWM) controller to produce the gating pulse signals to the IGBT switches of the APF shunt.

5. Generation of Reference Load Voltage

To keep source current and load voltage in phase, the total active components ($V_d = \left(v_{pa} + v_{pb} + v_{pc}\right)/3$) of the load voltage is one-third of supply voltage (V_{avg}) active components, i.e.

$$V_d = V_{avg} \tag{8}$$

The load end voltage (V_q) total reactive quantity is calculated as sum of average reactive components (V_{avg}) and extra loss reactive components (V_{loss}) required to maintain the specific terminal voltage.

$$V_q = V_{avg} + V_{loss} \tag{9}$$

The V_{loss} is a supply voltage loss component and it is estimated by AC bus PI controller output as

$$V_{loss}(t) = V_{loss}(t-1) + k_{pt}\left[V_{te}(t) - V_{te}(t-1)\right] + k_{it}V_{te}(t) \tag{10}$$

where, at t^{th} time instant, voltage loss term $V_{loss}(t)$ is treated as reactive part of load voltage, k_{pt} and k_{it} are the PI-gains of AC link. The term V_{te} is input parameter for this PI-controller, obtained when reference and actual load terminal voltages are subtracted as demonstrated in Fig. 2. The estimation of the reference load voltage ($v_{la}^*, v_{lb}^*, v_{lc}^*$) comprises active and reactive components. Hence, 3-phase active in-phase ($v_{pa}^*, v_{pb}^*, v_{pc}^*$) and reactive quadrature ($v_{qa}^*, v_{qb}^*, v_{qc}^*$) reference load voltage components are calculated as

$$\begin{aligned} v_{pa}^* &= V_d \times w_{pa}^i,\ v_{pb}^* = V_d \times w_{pb}^i,\ v_{pc}^* = V_d \times w_{pc}^i \\ v_{qa}^* &= V_q \times w_{qa}^i,\ v_{qb}^* = V_q \times w_{qb}^i,\ v_{qc}^* = V_q \times w_{qc}^i \end{aligned} \tag{11}$$

where the V_d is a total amount of the active components. Likewise, V_q is a total reactive component of reference load voltage value provided by $V_q = V_{avg} + V_{loss}$. Reference load voltages (v^*_{la}, v^*_{lb}, v^*_{lc}) are further calculated by summing these active as well as reactive quantities for each phase. The computed error values among reference 3 phases' load voltages (v^*_{sabc}) and actual 3-phase load voltages (v_{labc}) are passed over SPWM to generate switching signals.

B. PI Controller Tuning With SAMP-Rao Technique

In this paper, PI gains are implemented using SAMP-Rao-1 optimization to improve the dynamic response of 4-wire UPQC. The SAMP-Rao-1 algorithm is free from specific control parameters and metaphor-less heuristic search algorithms [28], [30]. It inclines to find best response and eliminate worst response. It is accomplished by lowering the predefined fitness feature on the UPQC device to improve transient dynamic behavior of both DC link and AC link voltage. Different performance specifications may be used to create the fitness function in the time domain, one of which is as follows:

$$F(K)=\min\{\text{ITAE}[(1-e^{-\rho})(M_p + E_{ss}) + e^{-\rho}(t_s - t_r)]\} \quad (13)$$

where $K=[k_p, k_i]$ is a parameter of PI gains. The ITAE, M_p, E_{ss}, t_s and t_r are ITAE, maximum overshoot, steady state error, settling and rising time respectively parameters required in time domain. Value ρ has an impact on system parameters since it is a weighting element. The consequence of ρ<0.7 on system parameters is to minimize t_s and t_r; whereas, if ρ>0.7 on system parameters is to decrease M_p and E_{ss}.

Optimal gains estimation is an unconstrained optimization problem in DC and AC link terminal voltage error reduction. Objective functions ITAE-1 and ITAE-2 are used for DC PI gains and AC PI gains, respectively. The gain of both PI controllers has some unknown variables such as k_{pd}, k_{id} and k_{pt}, k_{it} respectively. ITAE-1 function is obtained by subtracting reference DC link voltage (V^*_{dc}) from the actual detected DC voltage(V_{dc}). Similarly, error is caused by the reference terminal voltage (V^*_r) and actual measured terminal voltage (V_t). These functions aim to calculate optimum values of all unknown variables (k_{pd}, k_{id}, k_{pt}, and k_{it}) while converging the error towards zero with minimum objective function. During process, all the worst responses are eliminated and moving near to best responses is strategy of SAMP-Rao algorithm for any optimization process. Provided that the k^{th}-candidate solution of the j^{th} element at iteration i; $X_{j,k,i}$ upgraded value $X'_{j,k,i}$ is determined in

$$X'_{j,k,i} = X_{j,k,i} + r_{j,i}\left(X_{j,\text{best},i} - X_{j,\text{worst},i}\right) \quad (14)$$

where $X_{j,\text{best},I}$ is measured value of best candidate's j^{th} variable with best fitness value. Similarly $X_{j,\text{worst},i}$ is measured value of worst candidate's j^{th} variable with worst fitness value. The $r_{j,i}$ is random number between 0 and 1. The term 'solution' represents one or more decision variable values that cascaded to form a vector.

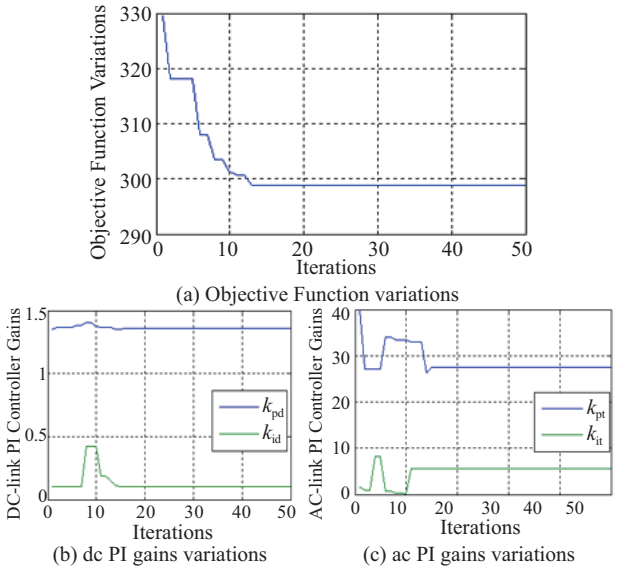
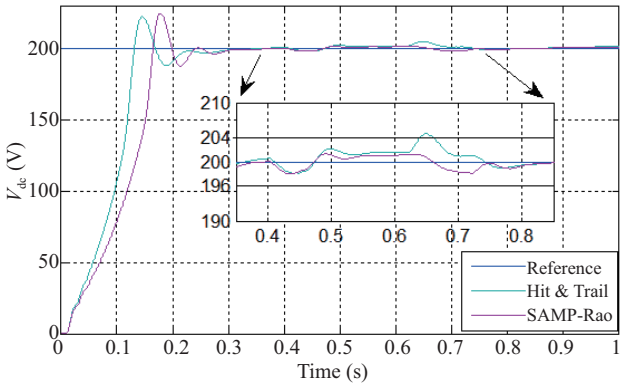


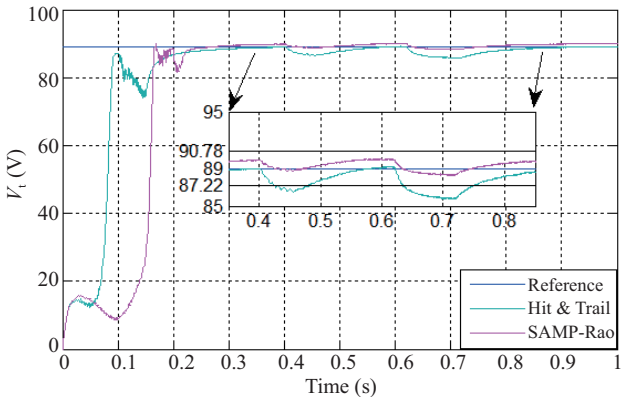
Fig. 3. SAMP-Rao-1 optimization performance study for determining PI gains values.

In MATLAB/SIMULINK environment this algorithm is implemented in UPQC for PI tuning. The best PI controller gains (k_{pd}, k_{id}, k_{pt}, and k_{it}) are determined with optimum objective function $F(K)$ is 298.92 as shown in Fig. 3(a). In an estimated fifty iterations, the SAMP-Rao-1 method employs twenty candidates for four unknown design factors. Fig. 3(b) determines the k_{pd}, k_{id} variation for fifty iterations on dc PI controller's gains which are steady at 1.362 and 0.1014 values respectively. Further, Fig. 3(c) presents k_{pt}, k_{it} variation for fifty iterations on ac PI controller's gains which are landed at 27.562 and 5.544 respectively.

The response nature of bus voltages are depicted in Fig. 4(a)-(b) respectively obtained with PI optimal values through SAMP-Rao algorithm. The enlarged section of obtained voltage natures under various above-mentioned PQ fluctuations is also described in Fig. 4(a)-(b). The specified band for underdamped system is governed at 100% of absolute value (i.e. 200 V and 89 V) and 2% acceptance band (i.e. 196 V-204 V and 87.22 V-90.78 V) is portrayed in Fig. 4. It shows that using optimal values significantly improves the reaction time of both terminal voltages. It converges fast with a minimal overshoot. Although the DC link voltage has almost same higher peak overshoot (220 V) but settles fast for both controllers. From the magnified portion, both have a smaller steady-state error, and system response is quickly settled to reference value as related to Hit and Trial method. In load unbalancing scenario, the steady-state error is 2 V for SAMP-Rao, but it is less than a volt in other PQ changes as revealed in Fig. 4(a). But in Hit and Trial approach, it has much higher steady state error on DC link voltage under all the PQ cases i.e. (near to 4.5 V in load unbalancing case). Similarly, the steady-state error is less than 1 V for SAMP-Rao as depicted in Fig. 4(b). Moreover, with Hit and Trial method, it is more than 2 V during power quality



(a) Performance of SAMP-Rao-1 optimization in tuning DC link



(b) Performance of SAMP-Rao-1 optimization in tuning AC link

Fig. 4. Performance of SAMP-Rao-1 optimization on IRZA-NLMS algorithm to tune the DC and AC link with its zoomed portion.

problems in distribution system. When compared to Hit and Trial approaches, system responses of SAMP-Rao look superior in terms of considered performance characteristics under above said power quality difficulties. When compared to the exploratory scheme, the coefficients of PI for optimum values are derived from Fig. 4. The SAMP-Rao can develop DC and AC link terminal voltages more steadily and quickly. The other results in UPQC system with IRZA-NLMS control and optimized PI gains are discussed in the succeeding section.

IV. Simulation Performance

The discussed control algorithm is illustrated in Fig. 2. A 4-wire UPQC is modeled in the MATLAB software using power systems block-set toolbox with an ode5 solver using 10 μs sample time. The performance of the UPQC-focused IRZA-NLMS algorithm is examined under corrupted source voltage and non-linear load conditions. Order of voltage harmonics to be examined is 5th and 7th type with respective magnitude. Different PQ conditions such as sag voltage and unbalanced voltage sag are listed to determine system output in steady-state operating conditions. The parameters considered in Appendix A1 are utilized for simulation analysis of the proposed UPQC.

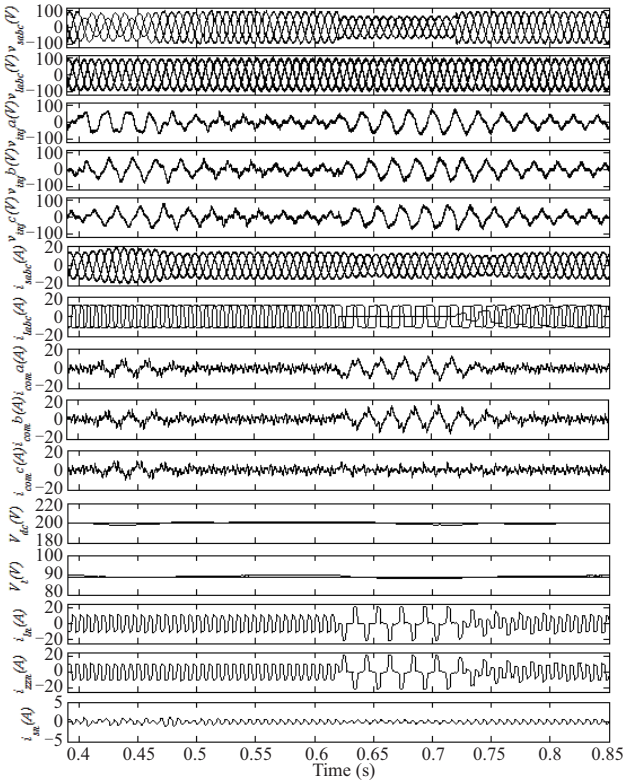


Fig. 5. Overall response of IRZA-NLMS algorithm on UPQC system under dynamic and steady-state operating conditions.

A. Overall Response of IRZA-NLMS Algorithm on UPQC Under Dynamic and Steady State Operating Conditions

Fig. 5 demonstrates dynamic effectiveness of four 4-wire UPQC systems with zig-zag transformers for mitigation of above-said power quality conditions. In Fig. 5 under various PQ conditions supply voltage (v_{sabc}), load voltage (v_{labc}), injection voltage by series transformer (v_{inja}, v_{injb}, v_{injc}), source current (i_{sabc}), load current (i_{labc}), compensator current (i_{coma}, i_{comb}, i_{comc}), dc-link voltage (V_{dc}), ac-link voltage (V_t) at load end PCC, load neutral current (i_{ln}), zig-zag neutral current (i_{zzn}) and source neutral current (i_{sn}) are illustrated. To distort the supply voltage, a 5th and 7th harmonic order voltage of 1/15th of the fundamental voltage is applied in series to source voltage. Moreover, a 30% voltage sag and 40% voltage unbalance in source voltage is assumed to validate its efficacy.

At 0.4 to 0.46 s voltage unbalance in "phase *a*", 0.5 to 0.56 s a voltage harmonic and 0.62 to 0.72 s a voltage sags are illustrated in Fig. 5 of the supply voltages (v_{sabc}) subplot. Despite the effects of PQ variations, the load voltage (v_{labc}) is sustained at the optimal value presented in Fig. 5 by an acceptable series filter injection voltage. The respective phase voltages injected by UPQC via series transformer are depicted in v_{inja}, v_{injb} and v_{injc} subplots. It has been proved that the terminal voltage may be adjusted to approximate reference necessary value by injecting correct voltage into the line using a series transformer. Similarly, UPQC compensates for both the case load current (i_{labc}) distortions and load removal state. It provides the sinusoidal source currents (i_{sabc}) waveform and is independent of the

TABLE I
IRZA-NLMS-BASED CONTROL FOR PERFORMANCE ANALYSIS IN UPQC

Power quality probiem	Parameters	% of harmonics and magnitude
Harmonics	Source voltage (v_{sab})	11.44%, 154.2 V
	Supply current (i_{sa})	4.47%, 155.6 A
	Load voltage (v_{lab})	3.98%, 590.8 V
	Load current (i_{la})	38.26%, 13.86 A

load current type distortions. Load of phase-*a* is disconnected at intervals 0.62 to 0.72 s in the subplot of load current (i_{labc}) in Fig. 5, resulting in load unbalancing situations in the system. Consequently, the output current was balanced and power factor remained at unity.

Current source profile is matched exactly at required levels and sinusoidal as UPQC provides the compensating current (i_{coma}, i_{comb}, and i_{comc}) in all phases shown respectively. The compensation current begins injecting harmonic current in the network that is equal to and opposite in nature of the load current. Control mechanism's effectiveness in the UPQC system is demonstrated by a small variation in DC-bus voltage (V_{dc}) and AC-link voltage PCC (V_t) with constant load voltages. As noticed in the subplot i_{sn}, zig-zag transformer distributes zero sequences fundamental current of the load neutral current (i_{ln}) created by imbalanced load while keeping source neutral current (i_{sn}) at almost zero. DC link voltage regulator's controller is capable of acting quickly and recovering the DC voltage and terminal voltage in a few cycles. Thus, under numerous multiple disruptions that occur concurrently with non-linear load, the UPQC device can operate efficiently and mitigate power quality problems.

Finally, harmonic spectrum analysis on UPQC is used to confirm the steady state condition for IRZA-NLMS control and its conclusions for harmonic distortion are shown in Table 1. It shows the harmonic spectrum of "line to line signals" for "phase *ab*" is measured for total harmonic distortion (THD) analysis. The results of other two phases are almost similar. The THD of a distorted supply voltage (v_{sab}) is 11.44% at 154.2 V, whereas the THD of a compensated load voltage (v_{lab}) is 4.47% at 155.6 V. The disrupted load current (i_{lab}) has a THD of 38.26% at 13.86 A, whereas supply current (i_{sab}) has THD of 3.03% at 13.72 A after correction. This demonstrates that the UPQC system with IRZA-NLMS filters can keep harmonic levels below 5%, which is the IEEE-519-2014 standard's point of reference.

V. EXPERIMENTAL RESULTS

Under nonlinear load, the IRZA-NLMS control method is applied based on response and characteristics for UPQC. A 4-channel digital storage oscilloscope, model DSO-X-2004A, was used to record all waveforms. Fluke-43B power quality analyser, manufactured by FLUKE, was utilized to record the steady-state results. The UPQC prototype has been made in lab using d-SPACE Micro Lab Box-based processor at 40 µs sampling time as shown in Fig. 6. The power quality (PQ) issues involving voltage sag, voltage unbalance, load removal, neutral current compensation, dynamic performance of UPQC has

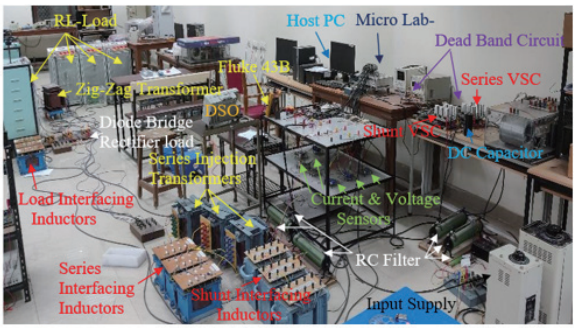


Fig. 6. Experimental setup of UPQC in 3-phase 4 wires system using Voltage Source Converters.

TABLE II
STEADY STATE PERFORMANCE SUMMARY OF UPQC

Nature of disturbance	Quantity in RMS			
	Source voltage (v_{sab})	Source current (i_{sa})	Load voltage (v_{lab})	Load current (i_{la})
Voltage harmonic	108.8 V, THD 11.3%	5.35 A, THD 4.5%	109.4 V, THD 4.8%	4.54 A, THD 25.3%
Voltage unbalance	99.1 V, THD 2.7%	6.13 A, THD 4.2%	109.30 V, THD 3.5%	4.56 A, THD 25.3%
Voltage sag	101.6 V, THD 3.3%	6.18 A, THD 3.8%	109.40 V, THD 4.2%	4.56 A, THD 25.3%

been examined. However, the voltage sag and neutral current compensation performance are depicted in Fig. 7. The steady-state performance of UPQC utilizing an IRZA-NLMS control approach is shown for voltage harmonics compensation, and rest results are provided in Table 2. Experimental data of prototype are mentioned in Appendix A2. Detailed discussion of performance of system is given below.

A. Hardware Set for UPQC

Micro Lab Box is made by NXP (Freescale), QorlQ P5020, dual-core, 2 GHz, with programmable FPGA Xilinx® Kintex®-7 XC7K325T as shown in Fig. 6. The 3 phase voltage and current have been sensed using LEM made LV-25P and LA-55P sensors respectively. The sensed voltage and current signals have been sent to controller through A/D channel for processing in processor. After processing modelled control algorithms in processor, the gate signals generated are taken out from controller through digital in-out (DIO) channel. A FLUKE-made single phase power quality analyzer (43B) has been used to record the steady state performance.

B. Dynamic Response of UPQC During Sag Mitigation

Fig. 7 demonstrates the compensation of −10% voltage sag issues using 4-wire UPQC with IRZA-NLMS-based control algorithm. The nature of source voltage (v_{sab}) in CH1, load voltage (v_{lab}) in CH2, source current (i_{sa}) in CH3 and load current (i_{la}) in CH4during the voltage sag occurring in phase '*ab*' is indicated in Fig. 7(a). As observed in Fig.7(a) in CH1, sag in the supply voltage (v_{sab}) causes voltage decreases of 0.9

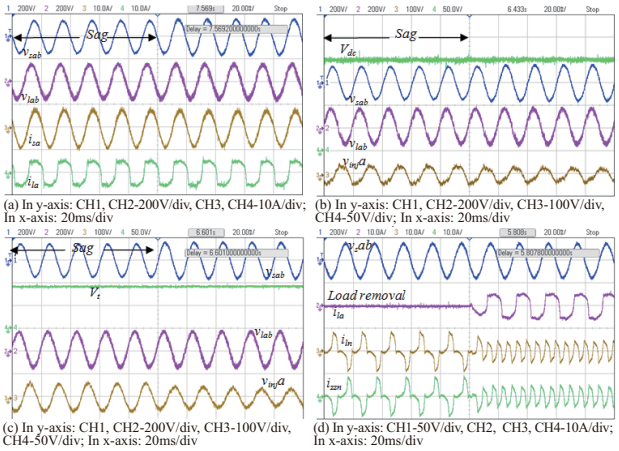


Fig. 7. Dynamic response of UPQC during (a) sag; (b) sag disturbance with DC link variation; (c) sag disturbance with AC link variation and (d) neutral current compensation.

per unit. The load voltage (v_{lab}) in CH2 after compensation is set back to its intended 110 V RMS value as illustrated in Fig. 7(a)-(c). After compensation, load voltage is returned to its ideal value with no interruptions.

As in Fig. 7(a) in CH3, amplitude of source current increases in response to supply voltage changes. It indicates that the UPQC control techniques preserve source current sinusoidal despite the impacts of load current harmonics. DC bus voltage variations during sag disturbance can be observed in Fig. 7(b) and it is settling at the desired 200 V level after little variation of 2 V-3 V in DC link voltage. From Fig. 7(b) throughout voltage sag excursion the necessary required injected voltage by series transformer is in-quadrature. Load voltage (v_{lab}) in CH2 is maintained sinusoidal with 110 V RMS level by injecting required compensator voltage ($v_{\text{linj}a}$) in CH3 for phase '*a*'. Similarly, terminal voltage variations can be noticed in Fig. 7(c) which is maintained at intended 89 V level. The necessary compensated voltage ($v_{\text{linj}a}$) in CH3 for phase '*a*' injected by series transformer is provided with required magnitude.

Fig. 7(d) depicts role of obtaining neutral current compensation during load removal. Source voltage (v_{sab}) in CH1, load current (i_{la}) in CH2, load neutral current (i_{ln}) in CH3 and neutral current of zig-zag transformer (i_{zzn}) in CH4 are noted in Fig. 7(e) wave shape. From the waveforms of Fig. 7(d), the zero sequence current generated by zig-zag transformer seems to be in perfect phase opposition to the neutral current. Because of this, the source neutral current has almost completely disappeared, enabling the UPQC to provide harmonic current in addition to zero-sequence current. The performance for other PQ disturbances is also found satisfactory. The 3-phase 4-wire UPQC dynamic performance during sag with IRZA-NLMS-based control algorithm is managing to compensate for power quality issues successfully.

C. Steady State Performance of UPQC With IRZA-NLMS Control

Fig. 8(a)-(j) demonstrates the steady-state execution of UPQC for Phase '*ab*' for the duration of supply voltage harmonics present in line. Fig. 8(a) displays supply voltages (v_{sab}) with distortions in it with compensated supply current (i_{sa}). Fig. 8(b) depicts phase load voltages (v_{lab}) after compensation with load current (i_{la}) with its RMS value. Series injection voltage ($v_{\text{inj}a}$) injected by UPQC via series transformer is depicted in Fig. 8(c) subplots of phase '*a*' with compensated source current (i_{sa}). Required compensating current ($i_{\text{com}a}$) of phase '*a*' is illustrated in Fig. 8(d) with load current (i_{la}). For supply voltages, the total harmonic distortions (THD) shown in Fig. 8(e) is 11.30%. The THD after compensation for the source current (i_{sa}) is also 4.5%, as displayed in Fig. 8(f). The THD % for load voltage is given in Fig. 8(g) and load current THD value is 25.3% described in Fig. 8(h) with an RMS value of 4.54 A. After compensation load voltages and source currents are within 5% THD level with desired magnitude.

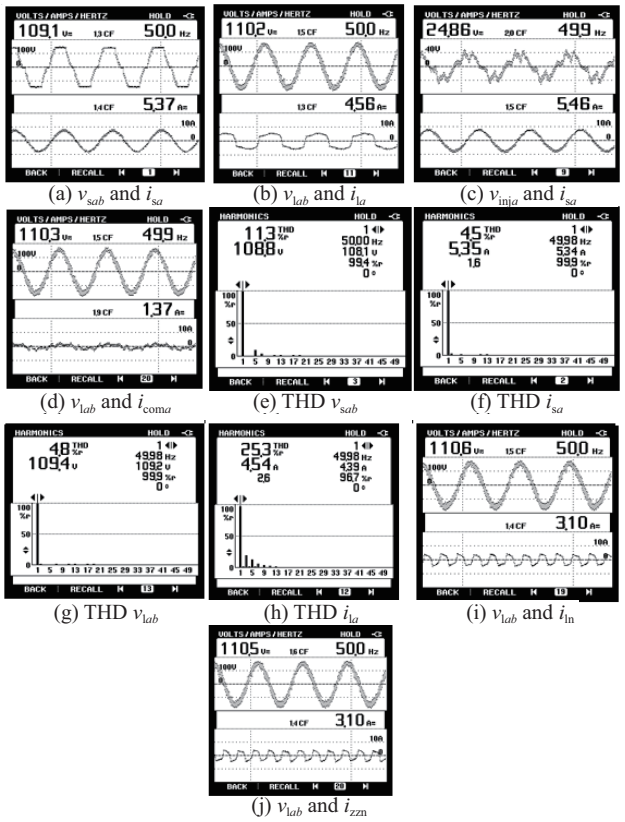


Fig. 8. Steady-state response of UPQC using IRZA-NLMS-based control algorithm during voltage distortions in supply voltage.

Fig. 8(i)-(j) depicts UPQC's evaluation with a zig-zag transformer for neutral current suppression. Zig-zag transformer neutral current (i_{zzn}) is used to be producing zero sequences currently in exact opposite phase to the neutral current (i_{ln}) and permitting compensated supply neutral current. Finally, it is shown that UPQC with IRZA-NLMS control algorithm is successful in mitigating supply current and load voltage distortion within the IEEE-519-2014 required range. Table 2 summarizes the usefulness of suggested IRZA-NLMS control algorithm in a 4-wire UPQC system for harmonic, voltage unbalance and sag. Table 2 explains recorded results of "phase *ab*" in uncompensated supply voltage (v_{sab}), mitigated source current (i_{sa}),

compensated load voltage (v_{lab}) and distorted load current (i_{la}) with a non-linear loading on 4 wire UPQC system. For sag and unbalance in the supply voltage, a minus of 10% voltage drop is generated. In the same way, around 10% of voltage harmonics are observed in the supply voltage. These steady-state performances are investigated for the above-mentioned conditions on the supply line. It can be seen that the v_{lab} and i_{sa} fall under the IEEE-519-2014 permissible limit.

VI. Conclusions

The proposed UPQC system performance effectively maintained the balanced sinusoidal load voltage, power factor correction, load balancing, harmonic elimination, and supply neutral current compensation has been explained. It is observed that the IRZA-NLMS algorithm-based UPQC successfully mitigates PQ issues and makes the load voltages and supply currents sinusoidal. The proposed IRZA-NLMS algorithm effectively reduces harmonics and provides fundamental components for the generation of reference signals. The IRZA-NLMS algorithm has reduced complexity, the smallest error of steady-state, the minimum dynamic oscillation, and the fastest convergence speed. The gains of PI-controller are optimized by utilizing SAMP-Rao algorithm seeks minimized terminal AC voltage and DC bus voltage fluctuation. The SAMP-Rao algorithm has fast-tracking performance, is simple to implement, requires basic arithmetic operations, and is without any specific parameters initialization. The effectiveness of the UPQC is significantly improved by employing proposed IRZA-NLMS algorithm and SAMP-Rao in terms of fundamental components extraction and optimizing PI gains respectively. So, the proposed 3-phase 4-wire UPQC can operate effectively under different numerous disruptions that occur concurrently with non-linear load and mitigate all PQ problems. The distortions present in supply voltage and load currents have been restricted to levels of IEEE standards.

Appendix A

A1. Parameter Used in Simulation of IRZA-NLMS Control Algorithm on UPQC System

Non ideal ac line voltage (v_{sabc}) 110 V, 50 Hz; Non-linear load: three single phase uncontrolled ac-dc converter having R=5 Ω, L=250 mH; dc link voltage (V_{dc}) =200 V; ac link terminal voltage (V_t) = 89 V; 4 kVA, 120/120 V series injection transformer; 7 kVA, 120/120 V zig-zag transformer; Source impedance (Z_s) R=0.060 Ω, L=2 mH; Interfacing inductance at shunt side (L_{sh}) = 2.5 mH; Series side Interfacing inductance (L_{se}) = 1 mH; LPF ripple filter: R_f=4 Ω, C_f=20 μF; IGBT converter switching frequency=10 kHz; Cut of frequency for filter=2*pi*10; IRZA-NLMS gains: γ=20, δ=0.01, ρ=5e^{-4} and ε=5.

A2. Parameter Used in Hardware Setup

Nonideal ac supply voltage: 110 V, 50 Hz; Nonlinear load: three 1-phase uncontrolled ac-dc converter with RL; dc bus voltage (V_{dc}) =200 V; dc-capacitor (C_{dc})= 3500 μF; ac bus voltage (V_t) =89 V; 4 kVA, 125/125 V series injection transformer; 1 kVA, 120/120 V zig-zag transformer; Interfacing inductance (L_{sh}) at shunt end = 4 mH; Series side interfacing inductance (L_{se}) = 4 mH; Cut off frequency for filter =2*pi*12.

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