

Dynamic Current Balancing for Paralleled SiC MOSFETs With Circuit Mismatches Considering Circulating Current in Drive Circuit

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Abstract—Parallel operation of silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) is necessary for high-power applications. However, the dynamic current sharing of paralleled devices is very sensitive to mis-matched circuit parasitic inductances due to their high switching speeds. Symmetric parasitic inductances are usually difficult to realize because of the limitation of circuit layout, especially when more than two devices are paralleled. In this paper, the effects of the circulating current in the drive circuit caused by the circuit mismatches, which result in dynamic current imbalance, are firstly analyzed in detail. The influences of related drive circuit parameters are presented, which reveal the mechanism of dynamic current sharing. Motivated by the analysis, a suppression method of the circulating current is proposed by inserting additional impedances in the drive circuit. Considering the coupling noises introduced by the additional impedances, the concept of blocking unit is proposed to guarantee the proper operation of the drive circuit. A simple circuit implementation and the operation principle are presented. Finally, the drive method is validated by both simulations and experiments. Experimental results show the peak current imbalance is reduced from 16.5% to 3.2% and the maximum switching loss imbalance is reduced by half.

Index Terms—Circulating current, circuit mismatches, dynamic current sharing, gate driver, paralleled SiC MOSFETs.

I. INTRODUCTION

WITH the superior intrinsic material properties of silicon carbide (SiC), SiC metal-oxide-semiconductor field-effect transistor (MOSFET), which can operate at higher voltage, higher switching frequency and higher temperature, is a good replacement for the silicon (Si) power device in applications like solar inverters, railway traction inverters and electric vehicles [1], [2]. Limited by the material performance and low

yield, the current ratings of single commercial SiC MOSFET chips are usually not large enough for high-power applications. Parallel operation of SiC MOSFETs is necessary to improve the capacity of power electronics systems [3], [4]. However, the current imbalance of paralleled SiC MOSFETs caused by mismatched device parameters and asymmetric circuit layout is still a problem to be solved [5]. Current imbalance will result in uneven junction temperatures and influence the reliability of the whole system. Therefore, it is necessary to investigate the mechanisms of current sharing and explore methods to balance the currents of paralleled devices.

To date, many research works on current sharing methods for paralleled devices have been carried out. The influences of device parameters on both static current sharing and dynamic current sharing are analyzed in [5]–[7]. The current imbalance caused by mismatched device parameters can be improved by advanced semiconductor process technology or device screening methods [8], [9]. The mismatched circuit parameters also play an important role in current sharing [5], [7], [10]–[14]. It is revealed that the power-source inductances are highly related with the dynamic current sharing of paralleled devices while other parts of parasitic inductances have minor effects.

In summary, the factors affecting current sharing can be categorized as device parameter tolerances and circuit parasitic mismatches. Therefore, the state-of-the-art current balancing methods are usually aimed at dealing with one or both of the factors. Among these methods, some active gate driver (AGD) methods and coupled inductor methods can mitigate the current imbalance caused by both types of factors, while circuit layout optimization methods usually focus on circuit parasitic mismatches.

The AGDs use the sensed current information to control the gate parameters of paralleled devices [15]–[19]. The advantage of the AGDs is the flexible control. However, complex analog/digital systems are required to adjust the drive signal delay, drive voltage or drive current, which increase the cost and lower the reliability. Besides, there has been no satisfactory solution of a compact and high-bandwidth current detection circuit, which is usually necessary to AGDs. The di/dt based analog feedback circuits in [20] and [21] are simple and effective. However, it requires a symmetric circuit layout.

Coupled inductors are also commonly used to improve current sharing due to their simple structure [22]–[26]. However,

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it is difficult to improve the power density since the inductors are bulky. In [24]–[26], the inductor sizes are smaller due to their much lower inductances. Nevertheless, lower inductances also mean these methods are more sensitive to the circuit mismatches. These passive methods are also hard to be extended for more paralleled devices.

Considering the drawbacks of AGDs and passive methods, device screening methods are simpler and widely used in industry to eliminate the influences of device tolerances. Therefore, some recent research works focus on the circuit mismatches and the optimization of circuit layout. Identical equivalent power-source inductances can be achieved by the adjustments of lengths of current paths or additional current paths [27], [28]. The circuit mismatches are compensated by the common source inductances in [29]. Such methods are straightforward but may increase the equivalent parasitic inductances and decrease the switching speed. They are not suitable for applications require ultra-low parasitics. Additional capacitive components can change the transient current paths of the paralleled devices. DC decoupling capacitors or silicon-based capacitors are adopted in [30]–[33] to reduce the circuit mismatch. These methods do not require complex circuit layout and can achieve good current balance. However, the footprints of ceramic capacitors are still too large for a power module, while the capacitances of silicon-based capacitors are limited.

As discussed above, the combination of device screening and symmetric layout design is a practical way to improve current sharing. However, the layout flexibility might be limited, which will affect other aspects of circuit performance. As mentioned in [33], the root cause of dynamic current imbalance with circuit mismatches is the circulating current in the gate drive circuit. Therefore, the current imbalance might be suppressed by special drive circuit design. However, the mechanism of the circulating current in the drive circuit with circuit mismatches has not been fully revealed by now. Different drive topologies were compared in [34] but the key factors and in-depth current sharing analysis are missed. Meanwhile, there have been seldom research works about the drive circuit design considering mismatched parasitics. Common-mode choke was inserted in the gate drive loop to limit the current imbalance in [35]. This is a simple method but the choke is bulky, which is hard to be integrated.

In this paper, the influence of the circulating current is comprehensively analyzed based on the equivalent circulating current loop. The suppression method of the circulating current is presented considering potential coupling noises in the drive circuit. A drive method is proposed to limit the circulating current and improve dynamic current sharing based on the concept of blocking units. The circuit implementation of the blocking unit is not sole can be very simple. Compared with layout optimization, the power circuit layout is more flexible with this method. Besides, the drive circuit composed of semiconductor components is suitable for further integration and extension to any number of paralleled devices.

The rest of this paper is organized as follows. In Section II,

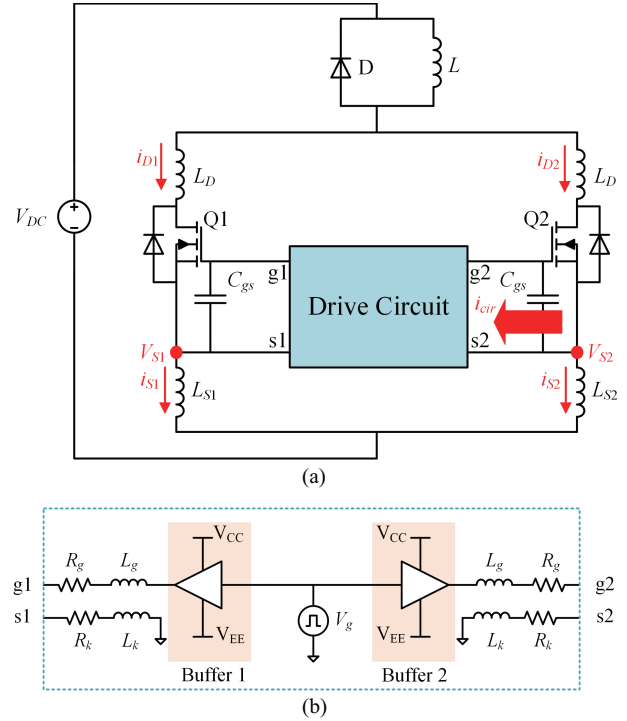


Fig. 1. Schematic of DPT circuit of two paralleled devices. (a) Power circuit. (b) Drive circuit.

the influence of the circulating current in the drive circuit and the related parameters are comprehensively analyzed considering mismatched power-source inductances. Section III introduces the circulating current suppression method considering the potential coupling noises. The hardware setup, simulations, and experiments are presented to validate the effectiveness of the proposed gate drive method in Section IV. Finally, a conclusion is summarized in Section V.

II. INFLUENCE OF CIRCULATING CURRENT IN DRIVE CIRCUIT

The parasitic inductances of paralleled SiC MOSFETs are usually not matched in multichip power modules or power converters due to the layout restrictions. The difference between the power-source inductances will cause significant dynamic current imbalance even with identical power devices [27]–[28]. This section focuses on how the circulating current caused by such circuit mismatches influences the dynamic current sharing of paralleled devices. The relationship between the circulating current and the gate drive circuit parameters will be discussed.

The schematic of a double pulse test (DPT) circuit of 2 paralleled SiC MOSFETs is shown in Fig. 1. The parameters in the circuit are listed in Table I. The detailed drive circuit is shown in Fig. 1(b). The drive currents are amplified by 2 buffers after the drive signal V_g . This drive circuit can enlarge the drive capability and guarantee the consistency of the driver loops. In order to simplify the analysis, L_{S1} and L_{S2} , the main causes of current imbalance, are considered to be different, while the other parameters of two devices are considered to be identical.

In Fig. 1, the voltage potentials of the source terminals of

TABLE I
PARAMETERS IN DPT CIRCUIT OF TWO PARALLELED DEVICES

Symbols	Parameters description
V_{DC}	DC bus voltage
D	Freewheeling diode
L	Load inductor
L_D	Drain inductance
V_g	Drive voltage
R_g	Gate resistance
L_g	Gate inductance
C_{gs}	Gate-source capacitance
L_k	Kelvin-source inductance
R_k	Kelvin-source resistance
L_{S1}, L_{S2}	Power-source inductance

Q1 and Q2 (V_{S1} and V_{S2}) are different because of the difference between L_{S1} and L_{S2} (L_{S2} is assumed to be higher in Fig. 1). As a consequence, a circulating current (i_{cir}) will flow through the gate drive circuit. The gate source voltages and the related dynamic current sharing are affected by i_{cir} . The MOSFET is modeled as a voltage controlled current source in the current rising/falling stage, which can be expressed as

$$i_D = g_{fs} (v_{gs} - V_{th}) \quad (1)$$

where g_{fs} is the transconductance, v_{gs} is the gate-source voltage, and V_{th} is the threshold voltage. g_{fs} is considered as a constant in this paper to simplify the analysis. In the following analysis, the drain currents of 2 paralleled MOSFETs are expressed in the form of

$$\begin{cases} i_{D1} = i_{D0} + \Delta i \\ i_{D2} = i_{D0} - \Delta i \end{cases} \quad (2)$$

Based on (1) and (2), the drain current variation Δi can be expressed as

$$\Delta i = g_{fs} (v_{gs1} - v_{gs2}) / 2 = g_{fs} \Delta v_{gs} / 2 \quad (3)$$

where Δv_{gs} is the gate-source voltage difference. According to Fig. 1, Δv_{gs} caused by the circulating current is highly related with the gate drive circuit. Therefore, the effects of the drive circuit parameters should be systematically analyzed.

The equivalent circuit of the drive circuit in Fig. 1(b) is shown in Fig. 2(a). The parasitics (R_c, L_c) of the connections to the power supply are also included. The capacitors C_p and C_N are decoupling capacitors for the buffers shown in Fig. 1(b). The turn-on and turn-off drive current paths are distinguished by red and blue lines.

Fig. 2(a) can be further simplified as Fig. 2(b), where only the turn-on drive current paths are considered. The power supply voltages are shorted because they do not contribute to the current difference. Decoupling capacitors are also shorted due to their very low impedances in the switching transients.

In Fig. 2(b), according to Kirchhoff's voltage law and current

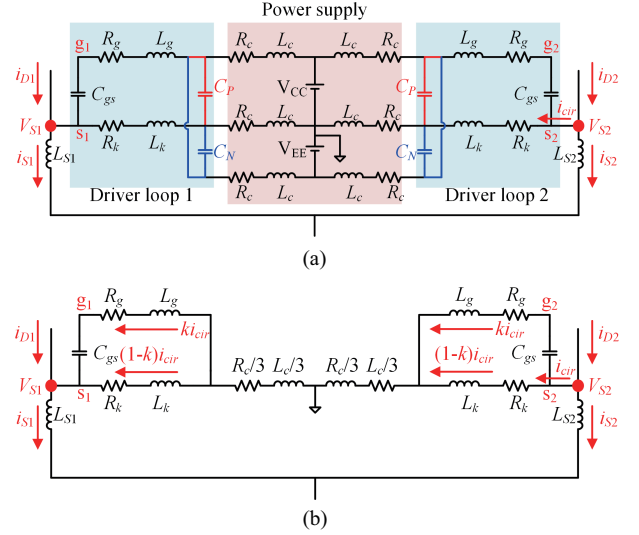


Fig. 2. Equivalent circuit of the drive circuit. (a) Complete circuit. (b) Simplified turn-on drive circuit.

law (KVL & KCL), the following relationship is presented:

$$i_{D1}(s)Z_{S1} + (Z_G + Z_c + Z_{S1} + Z_{S2})i_{cir}(s) = i_{D2}(s)Z_{S2} \quad (4)$$

where

$$\begin{cases} Z_{S1} = sL_{S1} \\ Z_{S2} = sL_{S2} \\ Z_G = 2(1/sC_{gs} + R_g + sL_g) // (R_k + sL_k) \\ Z_c = 2(R_c / 3 + sL_c / 3) \end{cases} \quad (5)$$

In Fig. 2(b), circulating current (ki_{cir}) charges/discharges the gate-source capacitance of Q1/Q2, which leads to Δv_{gs} . The factor k is a current sharing factor, which is defined as

$$k(s) = \frac{R_k + sL_k}{1/sC_{gs} + R_g + R_k + s(L_g + L_k)} \quad (6)$$

The difference between the gate-source voltages of two devices can be expressed as

$$\Delta v_{gs}(s) = \frac{2k(s)i_{cir}(s)}{sC_{gs}} \quad (7)$$

Combining (2)-(7), the following expression can be derived:

$$\frac{\Delta i}{i_{D0}}(s) = \frac{(Z_{S2} - Z_{S1})}{Z_{S1} + Z_{S2} + \frac{sC_{gs}}{k(s)g_{fs}}(Z_{S1} + Z_{S2} + Z_G + Z_c)} \quad (8)$$

(8) can reflect the degree of dynamic current imbalance caused by mismatched power-source inductances. For a constant $L_{S2} - L_{S1}$, the dynamic current imbalance can be mitigated

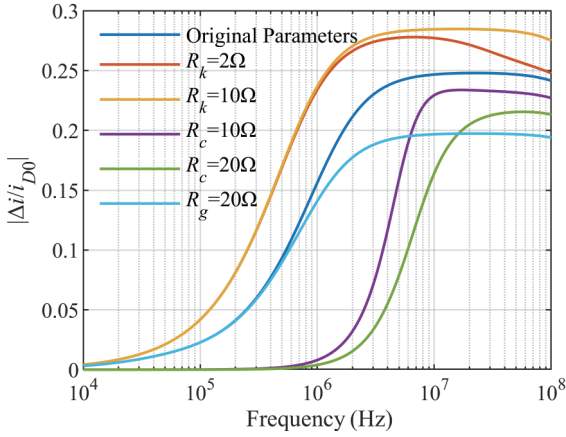


Fig. 3. Calculation of dynamic current imbalance with different gate drive circuit parameters.

by increasing the denominator of the left side of (8). The device-related parameters, including C_{gs} and g_{fs} , are fixed once the SiC MOSFETs is determined. The current imbalance can be reduced by increasing Z_{S1} and Z_{S2} simultaneous. However, larger parasitic inductances, which will cause severer parasitic oscillation and drain-source voltage spike, should be avoided.

(8) also indicates that the current sharing is highly related with the parameter configuration of the driver loops. Previous research works have tried to limit the circulating current by inserting additional R_k or R_c [34], [36]. However, the effects of these parameters on the dynamic current sharing performance have not been revealed. The influences can be evaluated by (8) based on the device parameters ($C_{gs}=3349$ pF, $g_{fs}=27$ S) of the SiC MOSFET C3M0032120K from Cree and a set of circuit parameters ($R_g=10$ Ω, $R_k=5$ mΩ, $L_g=10$ nH, $L_k=10$ nH, $L_{S1}=5$ nH, $L_{S2}=10$ nH, $R_c=5$ mΩ, $L_c=10$ nH). As is shown in Fig. 3, the amplitudes of (8) are calculated based on the original parameters and different R_k , R_c or R_g .

According to Fig. 3, the increase of R_g can improve the dynamic current sharing because it decreases the factor k and prevents the circulating current from charging the C_{gs} . However, the switching speed is highly related with R_g . It is also clear that increasing R_k is not effective for the current imbalance caused by the circulating current. The root cause of this phenomenon is that larger R_k can only decrease the circulating current through the kelvin source branch, which in turn increases the factor k , the circulating current through C_{gs} , and the related Δv_{gs} . Meanwhile, R_k is located in the driver loop, which will also affect the switching speed like R_g . In contrast, R_c is outside the driver loop and can mitigate the total circulating current, which prevents the voltage potential difference at the source terminals from charging C_{gs} . Therefore, it is shown in Fig. 3 that larger R_c can help improve the dynamic current sharing.

As discussed above, with the drive circuit configuration shown in Fig. 2, the circulating current in the drive circuit and the dynamic current imbalance can be decreased by inserting additional resistances in the connection paths of the power supply. However, whether the increase in the resistance will affect other performances of the drive circuit should be further analyzed.

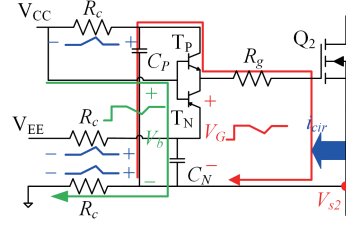


Fig. 4. Drive signal noise at the turn-on transient.

III. SUPPRESSION METHOD OF CIRCULATING CURRENT

The effects of circulating current in the drive circuit and related parameters have been comprehensively analyzed in Section II. It is possible that the circulating current can be suppressed by additional impedance in the drive circuit. In order to guarantee the proper operation of the drive circuit, the influences of the additional impedance on circuit performance will be analyzed in this section. Meanwhile, a circulating current suppression method is introduced to improve the dynamic current sharing performance based on the analysis.

A. Influences of Additional Impedance

Due to the buffer stages and their decoupling capacitors in the circuitry shown in Fig. 1(b), additional impedances R_c inserted in the power supply paths will not affect the rising/falling time of the switching transient. However, there are still problems for this circuit configuration.

The drive circuit in the turn-on transient is shown in Fig. 4. A totem-pole stage is usually used as the buffer. For simplicity, the drive circuit of Q1 is not shown, which is similar to that of Q2. The effect of additional resistances R_c is considered while other circuit parasitics are not shown for simplicity. As discussed in Section II, R_c should be large enough to suppress the circulating current, which means the source voltage difference ($V_{S1}-V_{S2}$) in the turn-on transient mainly drops across R_c , as shown in Fig. 4. The circulating current and its effects are highlighted in blue. The base voltage V_b of the totem-pole stage (i.e. input drive signal of the buffer stage) is affected by this voltage spike. In Fig. 4, the green loop is the KVL loop for the input voltage (V_b) of the totem-pole stage while the red loop represents the drive loop for the SiC MOSFET in the turn-on transient. The output voltage V_G of the buffer follows V_b , which means there is a coupling noise at the output caused by the additional R_c . Therefore, the gate-source voltages (v_{gs1} , v_{gs2}) of two paralleled devices are also affected by the source voltage difference. The circuit shown in Fig. 4 fails to suppress the current imbalance even with additional R_c . The circulating current is still suppressed by R_c but the proper operation of the drive circuit is affected. The totem stages are considered as switches fully turned on in Fig. 2, so the effect of the coupling noise caused by the additional resistances R_c is missed in the analysis of Section II.

B. Drive Circuit With Blocking Units

As discussed above, additional impedances in the drive

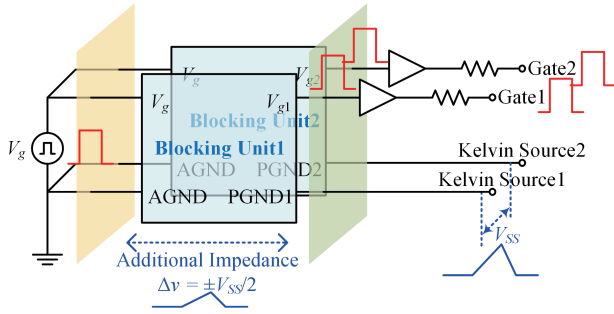


Fig. 5. Drive circuit with blocking units.

circuit can suppress the circulating current but it will distort the gate drive signal because of the coupling noise. In order to eliminate the influence of the noise, a gate drive architecture is proposed and shown in Fig. 5. Additional blocking units are inserted before the drive current buffers, which provide the additional impedances required to suppress the circulating current.

The key effect of the blocking unit is to simultaneously transmit the driver signal to the floating gate-source capacitance of each device and block the source-to-source voltage V_{SS} . The voltage V_g is the drive signal for the two blocking units. The outputs are the separate drive voltages (V_{g1} , V_{g2}) for two drive current buffers. In the circuit, PGND1 and PGND2 connected to the kelvin sources of paralleled devices are floating, whose potentials can be higher or lower than the reference ground AGND of gate driver input side. The blocking units will withstand the source voltage difference V_{SS} induced by mismatched power-source inductances and limit the circulating current through the gate network. As long as the delay of two blocking units is matched, the drive circuit can mitigate the dynamic current imbalance caused by mismatched source inductances.

C. Circuit Implementation

The function of blocking unit might be realized by various circuits, such as isolators or level shifters. However, there has been no commercially available IC for this application. To achieve a simple circuit structure with discrete transistors, the circuit implementation of the blocking unit is composed of complementary MOSFETs and additional resistors in this paper, as shown in Fig. 6. Compared with the drive circuit shown in Fig. 4, only two extra MOSFETs are required.

In Fig. 6, V_{CC} , V_{EE} and AGND represent the positive voltage, negative voltage, and ground of power supply, respectively. Each paralleled MOSFET Q_n (n means the n^{th} paralleled device) is configured with its own blocking unit. V_{CCn} and V_{EE_n} are the positive voltage and negative voltage powering the buffers, which are held by the capacitors C_{Pn} and C_{Nn} and provide the drive current for the SiC MOSFET. PGND $_n$ is connected to the kelvin source of the n^{th} device, which is also the reference ground of the buffers. The additional impedance in Fig. 5 is realized by blocking connection resistors R_c between the power supply and the buffers, which limit the circulating current that charges C_{gs} and results in current imbalance.

Similar to the circuit shown in Fig. 4, the amplitude of input

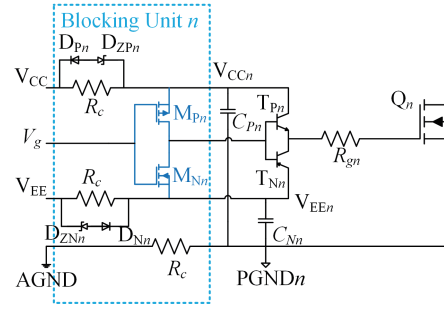


Fig. 6. Circuit implementation of blocking unit.

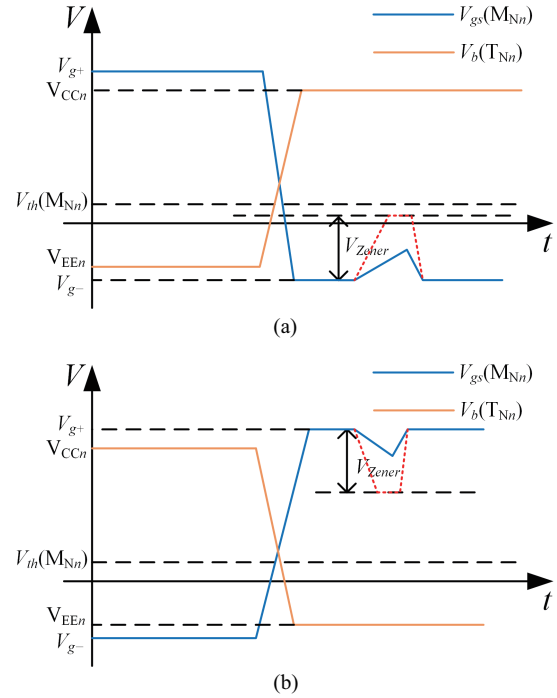


Fig. 7. Operation principle of blocking unit. (a) Turn-on transient state. (b) Turn-off transient state.

signal V_g will be affected by the voltage drops on R_c caused by V_{SS} in the switching transients as shown in Fig. 5. The complementary MOSFETs M_{Pn} and M_{Nn} is used to eliminate the influences of the voltage drop across R_c , and shape the input signal V_g to a non-distorted pulse signal for the cascaded buffer stage. Two branches composed of Zener diodes (D_{ZPn} , D_{ZNn}) and diodes (D_{Pn} , D_{Nn}) are paralleled to R_c in order to protect M_{Pn} and M_{Nn} from false turning on or turning off during the transient. The fast switching of the small-signal transistors can help avoid the delay difference.

The operation principle of the circuit shown in Fig. 6 during the turn-on/off transient is briefly illustrated by the waveforms shown in Fig. 7. In Fig. 7, the blue line is the gate-source voltage of M_{Nn} and orange line is the voltage between the base of T_{Nn} and PGND $_n$. When turning on the SiC MOSFET, M_{Nn} is turned off by $V_{gs}(M_{Nn})$ as shown in Fig. 7(a). There will be a spike of $V_{gs}(M_{Nn})$ after M_{Nn} is turned off, which is caused by the voltage drops on R_c . The polarity and amplitude of this spike is

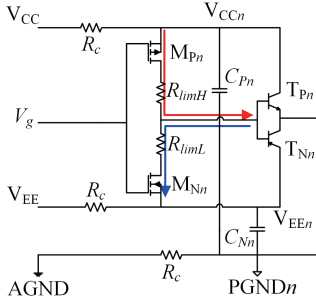


Fig. 8. Current limit resistances for the totem-pole MOSFETs.

dependent on the mismatched power-source inductances. Fig. 7 shows an example where the spike is positive. If the voltage difference between the power sources of the paralleled devices are too large, $V_{gs}(M_{Nn})$ might exceed the threshold voltage of M_{Nn} due to the spike, which will false turn on M_{Nn} . Therefore, D_{ZNn} is added to clamp the spike to V_{Zener} , which should be lower than $V_{th}(M_{Nn})$. This situation is shown in Fig. 7(a) by the red dot line. After turning off M_{Nn} , $V_b(T_{Nn})$ changes from V_{EE_n} to V_{CCn} , which turns on the SiC MOSFET. The high level of $V_b(T_{Nn})$ is smooth and not affected by the voltage drops on R_c . The process of turn-off transient is shown in Fig. 7(b), which is similar to the turn-on process and not repeated here.

With discrete transistors M_p and M_n , there might be a large overlapping range for the MOSFETs are turned on simultaneously. In order to avoid the potential overcurrent phenomenon and reduce the loss, resistors can be added in series with the MOSFETs to limit the current, as shown in Fig. 8, where the Zener diode branches are omitted. The resistors R_{limH} and R_{limL} can limit the current through the MOSFETs in the overlapping drive voltage range. The switching speed might be slightly reduced by the current limit resistances. To achieve a larger resistance and maintain a proper switching speed, as illustrated by the red and blue arrows in Fig. 8, R_{limH} and R_{limL} are added in the turn-on drive path and turn-off drive path, respectively. As a consequence, R_{limH} only affects the turn-on speed while R_{limL} only affects the turn-off speed.

The basic operation of the drive circuit with additional blocking unit is similar to that of the circuit shown in Fig. 4. With the current limit resistors, the power losses of the complementary is quite low, which hardly limit the switching frequency. The resistances will not influence the drive loss. The switching delay might be increased because the switching speeds of M_{Pn} and M_{Nn} are affected by the resistance of R_c . The relationship between the dynamic current imbalance and the resistance of R_c can be analyzed by the same method demonstrated in Section II, which can guide the determination of resistance R_c according to given circuit parameters.

IV. EXPERIMENTAL VALIDATION

In this section, a DPT hardware platform is built to verify the proposed circulating current suppression method. The dynamic current sharing performance of paralleled SiC MOSFETs are evaluated by both simulation and experiments.

TABLE II
EQUIVALENT VALUES OF PARASITIC INDUCTANCES CONSIDERING MUTUAL INDUCTANCES

Parameter	Equivalent Value
L_{LD1}	2.59 nH
$L_{LD2}+L_{LDD12}$	1.56 nH
$L_{LD3}+L_{LDD34}$	2.32 nH
L_{LD4}	2.48 nH
L_{LS1}	3.15 nH
$L_{LS2}+L_{LSS2}$	4.36 nH
$L_{LS3}+L_{LSS4}$	3.59 nH
L_{LS4}	2.46 nH

A. Layout of Power Circuit Loop

The equivalent circuit and the printed circuit board (PCB) layout of the DPT circuit are shown in Fig. 9. For simplicity, only power devices, the parasitics, and mutual couplings are shown in Fig. 9(a) and the high side devices are replaced by freewheeling diodes. Flux cancellation is adopted to minimize the parasitic inductance, which is realized by the opposite directions of device currents as marked in Fig. 9(b), like a bus-bar structure. Two decoupling capacitors (C_{dec1} and C_{dec2}) are placed at both sides of the paralleled devices, which are used to achieve a more symmetrical power circuit loop as demonstrated in Fig. 9(a) by loops in different colors.

The layout of PCB is modeled and simulated at 30 MHz by Ansys Q3D to extract the values of parasitic inductances. Considering the effects of mutual inductances, the equivalent key parasitic inductances in the commutation loops of low side devices are listed in Table II. It is found in Table II that the differences of equivalent parasitic inductances are still around 1~2 nH though efforts have been made to minimize the parasitic circuit mismatches, which means dynamic current imbalance will occur due to mismatched power-source inductances.

B. Parameter Design

The blocking resistance R_c in the blocking unit is important to the dynamic current sharing performance. In Section II, the relationship between dynamic current imbalance and various parameters has been demonstrated based on theoretical analysis. Though the coupling noise introduced by R_c is highlighted in Section III, the equivalent circuit of the drive circuit with blocking units is the same with that shown in Fig. 2, considering that the influence of the noise has already been eliminated. Therefore, the parameter R_c can be determined according to (8). Based on the extraction of parasitics, L_{S1} and L_{S2} (including the parasitics of package) are respectively set as 5.5 nH and 7.5 nH, respectively. The gate resistance R_g is set as 20 Ω while other related parameters are the same as those used in the calculation of Fig. 3. The comparison of dynamic current sharing performance with different R_c is shown in Fig. 10. Fig. 10 shows the relationship in the frequency domain rather than the time domain. However, it is reasonable to approximately evaluate the dynamic current sharing based on the bandwidth of the

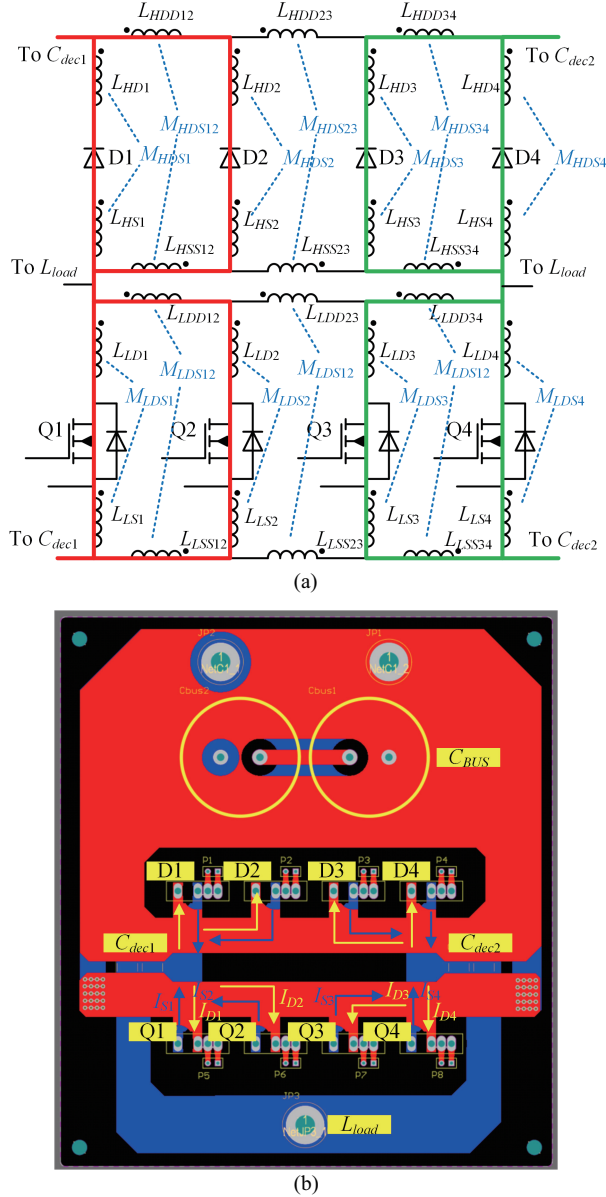


Fig. 9. DPT hardware configuration with four paralleled SiC MOSFETs. (a) Equivalent circuit. (b) PCB layout.

rising/falling edge of the device current. The high frequency bandwidth (BW) of the rising edge of the current can be expressed as

$$BW = \frac{0.35}{t_r} \quad (9)$$

where t_r is the rising time of the dynamic current of the SiC MOSFET.

Assuming that t_r is 40 ns, BW is about 8.75 MHz according to (9). It can be seen that the magnitude of current imbalance is below 5% within the BW of the dynamic current when R_c is chosen to be 24 Ω . Since the s-domain relationship cannot reflect the accurate relationship in the time domain, the design proce-

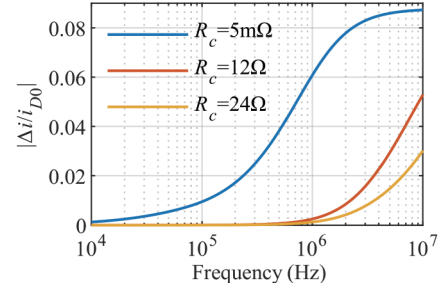


Fig. 10. Design of parameter R_c .

dure above just gives an approximate range for R_c . The effect of R_c can be further confirmed with the aid of circuit simulations.

C. Circuit Simulation

The power circuit for Pspice simulation is exactly the circuit shown in Fig. 9(a). Considering the symmetry of the layout, only two MOSFETs (Q1 & Q2) are considered in the simulations to avoid convergence problems. The parasitics are the same as the results extracted by Q3D. C_{dec1} is composed of two 100 nF decoupling capacitors. The ESL of a single decoupling capacitor is set as 2 nH. Two 220 μ F capacitors with 50 nH ESL are connected in series to serve as the dc bus capacitance. In the simulations, high side freewheeling diodes are replaced by SiC Schottky barrier diodes (SBDs). The low side switches are SiC MOSFETs. The spice models of SBD C3D30065D and SiC MOSFET C3M0032120K provided by Cree are adopted in the simulations. The dc bus voltage is 400 V.

The drive circuit includes two blocking units shown in Fig. 6. The gate resistance R_g is 20 Ω . C_p and C_N are both 10 μ F. The spice models of Si MOSFETs DMP610DL and DMN67D7L from Diodes are used as M_{p_n} and M_{n_n} as shown in Fig. 6. The spice model of the buffer composed of T_{p_n} and T_{n_n} is ZXG-D3003E6 from Diodes.

The simulation results of the proposed drive method ($R_c = 24 \Omega$) are compared with those of conventional drive circuit without blocking units and additional R_c , which are shown in Fig. 11. For the conventional drive circuit, the gate-source voltage is affected by the circulating current through the drive circuit, which results in dynamic current imbalance. The simulation results indicate that the influence of mismatched parasitics on the dynamic current sharing in the turn-off transient is less significant compared with that at turn-on transient. The device currents fall to zero fast before the gate-source voltages are affected by the circulating current. For the proposed drive method, the gate-source voltage difference is very small since the circulating current is limited by the additional impedances. Therefore, the dynamic current imbalance is also negligible.

The magnitudes total circulating current through the gate drive circuit in the switching transients in two different cases are also compared in the simulation, as shown in Fig. 12. It is clear that the circulating current can be effectively suppressed in both turn-on and turn-off transients by the proposed drive circuit. In the proposed drive circuit, it can be seen that the circulating current can also be quickly damped due to the exist-

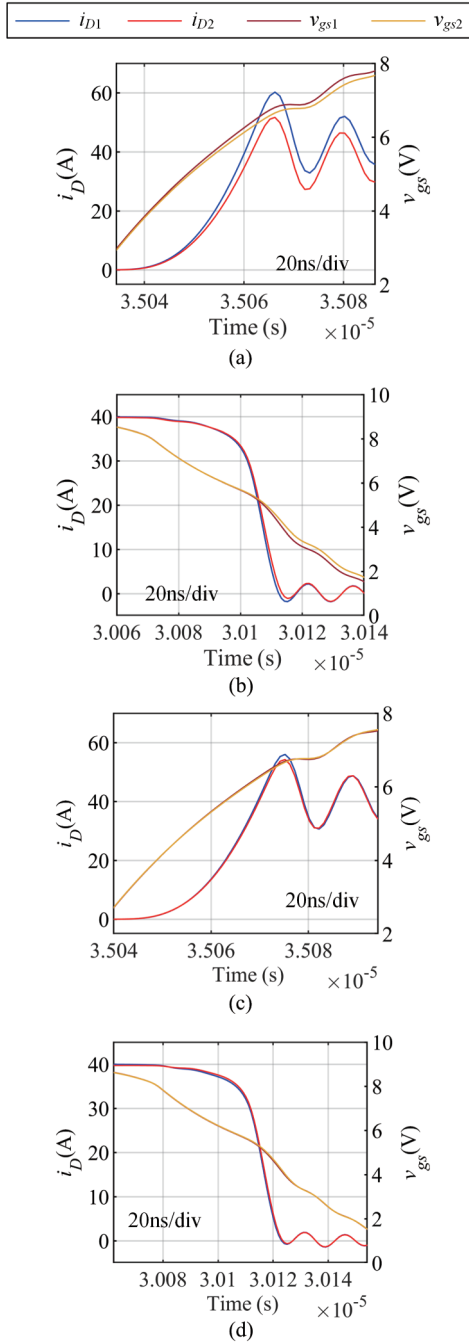


Fig. 11. Comparison of simulation results of conventional and proposed drive concept. (a) Turn-on transient with conventional driver circuit. (b) Turn-off transient with conventional drive circuit. (c) Turn-on transient with proposed gate drive circuit. (d) Turn-off transient with proposed gate drive circuit.

tence of additional R_c .

Corresponding to the theoretical waveforms shown in Fig. 7(a), the gate-source voltages of M_{N1} and M_{N2} and the base voltages of T_{N1} and T_{N2} in the turn-on transient are shown in Fig. 13. It is shown that the gate-source voltages of the MOSFETs in the blocking units are affected because of the voltage drop on R_c . However, the input voltages of the BJT buffers are not affected. Therefore, the drive voltage can be transmitted to the gates of SiC MOSFETs without coupling noises.

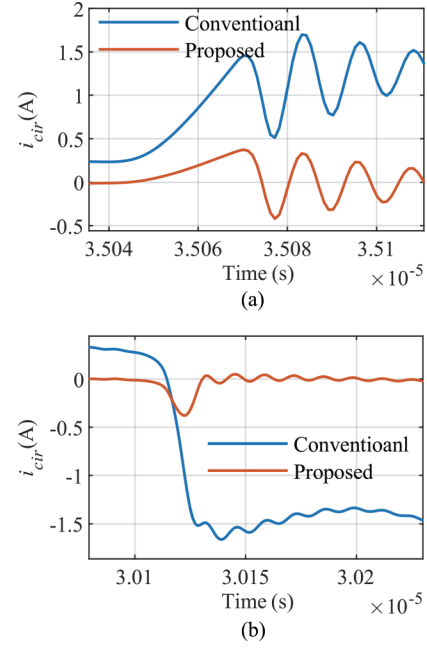


Fig. 12. Comparison of circulating current in two different cases. (a) Turn-on transient. (b) Turn-off transient.

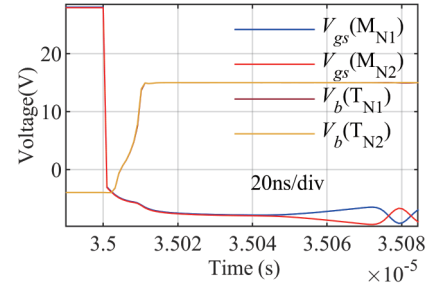


Fig. 13. The voltage waveforms of the transistors in the buffers.

D. Hardware Setup

The hardware setup is shown in Fig. 14. The part numbers of the key components are listed in Table III. The device currents are measured by Rogowski coils from PEM (30 MHz, 300 A). The load inductance is composed of two 50 μ H air-core inductors in series. The bus voltage is 400 V in the following experimental results. Fig. 14(b) shows the PCB of the drive circuit. The parameters are the same as those used in the circuit simulations.

The SiC MOSFETs with similar transfer characteristics are screened in advance. The transfer curves are measured by the curve tracer Keysight B1505A at 20 V drain-source voltage, which are shown in Fig. 15.

E. Experimental Results

According to Fig. 6, the gate driver is equivalent to a conventional drive circuit when $R_c = 0$. Therefore, current sharing performances are tested under 2 different conditions ($R_c = 0$, and $R_c = 24 \Omega$) to compare the effects of the gate drivers. The experimental results are shown in Fig. 16 and Fig. 17.

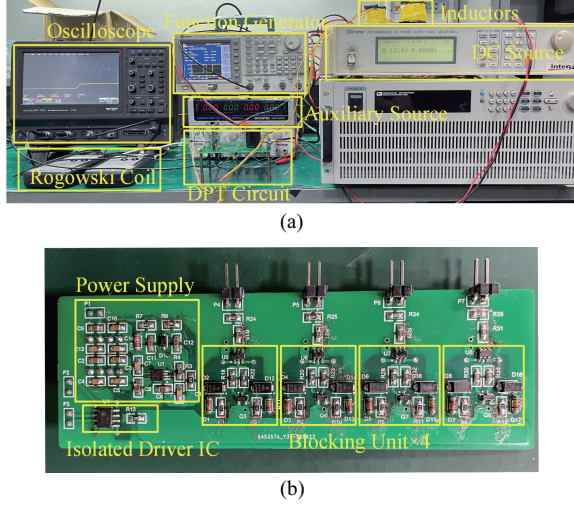


Fig. 14. Hardware setup. (a) DPT experimental platform. (b) PCB of driver circuit.

 TABLE III
 KEY COMPONENTS IN THE TEST CIRCUIT

Components	Parameters
Electrolytic capacitors	LGU2W221MELB (Nichicon) 450 V, 220 μ F
Decoupling capacitors	FV55X104K102EGG (PSA) 1 kV, 100 nF, X7R
Freewheeling SBDs	CSD10060A (Cree)
SiC MOSFETs	C3M0032120K (Cree)
P-channel MOSFETs	DMP610DL (Diodes)
N-channel MOSFETs	DMN67D7L (Diodes)
PNP and NPN buffers	ZXGD3003E6 (Diodes)

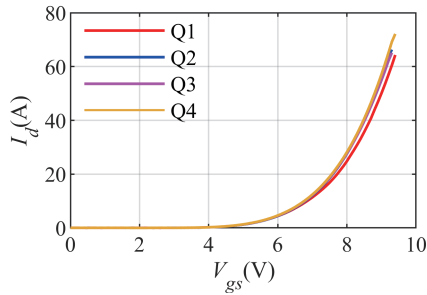


Fig. 15. Transfer curves of SiC MOSFETs.

As is shown in Fig. 9, the physical positions of Q1 and Q4 is symmetrical. Therefore, the current of Q1 is close to that of Q4 in tests. The relationship between Q2 and Q3 is also similar. According to the theoretical analysis and simulation, the power-source inductances of Q1 and Q4 are lower, which results in higher device currents in the turn-on transient when $R_c = 0$. When the resistance of R_c gets larger, the dynamic current imbalances in the turn-on transient become lower, which validates the effectiveness of the proposed gate drive method. The maximum turn-on current imbalances are summarized in Table IV. The maximum current imbalance is reduced from 6.7 A to 1.3 A

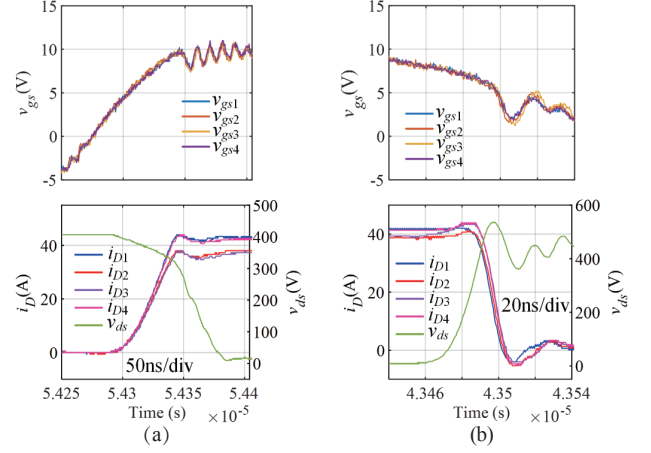
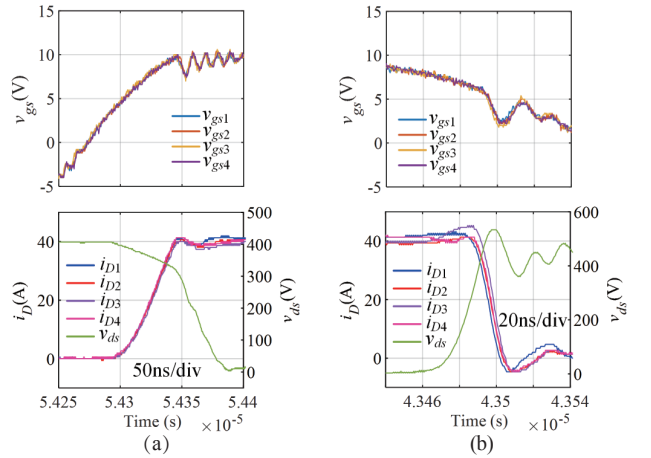

 Fig. 16. Experimental results ($R_c = 0$). (a) Turn-on waveforms. (b) Turn-off waveforms.

 Fig. 17. Experimental results ($R_c = 24 \Omega$). (a) Turn-on waveforms. (b) Turn-off waveforms.

 TABLE IV
 MAXIMUM TURN-ON CURRENT IMBALANCES

R_c	i_{D1max}	i_{D2max}	i_{D3max}	i_{D4max}	Δi_{max}	$\Delta i_{max}/i_{avg}$
0	44 A	38 A	37.3 A	43.3 A	6.7 A	16.5%
24Ω	41.3 A	40 A	40 A	41.3 A	1.3 A	3.2%

when R_c is increased to 24Ω . The ratio of maximum current imbalance to average device current is reduced from 16.5% to only 3.2%. In Fig. 16 and Fig. 17, the waveforms of gate-source voltages are nearly the same, which seems to be unreasonable. However, considering g_{fs} of the SiC MOSFET is 27 S, the maximum dynamic current imbalance can reach 7 A when Δv_{gs} is around only 250 mV, which is too low to be observed in the experimental waveforms. The initial current before the turn-off transient is dependent on static current sharing, which might also influence the dynamic current sharing. Meanwhile, the current slew rate is relatively larger in the turn-off transient. Therefore, current balancing effect during the turn-off transient is less obvious. The total switching losses of the paralleled devices are calculated and listed in Table V. The ratio of max-

TABLE V
TOTAL SWITCHING LOSSES OF PARALLELED DEVICES

R_c	E_{S1}	E_{S2}	E_{S3}	E_{S4}	$\Delta E_{Smax}/E_{Savg}$
0	908 μ J	850 μ J	874 μ J	949 μ J	11.1%
24 Ω	822 μ J	838 μ J	867 μ J	860 μ J	5.3%

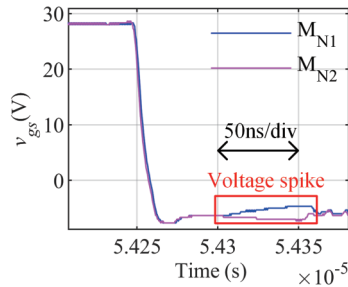


Fig. 18. Gate-source voltages of M_{N1} and M_{N2} .

imum switching loss imbalance to the average switching loss is reduced from 11.1% to 5.3% when R_c increases from 0 to 24 Ω . Generally, the experimental results are consistent with the simulation results.

The gate-source voltages of M_{N1} and M_{N2} in the blocking units are shown in Fig. 18. The voltage spikes are similar to the simulation waveforms shown in Fig. 13. Since efforts are taken to minimized the power-source inductances mismatch, the magnitudes of voltage spikes are very low, which are only around 1 V and far below the threshold voltage of M_{N1} . Therefore, there is enough margin for the proposed gate driver to operate with a larger power-source inductance mismatch or a higher current slew rate.

V. CONCLUSION

This paper presents a gate drive method to suppress the circulating current in the drive circuit of paralleled SiC MOSFETs with circuit parasitic mismatches, which can improve the dynamic current sharing. The influence of the circulating current on the dynamic current sharing, which has not been fully analyzed by previous works, is elaborated based on a theoretical analysis. The analysis reveals the effects of related circuit parameters and potential circulating suppression method. To limit the circulating current, additional impedances are required in the circulating current loop, which will introduce coupling noises and interfere the proper operation of the drive circuit. The concept of blocking unit is introduced to eliminate the influences of coupling noises. The circuit implementation of the blocking unit is flexible and can be realized by a simple circuit using several transistors. Therefore, it is easy to be integrated. The method also features with good extensibility, which is applicable to any number of paralleled devices.

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