

High-Resolution Digital PWM Optimization Method for Critical Path Delay in General FPGA

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Abstract—This paper proposes a high-resolution digital pulse width modulator (DPWM) signal optimization method for the critical path delay based on a field programmable gate array (FPGA), which mainly aims to improve the output regulation accuracy and linearity of the DPWM. This method realizes high-resolution and high-linearity DPWM output by constructing the logical symmetric multiplexer and the synchronous 2-to-1 selector for the critical path, and a simple placement constraint is used to reduce the critical path delay deviation. The high-resolution DPWM signal has the advantages of excellent linearity, easy expansion, and strong versatility, thus especially suitable for power electronic switching converters with high frequency, high accuracy, and high real-time control. The simulation and experimental results show that the DPWM with different FPGA achieves a resolution of 312.5 ps and high linearity, where R^2 is up to 0.99999. Finally, the proposed method is verified in a 48 V to 1 V DC/DC converter with a switching frequency of 1 MHz.

Index Terms—DPWM, FPGA, high-linearity, high-resolution.

I. INTRODUCTION

SWITCHING converters have been used more and more widely due to their advantages of flexible control, small size, and high efficiency. The volume and weight of the switching converter can be reduced with the increase of the switching frequency. With the rapid development of soft switching and semiconductor technology, switching converters can still achieve high-efficiency operation at switching frequencies up to MHz. In addition, the dynamic characteristics of switching converters are significantly improved at higher switching frequencies. Digital control technology has been widely used in high-frequency switching converters due to its reliability, strong scalability, and flexible control. For example, the control loop does not need complex analog components for feedback control. It is all completed

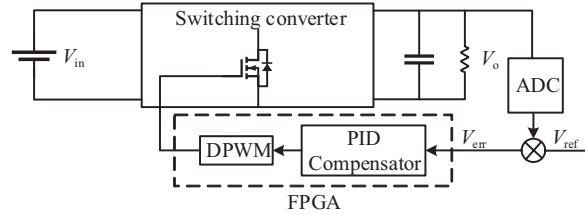


Fig. 1. Digitally controlled switching converter.

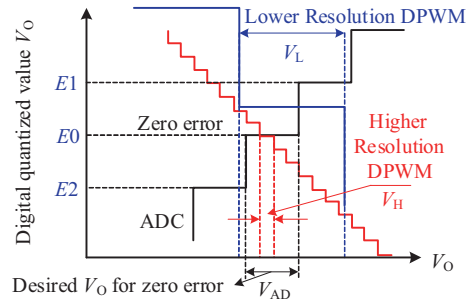


Fig. 2. Solution of limit cycle oscillation.

by a highly integrated microprocessor with a simple structure and high reliability. The controller can easily extend complex nonlinear control algorithms to improve the steady-state and dynamic performance of the converter. By modifying the software code of the controller and reprogramming, the control method update of the converter can be completed without modifying the hardware. The control system of the digital switching converter mainly consists of an analog-to-digital converter (ADC), a digital compensator, and a digital pulse width modulator (DPWM), as shown in Fig. 1. The higher resolution of ADC and DPWM, the higher control accuracy of the converter output voltage can be obtained. At the same time, the resolution of the DPWM signal needs to be higher than that of the ADC to reduce the output voltage error and avoid limit cycle oscillation [1]–[3]. As described in Fig. 2, the desired output voltage V_o is within the range of V_{AD} , and the value after ADC quantization is $E0$. When the DPWM resolution is low, the quantized value of the output voltage V_L is $E1$ or $E2$, which cannot reach $E0$. At this time, the control loop will continuously perform feedback adjustment, and the output voltage cannot be stabilized. When the DPWM resolution is high, the quantized value of the output voltage V_H can reach $E0$. At this time, the control loop realizes zero error, and the

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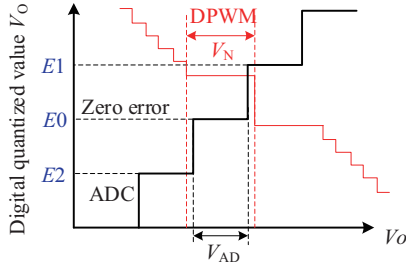


Fig. 3. Nonlinear effects of DPWM.

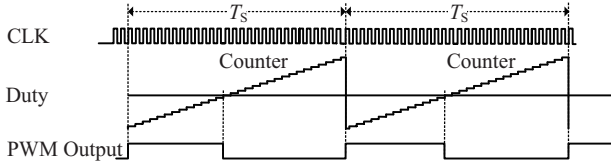


Fig. 4. The DPWM based on counter comparison method.

output voltage is stable.

On the other hand, what affects the output accuracy and stability of DPWM is its linearity. As shown in Fig. 3, when the resolution of DPWM has high non-linearity, its resolution deviation exceeds the resolution of ADC, the quantized value of the output voltage V_N cannot reach $E0$, which will also cause the decrease in output voltage accuracy and limit cycle oscillation.

Therefore, it is essential to realize high-resolution and high-linearity DPWM to improve the performance of high-frequency switching converters.

Digital controllers for switching converters are usually implemented with specific control chips. Current solutions for implementing high-precision DPWM are based on application-specific integrated circuits (ASICs) or provided as peripherals in microcontrollers, such as Texas Instrument TMS320F28035. However, ASICs have additional design costs, and microcontrollers have limited functionality. In addition, future iterations of technology updates require more significant costs. On the other hand, by constructing a high-resolution DPWM module and instantiating it in a field programmable gate array (FPGA), high-resolution DPWM output can be realized. FPGA has the feature of configurable programming. When it is necessary to improve the existing design or add new functions, it only needs to redesign the code and load it into the FPGA to realize the required functions without updating and iterating the hardware. FPGA has the characteristics of high flexibility and strong scalability, which makes it more and more widely used in switching converters.

The traditional way of generating DPWM signals based on FPGA is the counter comparison method, as shown in Fig. 4. It has the advantages of simple structure, less resource utilization, and high linearity. However, its minimum pulse time resolution is limited by the maximum clock frequency of the FPGA, given by (1), T_{step} is minimum pulse time resolution, and f_{clk} is the clock frequency for the counter.

$$T_{step} = \frac{1}{f_{clk}} \quad (1)$$

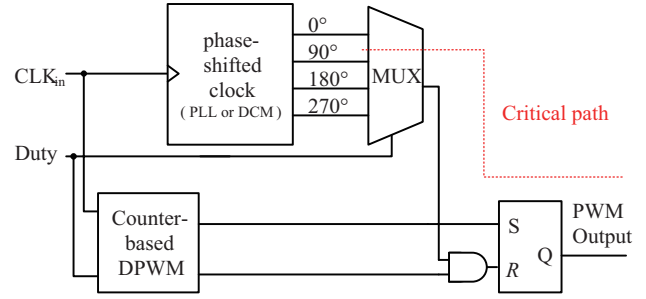


Fig. 5. The DPWM based on phase-shifted clock.

With the development of FPGA technology, the clock frequency that FPGA can support is getting higher and higher, reaching GHz. Even if the clock frequency reaches GHz, its minimum pulse time resolution only reaches the ns level, which does not significantly improve the resolution. Moreover, as the clock frequency increases, the cost of FPGA increases dramatically, which is unfavorable for the application of switching converters.

In recent years, many papers have proposed different methods based on FPGA to obtain smaller pulse time resolution. Table I summarizes the characteristics of these methods. These methods can be mainly divided into three types.

1) Based on phase-shifted clock: The first type utilizes the phase-locked loop (PLL) or digital clock management (DCM) unit of FPGA to generate phase-shifted clocks to construct delay lines for high-resolution DPWM signals, As shown in Fig. 5. The resolution of DPWM based on phase-shifted clock depends on the clock frequency and the number of clocks. [4] achieves 12.5 ns resolution with PLL. It uses eight 10 MHz phase-shifted clocks to construct eight phase-shifted carrier counters, which consumes many resources. The critical path contains two multiplexers, and there is no compensation for the delay deviation of the critical path. The delay deviation of DPWM is significant, and the linearity is low. Moreover, the clock signal's double-edge triggering capability has yet to fully develop. [5] and [6] use four 128 MHz phase-shifted clocks to achieve higher resolution, which reaches 2 ns. The critical path was not compensated, and its linearity was 0.994 with a resolution deviation of 450 ps in [6]. To improve the linearity of DPWM, [5] uses manual placement and routing to compensate for the delay deviation of the critical path, and the resolution deviation is reduced to 350 ps. In order to achieve a higher resolution, [3] uses three cascaded DCMs, and its resolution reaches 156 ps at a clock of 100 MHz. However, multi-stage multiplexers are on the critical path of the cascaded structure, which significantly reduces the DPWM linearity. Moreover, there is no compensation for the critical path. [7] proposes a DPWM structure with a time step of 19.5 ps based on the DCM of Xilinx FPGAs. The main disadvantage of the DPWM architecture is that the phase shift time of the clock must be dynamically updated when the duty cycle changes. Increasing update speed requires multiple phase-shifted clocks, and the presence of multiplexers in the critical path will reduce linearity.

2) Based on delay line: As shown in Fig. 6, the second approach uses the logic element or IDELAYE to obtain a delay

TABLE I
PERFORMANCE COMPARISON OF DIFFERENT DPWM ARCHITECTURES

| Ref | Year | Architecture | Clock Frequency | Compensation for Critical Path | Time resolution | Linearity R ² | Resolution Deviation | Main Characteristics |
|------|------|---------------------------------|-----------------|--------------------------------|-----------------|--------------------------|----------------------|---|
| [6] | 2008 | DLL-based DPWM | 128 MHz | No | 2 ns | 0.994 | 450 ps | Four clocks required. A multiplexer on the critical path. No compensation for the critical path. |
| [5] | 2009 | DPWM with DCM | 128 MHz | Yes | 2 ns | NA | 350 ps | Four clocks required. A multiplexer on the critical path. Manual place & route for the critical path. |
| [3] | 2009 | Cascaded DCM-based DPWM | 100 MHz | No | 156 ps | NA | NA | Using cascaded DCM to construct phase-shifted clock. There are multiplexers on the critical path. The more DCMs are used, the greater linearity deviation. No compensation for the critical path. |
| [7] | 2010 | DPWM with PLL | 200 MHz | No | 19.5 ps | NA | NA | Needs to dynamically update the phase shift angle of the clock. Increasing DPWM update speed requires multiple clocks. No compensation for the critical path. |
| [8] | 2010 | Hybrid DPWM with delay line | 50 MHz | Yes | < 100 ps | NA | NA | Using the adder carry to achieve fine delay adjustment. Complex manual layout required. Poor versatility. |
| [9] | 2013 | Carry chain-based DPWM | 200 MHz | Yes | < 100 ps | 0.9994-0.9999 | 20 ps | Using the carry chain to achieve fine delay adjustment. Additional constraints need to be added to reduce the deviation of the delay line. |
| [10] | 2015 | Carry chain-based DPWM | 46.34 MHz | No | 80 ps | NA | NA | Add registers at the front end of the carry chain and use FFOut to replace SR latch. The key path is the carry chain structure, and the linearity deviation is large. |
| [4] | 2017 | DPWM with PLL | 10 MHz | No | 12.5 ns | NA | NA | Eight clocks and eight counters required. The multiplexer on the critical path. No compensation for the critical path. |
| [11] | 2018 | PLL and carry chain based | 75 MHz | Yes | 53 ps | 0.9949 | NA | Use phase-shift clock and adder to delay carry to achieve high-precision delay. Manual place & route for the critical path. |
| [12] | 2018 | Controllable delay circuit | 12.8 MHz | No | 69.2 ns | NA | NA | Construct the integrator and the DA converter hardware circuit to achieve high-resolution DPWM output. The accuracy depends on the DA converter. DPWM has low precision and low flexibility. |
| [13] | 2018 | DCM-based and delay-line | 200 MHz | No | 625/500 ps | NA | NA | The RS latch utilized is replaced by the OR gate which possesses good stability as well as simplicity. No compensation for the critical path. |
| [14] | 2019 | Hybrid DPWM with IDELAYE | 400 MHz | No | 39 ps | NA | 16.5 ps | FPGA with IDELAYE2 function realizes fine delay line. The multiplexer on the critical path. No compensation for the critical path. |
| [15] | 2019 | Digitally-controlled delay-line | 10-20 MHz | No | 50 ps | NA | NA | Use the delay unit to realize the fine delay line. The multiplexer on the critical path. No compensation for the critical path. |
| [16] | 2020 | DETFE and carry chain-based | 122 MHz | Yes | 32 ps | 0.99 | 130 ps | Use adder carry and phase-shift clock for fine delay line. The compensation is realized by hardware logic circuits. Linearity deviation is still large after compensation. |
| [17] | 2020 | PLL & delay line | 188 MHz | Yes | 41.3 ps | 0.9994 | 130 ps | Synchronous phase-shifted clock circuit. Use DFF instead of SR latch. |
| [18] | 2020 | IDELAYE-based | 400 MHz | No | 80 ps | NA | 52 ps | FPGA with IDELAYE2 function realizes fine delay line. No any placement and routing required. |
| [19] | 2021 | DLL and delay-adjustable | 20-25 MHz | Yes | 1.25 ns | NA | 500 ps | Use delay chains to achieve fine adjustment, insert adjustable delay units in the critical path. Compensate for the delay deviation of the critical path, and improve linearity. |
| [20] | 2021 | IDELAYE-based | 400 MHz | No | 76.9 ps | NA | NA | FPGA with IDELAYE2 function realizes fine delay line. No any placement and routing required. |
| [21] | 2021 | DDS-Based DPWM | 400 MHz | No | 4 ns | NA | NA | Direct digital Synthesis-based DPWM architecture to achieve a high resolution. The implementation method is complex and has low flexibility. |
| [22] | 2022 | Digitally-controlled delay-line | 17 MHz | No | 41 ps | NA | NA | Use the delay unit to realize the fine delay line. The multiplexer on the critical path. No compensation for the critical path. |
| [23] | 2023 | Delay-Line Based | NA | No | 200-220 ps | NA | NA | High-resolution variable frequency variable duty-cycle. Use the delay unit to realize the f fine delay line. The implementation method is complex and has low flexibility. |

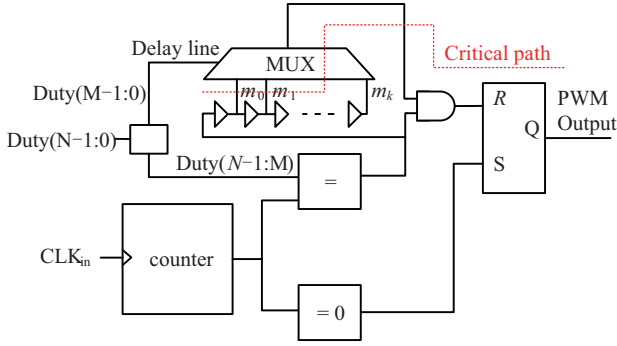


Fig. 6. The DPWM based on the delay line.

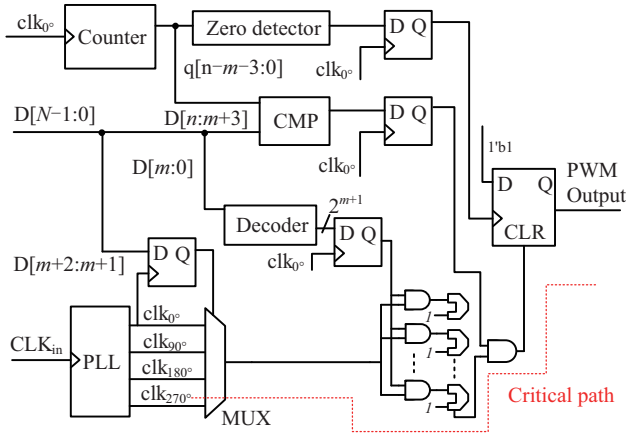


Fig. 7. The DPWM based on the hybrid structure.

line. This method can also generate high-resolution DPWM signals, and it does not use the internal PLL or DCM in FPGA and is not limited by the clock frequency. [14] uses two IDELAYE2 blocks to achieve a resolution of 19.5 ps. [20] implements complementary DPWM signals using four IDELAYE blocks, the time resolution for the Artix-7 is 79.6 ps, and the Kintex-UltraScale 7 is 4.72 ps. IDELAYE block is an IP officially provided by Xilinx that can be used to delay specific signals, so the method of using the IDELAYE block to realize high-precision DPWM can only be applied to FPGAs of the Xilinx series. [8] and [9] use the adder carry method to achieve fine delay adjustment with a resolution of less than 100 ps. However, this method requires additional layout and routing constraints for the fine delay unit, which is complex to implement and needs better versatility. [10], [15], [19], [22] and [23] adopt similar structures, and cascaded logic gates realize their fine delay elements. The inconsistency of the delay line and the presence of multiplexers on critical paths will lead to poor linearity.

3) Based on phase-shifted clock and delay line: In addition to these two main methods, high-resolution DPWM is also achieved by using the hybrid structure method, which has some of the advantages of the above two methods and improves the overall performance, as shown in Fig. 7.

In order to improve the critical path delay deviation, [16] uses hardware combinational logic to achieve duty cycle accuracy compensation, and [11] implements critical path optimization

through manual layout and routing. [17] proposes a synchronous phase-shifted circuit to optimize the critical path of the phase-shifted clock. Moreover, its implementation is complex.

Previous studies found that the phase-shifted clock-based method has good versatility. However, there is a common problem: the presence of multiplexers on the critical path, resulting in large delay deviations and reducing the linearity of DPWM. The method based on the delay line structure usually requires a complex manual layout and routing constraints on the delay path of the delay line or uses a specific type of FPGA to achieve fine delay. The device speed grade significantly affects the resolution, and the versatility is low. Although the hybrid architecture can improve the accuracy of DPWM, it also needs to optimize the delay of the critical path, and the implementation is complicated.

When the switching frequency of DPWM is up to MHz or higher, the time resolution will reach the picosecond level. Moreover, the delay time deviation of the critical path caused by the logic unit and interconnection will be greater than the time resolution of DPWM, which will cause serious non-linearity of DPWM. The inconsistency of DPWM output pulse width changes will lead to limit cycle oscillation and affect the regulation performance of the converter.

Considering the application of a high-frequency power electronic converter, the modulation of DPWM needs to have good universality, low complexity, high output accuracy, and high linearity. To actualize the above performances, the paper presents a simplified structure with an improved critical path optimization, which has the advantages of high linearity, easy implementation, less logical resource occupation, and simplicity of transplantation. The main contribution of the method proposed in this paper is to construct a simplified clock synchronization multiplexer and phase-shifted DPWM signal synchronization selector, which improves the delay deviation of the traditional multiplexer in the critical path.

The structure of this paper is as follows: Section II describes the architecture and application of the proposed implementation method. Section III illustrates the implementation of linearity optimization and provides a comparative analysis with traditional multiplexer method. Section IV evaluates and verifies the performance of the proposed method through simulation and experiment. Finally, Section V concludes the paper.

II. PROPOSED DPWM ARCHITECTURE AND APPLICATION

Fig. 8 shows the control architecture of the proposed DPWM signal modulation method. It consists of a decoder, a phase-shifted clock whose phase is delayed 180° $D[m-1:0]/2^m$ by the internal PLL of the FPGA, a reference PWM signal generating unit, and a phase-shifted PWM unit. $D[n-1:0]$ is the input duty cycle signal. $D[n-1:m+1]$ is used to generate a reference PWM signal, which is denoted as PWM_{Ref} . $D[m]$ is a flag-selected data bit that enables the corresponding phase-shifted PWM signal. $D[m-1:0]$ is used to select the phase-shifted clock, denoted as CLK_ϕ . CLK_{in} is the input clock signal of FPGA for PLL. PWM_{Output} is the output signal.

As Fig. 8 shows, the PLL generates clocks of the same fre-

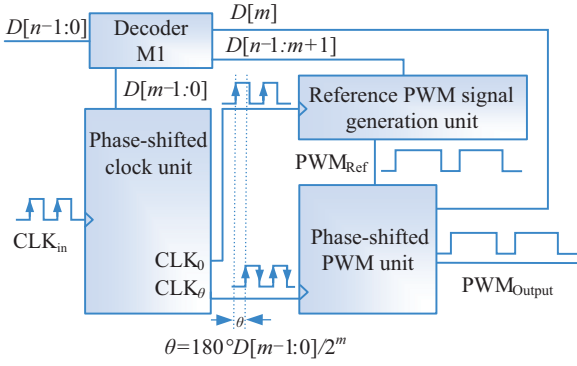


Fig. 8. Architecture of the proposed DPWM signal modulation method.

TABLE II
FUNCTION OF $D[m]$

| $D[m]$ | PWM_p | PWM_n | Phase-shifted angle under CLK_θ |
|--------|-------------|-------------|--|
| 0 | PWM_{Ref} | 0 | θ |
| 1 | 0 | PWM_{Ref} | $\theta+180^\circ$ |

quency and different phases. The PWM_{Ref} is generated with the clock of a 0° phase-shifting angle. The corresponding phase-shifted clock CLK_θ is selected according to the signal $D[m-1:0]$, and the phase-shifted clock CLK_θ shifts the phase of PWM_{Ref} by θ . The high-resolution PWM signal PWM_{Output} is constructed in the phase-shifted PWM unit.

In this section, the implementation of the proposed method will be introduced in detail.

A. Decoder Operation

The function of the decoder M1 is to turn input $D[n-1:0]$ into three parts, which are the most significant bits $D[n-1:m+1]$, the intermediate significant bit $D[m]$, the least significant bits $D[m-1:0]$. $D[n-1:m+1]$ is the modulated signal used to generate PWM_{Ref} under the rising edge of CLK_0 . $D[m]$ is the control signal used to select the reference PWM_{Ref} as PWM_p or PWM_n and then shift the phase of PWM_{Ref} through CLK_θ , as Table II shows. $D[m-1:0]$ is divided into two parts by decoder M2: the Clkselect and Ena. The Clkselect is used to select the clock from PLL, and the Ena enables the corresponding outclk clock signal, according to Table III.

B. Phase-Shifted Clock Configuration and Selection

In the phase-shifted clock unit, the clock signal with the high-resolution phase-shifting angle is generated, which is used to perform phase-shifting processing of the PWM_{Ref} .

1) PLL Configuration: There are configurable hardware PLL modules in FPGA chips. Different FPGAs can support different numbers of PLL. Generally, the number of supported PLL is 2 or 4 in FPGA, and each PLL can generate 5 clocks with different frequencies and phases. It can be configured according to actual needs.

The number of PLL selected is N_p and the number of clocks that each PLL can generate is N_c in this paper. To reduce the

TABLE III
FUNCTION OF $D[m-1:0]$

| $D[m-1:0]$ | Clkselect | Ena | CLK_θ | Phase-shifted delay |
|------------|-----------|----------|-------------------------------------|---------------------------|
| 00...000 | 10 | 00...001 | CLK_{0° | $0 \cdot T_p$ |
| 00...001 | 11 | 00...001 | $CLK_{180^\circ/2^m}$ | $1 \cdot T_p$ |
| 00...010 | 10 | 00...010 | $CLK_{180^\circ \cdot 2/2^m}$ | $2 \cdot T_p$ |
| 00...011 | 11 | 00...010 | $CLK_{180^\circ \cdot 3/2^m}$ | $3 \cdot T_p$ |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ |
| 11...100 | 10 | 01...000 | $CLK_{180^\circ \cdot (2^m-4)/2^m}$ | $(2^m-4) \cdot T_p / 2^m$ |
| 11...101 | 11 | 01...000 | $CLK_{180^\circ \cdot (2^m-3)/2^m}$ | $(2^m-3) \cdot T_p / 2^m$ |
| 11...110 | 10 | 10...000 | $CLK_{180^\circ \cdot (2^m-2)/2^m}$ | $(2^m-2) \cdot T_p / 2^m$ |
| 11...111 | 11 | 10...000 | $CLK_{180^\circ \cdot (2^m-1)/2^m}$ | $(2^m-1) \cdot T_p / 2^m$ |

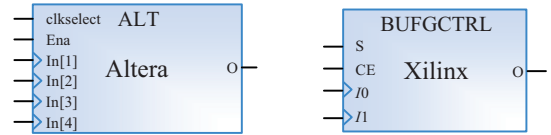


Fig. 9. The dedicated clock control blocks in Altera and Xilinx FPGA.

computational complexity and optimize the resource utilization of FPGA, the number of phase-shifting clocks N_p and N_c is selected as a multiple of 2, and the total number of clocks that can be generated is 2^m :

$$2^m = N_c \times N_p \quad (2)$$

The phase offset of adjacent phase-shift clocks is θ_c :

$$\theta_c = 180^\circ / 2^m \quad (3)$$

The phase delay of adjacent phase-shift clocks is T_p :

$$T_p = T_c / 2^{m+1} \quad (4)$$

The T_c is the period of the clock from PLL.

2) Clock Selection: To improve the nonlinear effect caused by excessive delay deviation of conventional MUX, this paper proposes a logically symmetric MUX whose basic unit contains dedicated clock control blocks and logical OR gates.

The dedicated clock control block is a unique clock selector with excellent symmetry. It can dynamically select the input clock signal and has the function of enabling the output signal. Most FPGAs are configured with this feature. The dedicated clock control blocks for Altera and Xilinx series FPGAs are shown in Fig. 9.

The altclkctrl (ALT) is a clock control block in Altera FPGA with a clock control function. With the Quartus II MegaWizard Plug-In Manager, the clock control block can be easily configured in supported devices. It is available for Arria 10, Arria II GX, Arria II GZ, Arria V, Arria V GZ, Cyclone III, Cyclone III LS, Cyclone IV E, Cyclone IV GX, Cyclone V, Cyclone 10 LP, Stratix IV, Stratix V, and MAX 10 device series.

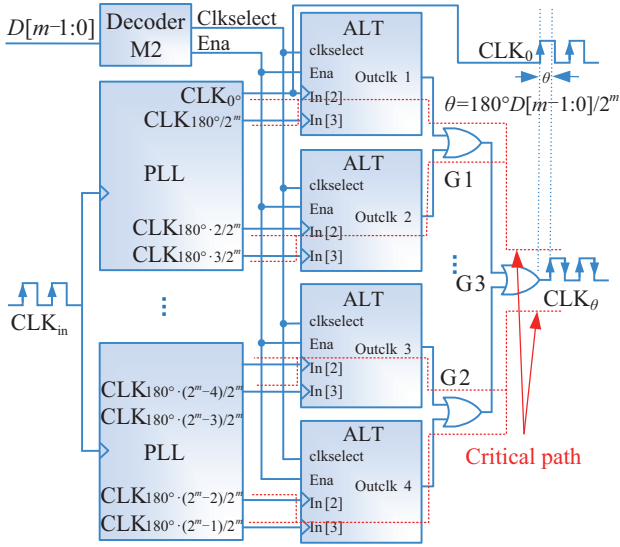


Fig. 10. Phase-shifted clock unit with proposed logically symmetric MUX.

Similar clock control blocks in FPGAs of other manufacturers, such as BUFGCTRL in Xilinx FPGA, can achieve the same function as the ALT block in Altera FPGA.

This paper uses ALT in Altera FPGA as an example to introduce the proposed synchronous clock phase shifting method. When ALT uses multiple input sources, the In[x] ports can only be driven by the dedicated clock input pins and the PLL clock outputs. Dedicated clock input pins must feed only In[0] and In[1], while the PLL clock outputs must feed only In[2] and In[3]. In this article, In[2] and In[3] are used to form a two-to-one multiplexer for selecting phase-shifted clocks from PLL.

As is shown in Fig. 10 and Table III, the phase-shifted clock from the PLL is selected by Clkselect, and the valid Outclk signal is output by the enable signal Ena in ALT. Turn off the Outclk clock by Ena in the unused ALT block. That is, only one ALT is working at the same time, and only one effective clock signal is output to ensure that the output clock signals of multiple ALT modules do not affect each other, and then pass through a symmetrical logic OR gate to obtain the phase-shifted clock signal CLK_θ .

C. The Reference PWM Signal Generation

The function of the reference PWM signal generation unit is to construct a coarse adjustment signal PWM_{Ref} for a high-resolution PWM signal, as shown in Fig. 11. The timing diagram is shown in Fig. 12.

1) Carrier Counter: Select the clock signal CLK_0 as the reference clock, and use the rising edge of the CLK_0 to generate a carrier counter. The period of the carrier counter is denoted as T_S . The carrier counter starts counting from 0, increasing by 1 for each reference clock cycle until the count period reaches T_S and the carrier counter is set to 0. Then, repeat the next cycle of counting.

2) Comparator: The value of the modulated signal is expressed as $D[n-1:m+1]$. When the Cnt value of the carrier counter is greater than $D[n-1:m+1]$, the PWM output is at a

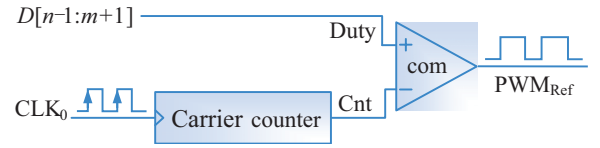


Fig. 11. Reference PWM signal generation unit.

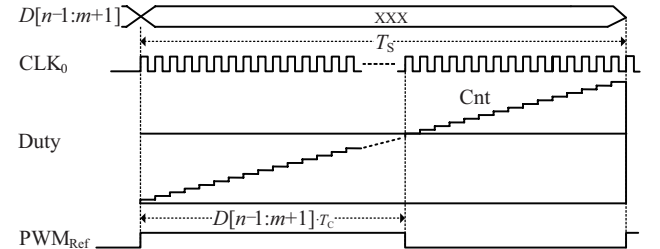


Fig. 12. Timing diagram of reference PWM signal.

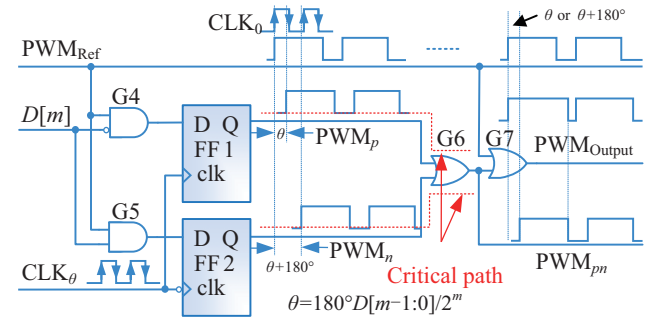


Fig. 13. Phase-shifted PWM signal unit with proposed synchronous two-to-one multiplexer.

low level. Otherwise, the PWM output is at a high level, and the reference PWM signal generated by this method is recorded as PWM_{Ref} :

$$PWM_{Ref} = \begin{cases} 0 & D[n-1:m+1] \leq Cnt \\ 1 & D[n-1:m+1] > Cnt \end{cases} \quad (5)$$

D. The Phase-Shifted PWM Signal Construction

As described in Fig. 13, the accurate delay time of the reference PWM_{Ref} signal is achieved by using the phase-shifted clock CLK_θ .

At the rising edge of the phase-shifted clock CLK_θ , the reference PWM_{Ref} signal is phase-shifted by θ with FF1, expressed as PWM_p .

Similarly, at the falling edge of the phase-shifted clock CLK_θ , the reference PWM_{Ref} signal is phase-shifted by $\theta+180^\circ$ with FF2, which is expressed as PWM_n .

In this paper, a synchronous two-to-one multiplexer is proposed, as shown in Fig. 13, to select the PWM signal while avoiding the influence of delay deviation caused by using a multiplexer. The selection signal $D[m]$ is placed at the front end of flip-flops FF1 and FF2. The PWM_{Ref} is sent to the data port D of the flip-flop after being selected by the AND gate G4 and

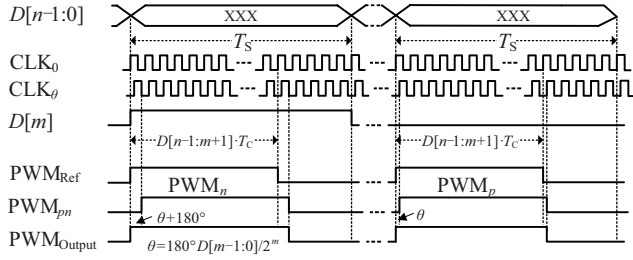


Fig. 14. Timing diagram of Phase-shifted PWM signal.

the AND gate G5. Under the flip-flop's clock synchronization, the AND gate's logic delay effect is eliminated.

When $D[m]$ is 0, the output signal of AND gate G4 is PWM_{Ref} and the output signal of AND gate G5 is 0. On the rising edge of CLK_θ , the PWM_{Ref} signal is output as PWM_p through the flip-flop FF1, and the output port data of the flip-flop FF2 is 0. That is, PWM_n is 0.

When $D[m]$ is 1, the output signal of AND gate G4 is 0, and the output signal of AND gate G5 is PWM_{Ref} . On the falling edge of CLK_θ , the PWM_{Ref} signal is output as PWM_n through flip-flop FF2, and the output port data of flip-flop FF1 is 0. That is, PWM_p is 0.

After the output signals of flip-flops FF1 and FF2 pass through the symmetrical logic OR gate G6, the desired phase-shifting PWM_{pn} signal can be selected.

After the phase-shifted PWM_{pn} signal and the PWM_{Ref} signal are processed by the OR gate G7, the high-resolution PWM_{Output} signal can be obtained as follows:

$$PWM_{Output} = \begin{cases} PWM_{Ref} | PWM_p & D[m] = 0 \\ PWM_{Ref} | PWM_n & D[m] = 1 \end{cases} \quad (6)$$

The timing diagram of the fine adjustment PWM_{Output} signal is shown in Fig. 14.

E. Pulse Width of the Proposed Method

According to the proposed method, when using PLL to generate 2^m phase-shifted clocks, the phase deviation of adjacent phase-shifted clocks is $180^\circ/2^m$. Select the required phase-shifted clock CLK_θ by the proposed symmetrical clock multiplexer.

The pulse width resolution of the PWM_{Output} is T_p , as shown in (4). The pulse width T_{PW} of PWM_{Output} is expressed as:

$$T_{PW} = D[n-1:m+1] \times T_C + D[m:0] \times T_p \quad (7)$$

The method proposed in this paper improves the pulse width resolution by a factor of 2^{m+1} .

F. Timing Diagram of the Proposed Method

By configuring the PLL, the clock signal with phase-interleaved delay is generated. Taking $N_p = 2$ and $N_c = 4$ as an example, then $m = 3$, the input modulation signal $D[n-1:0]$ takes 85 in decimal and 1010101 in binary, then the value of n is 7. This way, eight channels of phase-shifted clock signals with

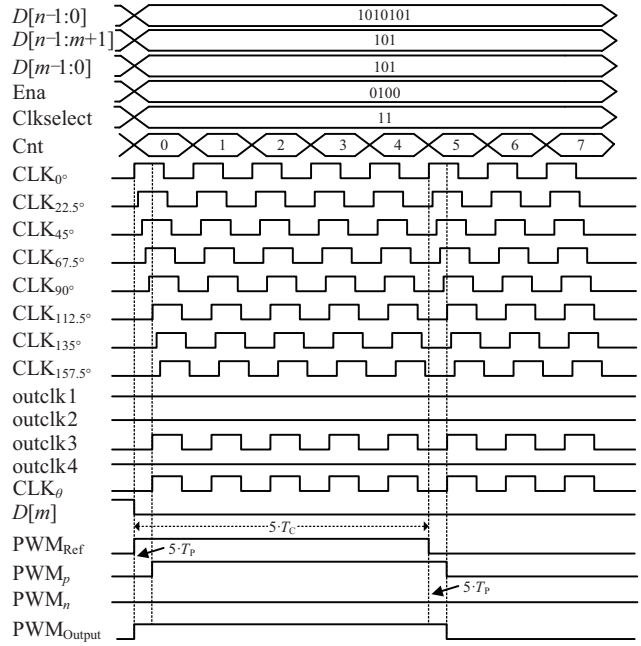


Fig. 15. Timing diagram of the proposed DPWM signal modulation method.

the same frequency and interleaved delay phase with 22.5° are generated. $D[n-1:m+1]$ is 101 in binary, and the pulse width of PWM_{Ref} signal is $5T_C$. According to Table II, $D[m-1:0]$ is 101 in binary, and the CLK_θ is selected as $CLK_{180^\circ \cdot (2^m - 3) / 2^m}$. When $m = 3$, the CLK_θ is $CLK_{112.5^\circ}$. $D[m] = 0$, the PWM_{Ref} signal is phase-shifted by 112.5° on the rising edge of $CLK_{112.5^\circ}$ to obtain PWM_p . The high-resolution PWM_{Output} signal can be obtained as (6) is $PWM_{Ref} | PWM_p$. The pulse width of the PWM_{Output} as (7) is $5T_C + 5T_p$.

The waveform of each stage of generating high-resolution PWM_{Output} is shown in Fig. 15.

III. LINEARITY AND POWER CONSUMPTION OPTIMIZATION WITH PROPOSED METHOD

A. Critical Path Analysis

In the high-resolution PWM signal generation method, the phase-shifting circuit is the critical path that affects the linearity of the PWM signal. In the traditional multiplexer method, the combinational logic in the critical path deteriorates the linearity of the PWM signal, as shown in Fig. 16.

1) The asymmetric critical path caused by the selection unit of the phase-shift clock CLK_θ : In the previous work, the multiplexer is usually composed of combinational logic to select the phase-shift clock, and LUT implements this combinational logic in FPGA. Depending on the FPGA, either 4-input or 6-input LUTs can be used. The 4-input LUT can form a 2-to-1 multiplexer, and the 6-input LUT can form a 4-to-1 multiplexer. In this article, using Altera Cyclone-IV series FPGA with 4-input LUT, the LUT unit's delay deviation range from different input ports to output ports is 0.15 ns to 0.5 ns. LUTs are combined in cascaded structures when multiplexers for more inputs are required.

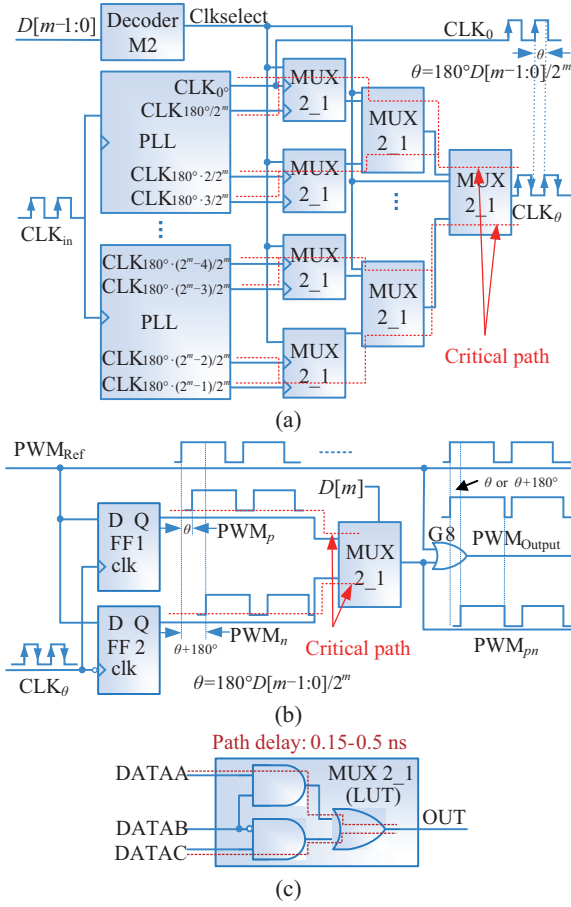


Fig. 16. (a) Phase-shifted clock unit with traditional MUX. (b) Phase-shifted PWM signal unit with traditional MUX. (c) LUT-based MUX 2_1 structure.

Synthesis tools will synthesize the multiplexer into an asymmetric structure, and the critical path delay of the phase-shifted clock selection unit will have a more significant deviation.

2) The asymmetric critical path caused by the selection unit of the phase-shifted PWM_{pm} signal: To generate the higher-resolution PWM signal, this paper uses the double-edge trigger function of the phase-shifted clock CLK_θ to generate two phase-shifted PWM_{pm} signals. Then, select the required phase-shift PWM signal through the multiplexer. The traditional multiplexer uses a 4-input LUT unit to form a 2-to-1 multiplexer, and the critical path has a delay deviation of 0.15-0.5 ns.

B. Critical Path Optimization

Due to the asymmetric structure of the traditional multiplexer, it will bring a more significant delay deviation, which is unsuitable for high-resolution PWM signals.

According to the method proposed in this paper, the linearity of the PWM signal can be significantly improved by optimizing the design of the selection unit with the symmetrical multiplexer. The logic symmetrical multiplexer for clock selection and synchronous 2-to-1 selector for phase-shifted PWM in verilog code is shown in Appendix A.

1) Logic Symmetrical Multiplexer: The proposed method uses eight clocks from the PLL, and an 8-to-1 multiplexer

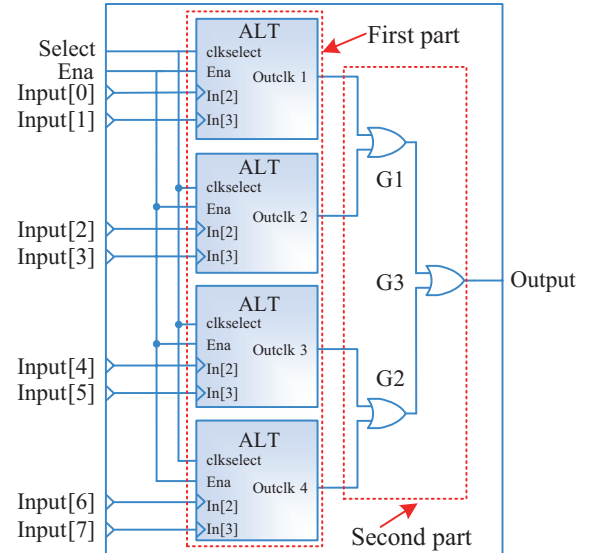


Fig. 17. Logic symmetrical 8-to-1 multiplexer.

needs to be constructed. For better illustration, the logic symmetric multiplexer in Fig. 10 is redrawn, as shown in Fig. 17.

The 8-to-1 multiplexer is divided into two parts. The first part uses the ALT IP core to select the clock signal from the PLL dynamically. As a unique clock selector, the ALT module can avoid the jitter of dynamic selection. Moreover, the logic delays from different clock input ports to output ports are entirely consistent. The ALT module has four input ports, only the In[2] and In[3] ports are allowed to access the PLL clock signal. To select eight clocks, use four ALT modules to construct four 2-to-1 clock selectors. Enable the corresponding ALT module according to Ena port. That is, only one input signal is output from four ALT modules simultaneously. The second part is composed of two-level logic OR gates. The function of the logic OR gate is to combine the output signals from the four ALT modules to ensure that the input signal can come from any ALT module. These logic OR gates are implemented by LUT units. Through timing analysis, although the delay deviations of the four input ports of the LUT in FPGA are different, the path delay deviation of the DATAA and DATAB ports are small. The 2-input OR gate can be formed by using the DATAA and DATAB ports with LUT, as shown in Fig. 18. By using 3 LUT units combined into a 4-input OR gate with a symmetrical structure, the delay deviation can be reduced.

The traditional multiplexer structure uses 7 LUT units, and the critical delay path with combinational logic contains three levels of LUTs. The logically symmetric multiplexer proposed in this paper only uses three LUT units, and the critical delay path of combinational logic is reduced to a two-stage LUT. The non-linear influence caused by the delay deviation of the clock multiplexer is significantly reduced.

2) Synchronous 2-to-1 selector: The Synchronous 2-to-1 selector in Fig. 13 is redrawn as shown in Fig. 19. The selection signal is placed at the front end of the flip-flop, and under the clock signal synchronization, the delay effect caused by the se-

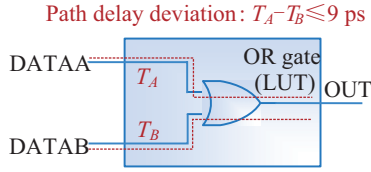


Fig. 18. The delay deviation of OR gate in LUT.

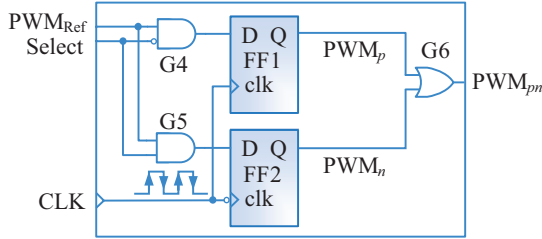


Fig. 19. Synchronous two-to-one multiplexer.

lection signal is eliminated. The function of the two-input OR gate G6 combines the outputs of the two flip-flops. The critical path of the synchronous 2-to-1 selector has only one logic OR gate, and the delay deviation of the combinational logic will be significantly improved.

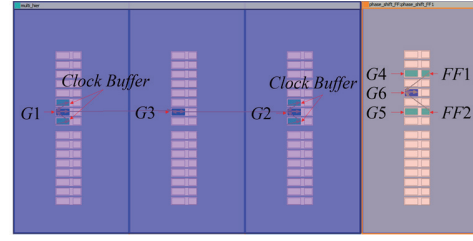
3) Placement and route constraints and the assignment of LUT input port: By optimizing the design of the selection unit in the critical path, the critical path of the synthesized clock selector and phase-shift PWM signal selector is logically symmetrical. In addition to considering the symmetry of the circuit structure, it is also necessary to ensure that the wiring delay of the combinational logic in the critical path is symmetrical. After optimization with the proposed method, the critical path of the clock selector contains three logical OR gates, and the critical path of the phase-shift PWM signal selector has one logical OR gate. Compared with traditional multiplexer method, the method proposed in this paper uses fewer logic gates and simpler placement and routing constraints.

According to the above analysis, the delay deviation of the DATAA and DATAB ports of the 4-input LUT unit is slight. However, the input port of the logical OR gate synthesized by the synthesis tool is not necessarily the DATAA and DATAB ports. Therefore, it is also necessary to allocate the ports of the 4-input LUT unit and ensure the input ports of the logic OR gate are DATAA and DATAB to minimize the delay deviation of the critical path.

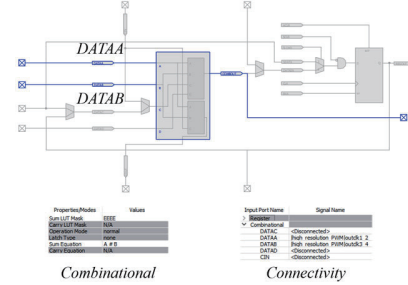
3.1 Placement and route constraints

The delay deviation of the critical path is reduced by placements and routing constraints on the four logic OR gates.

The logic OR gates G1, G2, and G3 are symmetrically placed in the same Logiclock regions, and each BLOCK of the FPGA allows simultaneous access to two global clock signals. Therefore, the Logiclock regions are set to 3 BLOCKs to ensure the minimum delay of the clock signals connected to the logic OR gates G1, G2, and G3. Similarly, the flip-flops FF1 and FF2 and the logic OR gate G6 are symmetrically placed in the same Logiclock regions.



(a)



(b)

Fig. 20. (a) Placement and routing constraints in chip planner. (b) Input port assignment of LUT in Resource Property Editor.

Using the Logiclock assignment function to fix the logic OR gates at the designated location of the FPGA to ensure that the path delays of the logic OR gates after compilation remain unchanged. The logic OR gates are placed symmetrically to reduce delay deviation. The location constraints of the logiclock are shown in Fig. 20(a).

3.2 The assignment of LUT input port

As shown in Fig. 20(b), use the Resource Property Editor to redistribute LUT input port signals and edit the logical relationship between input and output signals. In Connectivity, set LUT's DATAA and DATAB ports as input ports, and in Combinational, set the LUT's input and output signal relationship to OR logic. The configuration of logic OR gates G1, G2, G3, and G6 is completed as described above.

C. Critical Path Delay Comparison

The path delay comparison between the optimized selector proposed in this paper and the traditional multiplexer is shown in Fig. 21. For the selection unit of the phase-shifted clock CLK_{ϕ} , the maximum delay deviation by the traditional multiplexer is 1.135 ns, and the method proposed in this paper is 60 ps. For the selection unit of the phase-shifted PWM_{pn} signal, the maximum delay deviation by the traditional multiplexer is 0.164 ns, and the method proposed in this paper is 9 ps. The proposed method has better symmetry and minor delay deviation in the critical path.

D. Power Consumption Optimization

The proposed method uses eight clocks of the PLL. Using traditional multiplexers, the power consumption of FPGA is relatively large and requires eight clocks to work simultaneously. The optimized method prohibits the unused clock output by using the enable function of the ALT module to ensure that

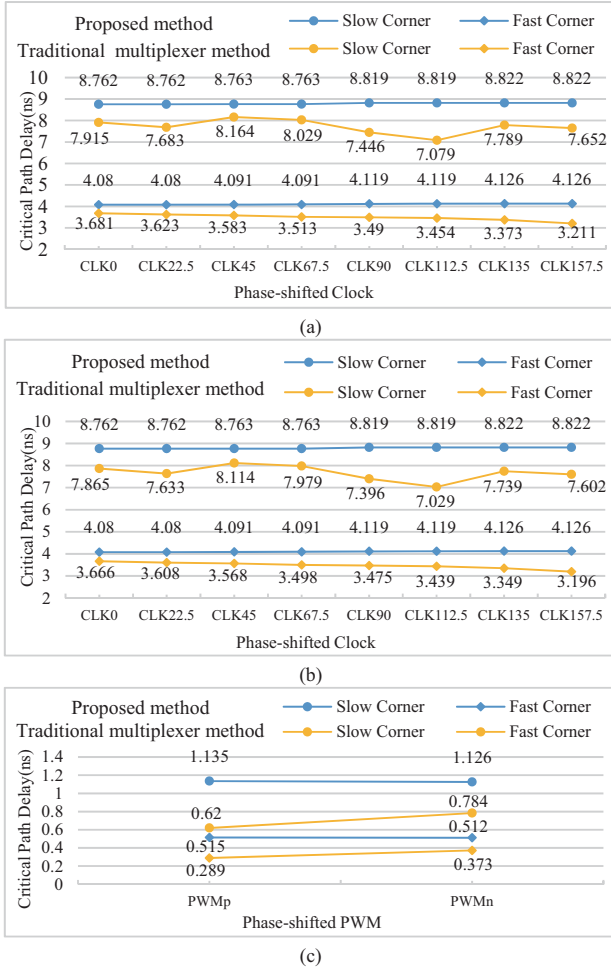


Fig. 21. (a) The simulation critical path delay of CLK_{θ} from PLL to FF1. (b) The simulation critical path delay of CLK_{θ} from PLL to FF2. (c) The simulation critical path delay from FF1 and FF2 to logic OR gate G6.

only one phase-shifted clock works simultaneously. The power consumption of FPGA can be reduced. Power consumption was evaluated using the PowerPlay Early Power Estimator, as shown in Fig. 22 and Table IV.

IV. PERFORMANCE EVALUATION AND EXPERIMENTAL RESULTS OF THE PROPOSED METHOD

According to the proposed method, the program design is completed in the different FPGA. By timing analysis and critical path optimization, the high-resolution DPWM is realized. It is verified by simulation and experiments.

A. Simulation Results

- The detailed simulation parameters are as follows:
- The reference clock frequency: 200 MHz
 - The modulation signal $D[n-1:0]$: 85
 - PWM signal switching frequency: 1 MHz.

The simulation waveform of Cyclone IV FPGA is shown in Fig. 23(a), and the simulation waveform of Atrix7 FPGA is shown in Fig. 23(b). The period of the reference clock is 5 ns,

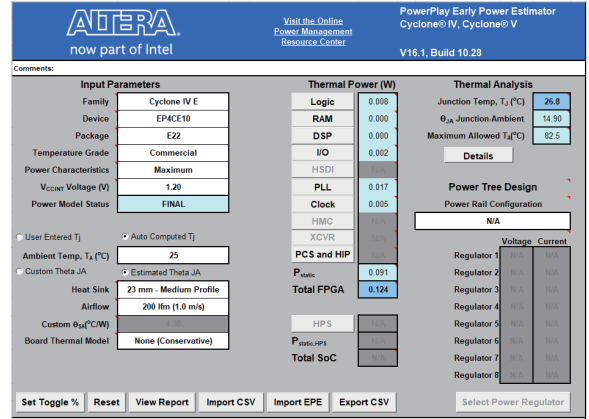


Fig. 22. PowerPlay Early Power Estimator for Altera FPGA.

TABLE IV
POWER CONSUMPTION OF TRADITIONAL MULTIPLEXER METHOD AND PROPOSED METHOD

| Method | Clock working status | Power consumption |
|--------------------------------|-----------------------------|-------------------|
| Traditional multiplexer method | 8 clocks run simultaneously | 0.138 W |
| Proposed method | one clock run | 0.124 W |

and the single-step adjustment resolution of PWM_{Output} is 312.5 ps. The value of $D[n-1:0]$ takes 85 in decimal, 1010101 in binary. $D[n-1:m+1]$ is 101 in binary, $D[m]$ is 0, and $D[m-1]$ is 101. The CLK_{θ} comes from $CLK_{112.5^{\circ}}$. The PWM_{Ref} is shifted to 1.562 ns with $CLK_{112.5^{\circ}}$. The pulse width of PWM_{Output} is 26.562 ns.

B. Experimental Results

1) Experiments Results for the Cyclone IV FPGA

To verify the performance of the proposed method, experiments were carried out on the Cyclone IV FPGA.

The pulse width test results of the traditional multiplexer method and the proposed method in the Cyclone IV FPGA are shown in Fig. 24, and the modulation signal $D[n-1:0]$ of DPWM changes from 16 to 127. The linearity of the traditional multiplexer is 0.99951, and the linearity of the proposed method is 0.99999, which is close to 1.

The high-resolution DPWM signal is constructed by the phase-shifted PWM_{pn} signal generated by the CLK_{θ} and the PWM_{Ref} signal generated by CLK_0 . As shown in Fig. 25, the delay path of the CLK_0 and CLK_{θ} are inconsistent, which will cause a constant pulse width deviation T_{CO} between the high-resolution DPWM signal and the ideal DPWM signal.

As shown in Fig. 26(a), there is a constant delay deviation between the high-resolution DPWM signal proposed in this paper and the ideal DPWM signal. According to the architecture proposed in this paper, by setting an initial offset for the modulation signal $D[n-1:0]$, the constant pulse width deviation T_{CO} can be easily compensated. The constant pulse width deviation does not affect the linearity and resolution of the high-resolution PWM signal. Therefore, no compensation is made for the constant pulse width deviation in this paper.

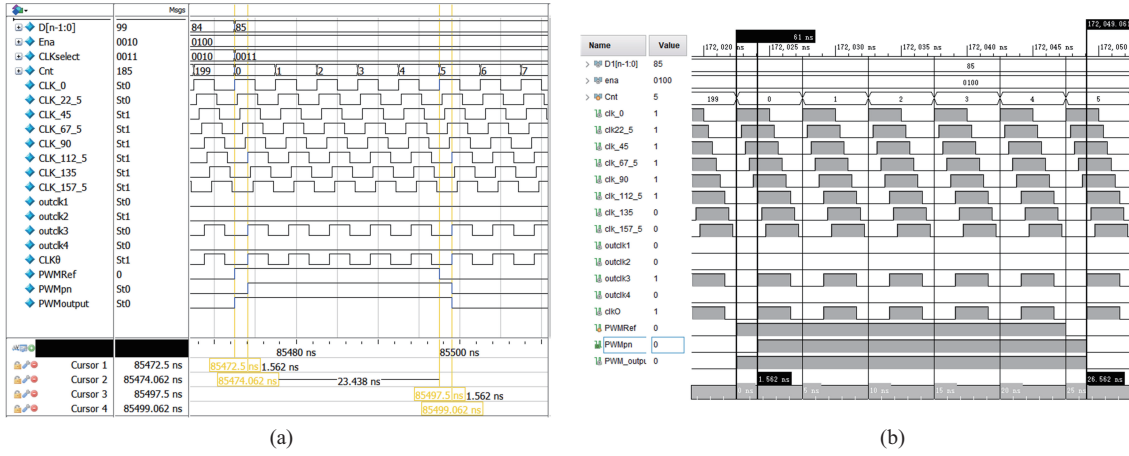


Fig. 23. (a) Simulation waveform for generating high-resolution PWM in the Cyclone IV FPGA. (b) Simulation waveform for generating high-resolution PWM in the Atrix7 FPGA.

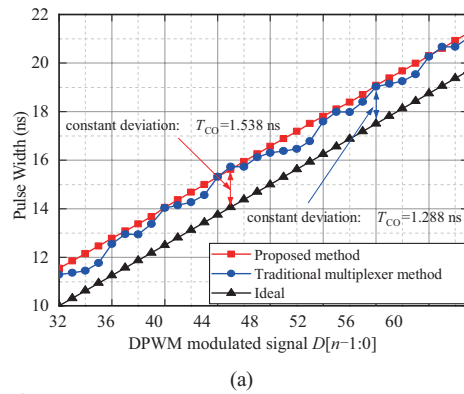
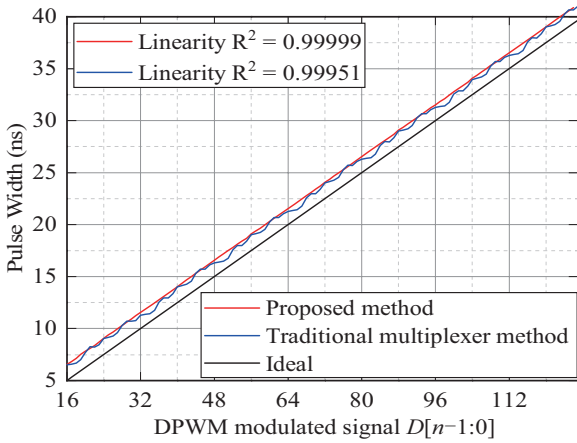


Fig. 24. Comparison of linearity between the traditional multiplexer method and the proposed method in the Cyclone IV FPGA.

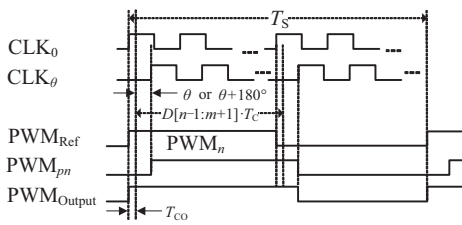


Fig. 25. Timing diagram of constant pulse width deviation with the proposed architecture.

The pulse signal varies from 11.286 ns to 21.052 ns of DPWM by the traditional multiplexer, as shown in Fig. 26(b), the modulation signal $D[n-1:0]$ changes from 0000_0010_0000 to 0000_0011_1111 in binary, which is from 32 to 63 in decimal, and the non-linear deviation of the pulse width is relatively large.

The pulse signal waveform of DPWM by the method proposed in this paper is shown in Fig. 26(c) with the same changing modulation signal $D[n-1:0]$. The pulse width varies uniformly from 11.547 ns to 21.240 ns with the modulation signal $D[n-1:0]$ and has excellent linearity. Taking $D[n-1:0] = 63$ in decimal as an example, the $D[n-1:m+1] = 3$, the $D[m] =$

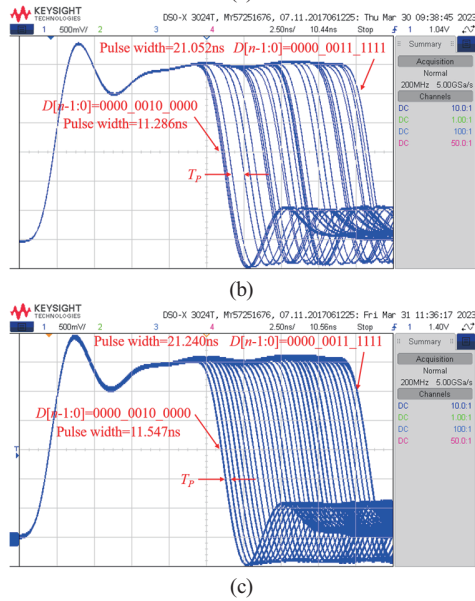


Fig. 26. (a) The constant deviation between the traditional multiplexer method and the proposed method in the Cyclone IV FPGA. (b) The pulse signal of the traditional multiplexer method with the modulated signal from 32 to 63 in the Cyclone IV FPGA. (c) The pulse signal of the proposed method with the modulated signal from 32 to 63 in the Cyclone IV FPGA.

1, the $D[m:0] = 15$, and the pulse width T_{PW} is: $T_{CO} + 3 \cdot T_C + 15 \cdot T_p = 1.538 \text{ ns} + 3 \cdot 5 \text{ ns} + 15 \cdot 0.3125 \text{ ns} = 21.2255 \text{ ns}$, the absolute

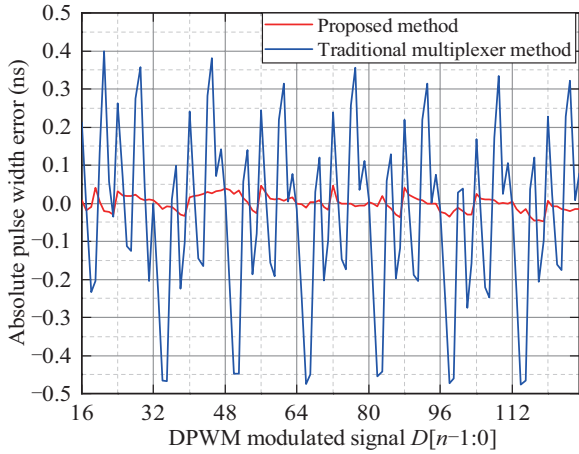


Fig. 27. Absolute pulse width error of DPWM with modulation signal $D[n-1:0]$ from 16 to 127 in the Cyclone IV FPGA.

error of the pulse width is $21.24 \text{ ns} - 21.2255 \text{ ns} = 0.0145 \text{ ns}$. When the absolute error of the pulse width is considered, the effect of constant delay deviation T_{CO} between the PWM_{Ref} signal and the phase-shifted PWM_{pn} signal can be ignored. Fig. 27 shows the pulse width absolute error of DPWM without T_{CO} with the modulation signal $D[n-1:0]$ from 16 to 127. The maximum absolute pulse width deviation between the high-resolution DPWM signal generated by the traditional multiplexer and the ideal DPWM signal is 0.4765 ns. The maximum absolute pulse width deviation is 48.5 ps with the proposed method. According to the architecture proposed in this paper, the DPWM signal will be fine-tuned at a 1/16 clock cycle. The experimental results show that the proposed method achieves high-resolution PWM output with high linearity in the Cyclone IV FPGA.

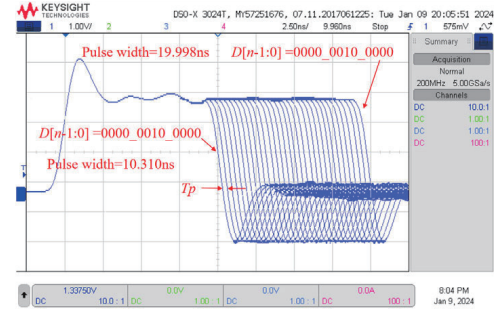
2) Experiments Results for the Atrix7 FPGA

In order to better illustrate the versatility of the proposed method. The same experimental verification was performed on Atrix7 series FPGA from Xilinx, the cascaded BUFGCTRL is used to replace the ALT realize the selection of the phase-shifted clock from the PLL. The experimental results are shown in Fig. 28. The pulse width varies with the modulation signal $D[n-1:0]$ changes from 0000_0010_0000 to 0000_0011_1111 in binary, which is from 32 to 63 in decimal are shown in Fig. 28(a). As shown in Fig. 28(b), the linearity reaches 0.99999, which is close to 1. Fig. 28(c) shows the pulse width absolute error of DPWM without T_{CO} , and the maximum absolute pulse width deviation is 20.5 ps with the proposed method in the Atrix7 FPGA.

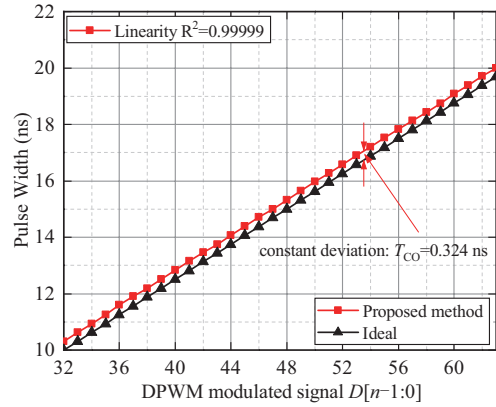
The experimental results show that the proposed method can achieve high-resolution PWM output and high linearity in different FPGAs, and has good versatility.

C. Resource Occupancy of FPGA

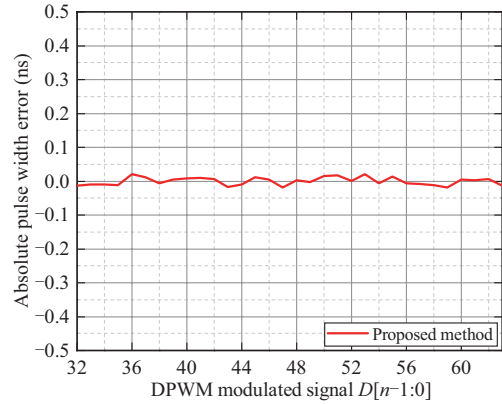
According to the above method, the high-resolution DPWM can be simply realized. The maximum value of modulation signal $D[n-1:0]$ is 3200 in decimal with a switching frequency of 1 MHz. The effective bits of the DPWM are close to 12 bits. The high-resolution DPWM module uses 63 LUTs (0.61%), 27 FFs (0.26%), 2 PLL modules, and 4 ALT modules, taking up



(a)



(b)



(c)

Fig. 28. (a) The pulse signal of the proposed method with the modulated signal from 32 to 63 in the Atrix7 FPGA. (b) The constant deviation and linearity of proposed method in the Atrix7 FPGA. (c) Absolute pulse width error of DPWM with modulation signal $D[n-1:0]$ from 32 to 63 in the Atrix7 FPGA.

fewer resources with the available 10320 logic element in the Cyclone IV FPGA. The high-resolution DPWM module uses 39 LUTs, 27 Registers, 2 PLL modules, and 7 BUFGCTRL modules in the Atrix7 FPGA.

D. Comparative Analysis With Different DPWM Method

Table V summarizes the performance comparison based on the phase-shifted clock and the proposed methods. The degree of difficulty from easy to difficult: extremely easy, easier, generally easy, difficult.

[4] achieves 12.5 ns resolution with 10 MHz clock frequency. If the clock frequency in [4] is increased to 200 MHz, the

TABLE V
COMPARISON OF DIFFERENT DPWM METHODS

| Ref | Degree of Difficulty | Device | Resolution | Resolution Deviation | Linearity R ² |
|------------|----------------------|-----------------------------|------------|----------------------|--------------------------|
| [4] | extremely easy | Altera EP4CE22F17C6 | 12.5 ns | NA | NA |
| [6] | easier | XC3S200F T256-4 | 2 ns | 450 ps | 0.994 |
| [5] | easier | Spartan-3 XC3S1000 -FT256-4 | 2 ns | 350 ps | NA |
| [13] | generally easy | Artix-7 | 625/500 ps | NA | NA |
| [3] | generally easy | Virtex4 XC4VSX3 5 FFG668 | 156 ps | NA | NA |
| [19] | difficult | XC7A100 TFGG484 | 1.25 ns | 500 ps | NA |
| [17] | difficult | Altera EP4CE15F23C8N | 41.3 ps | 130 ps | 0.9994 |
| [16] | difficult | Artix-7 | 32 ps | 130 ps | 0.99 |
| This paper | extremely easy | General FPGA | 312.5 ps | 48.5/20.5 ps | 0.99999 |

resolution becomes 625 ps. Compared with [4], this paper makes full use of the double-edge triggering of the phase-shifted clock to achieve a lower resolution, and the resolution is reduced to 312.5 ps.

[5] and [6] use a 128 MHz clock to achieve a resolution of 2 ns, and there is a multiplexer on the critical path. The linearity of [6] is low, and the linearity deviation is large, reaching 450 ps. Although [5] uses manual placement and routing to compensate for the critical path delay deviation, the resolution deviation is still large, reaching 350 ps.

[13] uses two methods to construct high-resolution DPWM. The first method is to use DCM to construct four reference phase-shift clocks and use eight D-triggers to generate 8-way phase-shift delay circuits with a resolution of 625 ps, and its linearity is limited by the D-triggers and multiplexers on the critical path. The second method uses LUT units to construct a delay circuit with a resolution of 500 ps, and its resolution is limited by the device's speed level. These two methods are simple in structure but require strict layout and routing constraints on D-triggers, multiplexers, and LUT units.

[3] uses multiple cascaded DCMs to achieve a resolution of 156 ps. There are multi-stage multiplexers on the critical path, which greatly reduces linearity. The more DCMs used, the greater the linearity deviation.

In order to obtain a higher DPWM resolution, [16], [17] use a hybrid DPWM architecture, which consists of a first-stage phase-shift clock and a second-stage adder carry chain. [11] carried out manual layout and routing optimization on the multiplexer for phase-shift clock selection and adder delay line used in the critical path, and the optimized linearity was 0.9949. [16] and [17] use D-triggers and logic gate circuits to optimize the clock selection delay unit, which further reduces the delay deviation of the critical path. The optimized linearity is 0.994 and 0.99, respectively, but these two methods increase the circuit complexity. Although the hybrid DPWM architec-

TABLE VI
TECHNICAL SPECIFICATIONS OF DC/DC CONVERTER

| Item | Requirements |
|-------------------|----------------------|
| Input voltage | 48 V |
| Output voltage | 0.99 V~1.01 V@100 A |
| Voltage overshoot | < 150 mV @50 A-150 A |
| Output power | 200 W |
| Volume | < 90 mm*55 mm*50 mm |

ture achieves higher resolution, the operation is complex, and the versatility is low, and its resolution is mainly affected by the carry chain of the second-stage adder. The delay deviation of the carry chain of the second-stage adder is greatly affected by the device, and it needs careful layout and routing to obtain better linearity.

Compared to the other methods in Table V. Although the resolution of the method proposed in this article does not reach the minimum, it has a simple structure and high reliability. The proposed method constructs the symmetric multiplexers for phase-shifted clock signals and the synchronous 2-to-1 multiplexer for selecting phase-shifted PWM signals. Then, the simple placing and routing constraints are used to compensate for critical delay paths. Achieved linearity as high as 0.99999, and the resolution deviation is smaller than other methods. The resources used in the proposed method can be obtained from other types of FPGA, which have good universality and are easy to transplant.

E. Application of Proposed Method to a DC/DC Converter

This method is applied to a 48 V to 1 V/200 A DC/DC converter that powers the CPU. The technical specifications of the converter are shown in Table VI.

Since the CPU has high requirements on the volume and dynamics of the power supply, the converter is required to have very high efficiency, power density, and control bandwidth. In order to meet the power supply needs of the CPU, this paper designs a two-stage high-efficiency DC/DC converter, which consists of a DC transformer (DCX) and an interleaved buck converter. The DCX is used to achieve high-efficiency conversion from 48 V to 5 V, which is achieved by an LLC converter working at the resonance point with a switching frequency of 1 MHz. The buck converter uses an interleaving method with a switching frequency of 1 MHz to achieve high efficiency and high dynamics response. The circuit structure and control diagram of the DC/DC converter are shown in Fig. 29.

The converter test platform mainly includes input power supply, DC/DC converter, electronic load, and oscilloscope, as shown in Fig. 30. To validate the proposed high-resolution DPWM method, the steady-state and dynamic performance of the output voltage is tested.

As shown in Fig. 31, the output voltage of the DC/DC converter from 0.99 V to 1.01 V with DPWM single-step change. Compared with the traditional multiplexer method, the proposed method in this paper achieves better control accuracy and linearity.

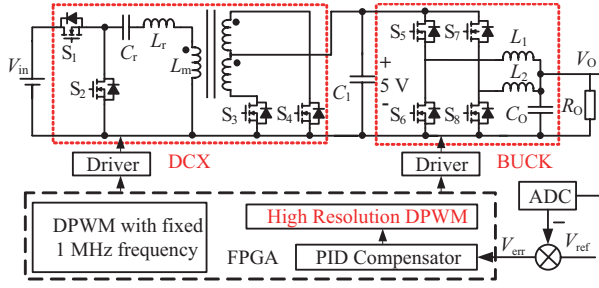


Fig. 29. The structure of 48 V to 1 V/200 A DC/DC converter.

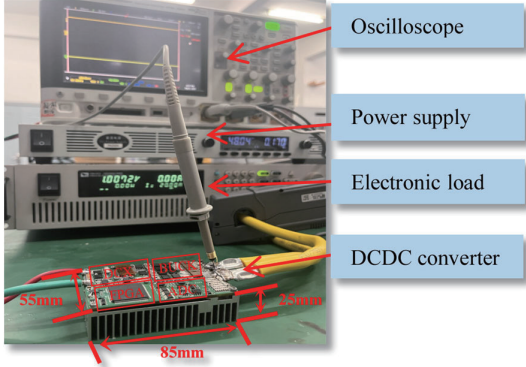


Fig. 30. Experimental platform of DC/DC converter.

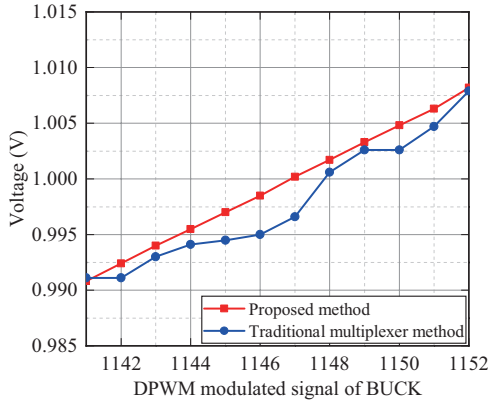


Fig. 31. The output voltage of converter with DPWM single-step change.

The converter operates with a load of 100 A, and the output voltage and current curve is as shown in Fig. 32 with proposed method.

The ADC of the DC/DC converter is LTC2311-12 with a resolution of 1 mV. Considering the influence of integral non-linearity (INL), discarding the lowest bit of the ADC, its effective resolution is 2 mV.

When the proposed high-resolution DPWM method is used, the single-step adjustment accuracy of the output voltage is:

$$\Delta V_O = 5 \text{ V} \times \frac{0.313 \text{ ns}}{1000 \text{ ns}} = 1.565 \text{ mV} \quad (8)$$

The resolution of DPWM is smaller than that of ADC, which meets the output voltage control accuracy requirements.

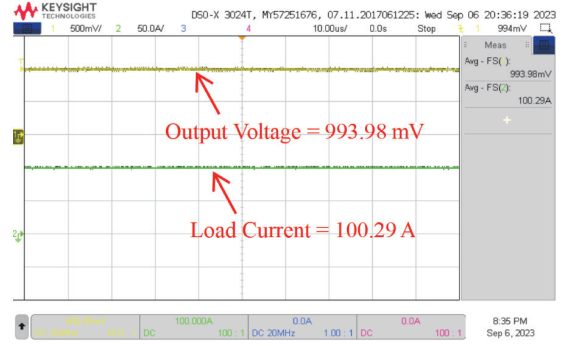


Fig. 32. The output voltage and current of DC/DC converter in steady state operation.

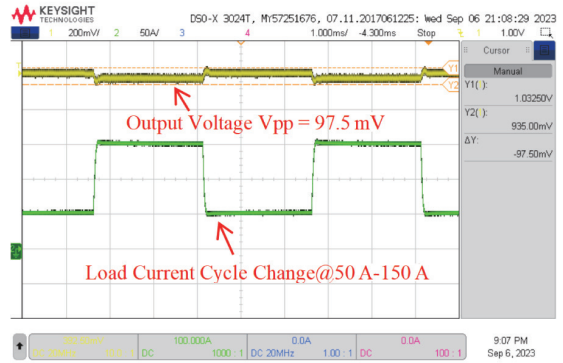


Fig. 33. The output voltage and current of DC/DC converter in transient state operation.

When the load jumps from 50 A to 150 A at a rate of 100 A/μs, the output voltage and current waveforms are shown in Fig. 33, and the voltage overshoot is 97.5 mV. After the transient process is over, the output voltage runs stably around 1 V.

The output voltage steady-state and dynamic performance test results show that the output voltage accuracy of the DC/DC converter meets the design requirements, and the output voltage has no limit cycle oscillation. The effectiveness of the proposed method has been verified.

V. CONCLUSION

This paper proposes the high-resolution DPWM signal modulation method based on FPGA, which uses the PLL of FPGA and the double-edge trigger function of the clock to achieve high-resolution DPWM. The logically symmetric clock multiplexers and synchronous 2-to-1 selector with simple placement and routing constraints are used to optimize the critical delay paths for high-resolution DPWM signals. The linearity of the DPWM signal is significantly improved, and the use of logic cell resources is slight. The resolution of DPWM is improved by 16 times. The power consumption of FPGA is reduced through the ALT module to disable unused phase-shift clocks. The effectiveness of this method is verified by simulation and experiment in different FPGA. The proposed architecture achieves a resolution of 312.5 ps, and its maximum delay deviation is 48.5 ps with high linearity, where R^2 is up to 0.99999.

Finally, the proposed method is verified in a 48 V to 1 V DC/DC converter with the switching frequency of 1 MHz.

APPENDIX A

VERILOG HDL CODE FOR SYMMETRICALLY CLOCK MULTIPLEXERS AND SYNCHRONOUS 2-TO-1 SELECTOR

```

module Clock_MUX (
input  clk_50M,
input  rst_n,
input  [11:0] D,
output clk_200M_0,
output clk_out
);
wire clk_200M_0/*synthesis keep*/;
wire clk_200M_22_5/*synthesis keep*/;
wire clk_200M_45/*synthesis keep*/;
wire clk_200M_67_5/*synthesis keep*/;
wire clk_200M_90/*synthesis keep*/;
wire clk_200M_112_5/*synthesis keep*/;
wire clk_200M_135/*synthesis keep*/;
wire clk_200M_157_5/*synthesis keep*/;
reg [3:0] Ena;
reg [3:0] Clkselect;
wire outclk1/*synthesis keep*/;
wire outclk2/*synthesis keep*/;
wire outclk3/*synthesis keep*/;
wire outclk4/*synthesis keep*/;
wire outclk1_2/*synthesis keep*/;
wire outclk3_4/*synthesis keep*/;
wire clk_out;
// PLL for 8 phase-shifted clocks
PLL_200M_M1 PLL_200M_M1 (
.areset(rst_n),
.inclk0(clk_50M),
.c0(clk_200M_0),
.c1(clk_200M_22_5),
.c2(clk_200M_45),
.c3(clk_200M_67_5),
);
PLL_200M_M2 PLL_200M_M2 (
.areset(rst_n),
.inclk0(clk_50M),
.c0(clk_200M_90),
.c1(clk_200M_112_5),
.c2(clk_200M_135),
.c3(clk_200M_157_5),
);
// Decoder for Altclkctrl module
always@(*)begin
case(D[2:0])
4'd0:begin Ena <= 4'b0001;Clkselect <= 2'b10; end
4'd1:begin Ena <= 4'b0001;Clkselect <= 2'b11; end
4'd2:begin Ena <= 4'b0010;Clkselect <= 2'b10; end
4'd3:begin Ena <= 4'b0010;Clkselect <= 2'b11; end
4'd4:begin Ena <= 4'b0100;Clkselect <= 2'b10; end
4'd5:begin Ena <= 4'b0100;Clkselect <= 2'b11; end
4'd6:begin Ena <= 4'b1000;Clkselect <= 2'b10; end
4'd7:begin Ena <= 4'b1000;Clkselect <= 2'b11; end
endcase
end
//Select phase-shifted clock
Altclkctrl Altclkctrl_inst1 (
.clkselect ( Clkselect ),
.ena ( Ena[0] ),
.inclk2x ( clk_200M_0),
.inclk3x ( clk_200M_22_5 ),
.outclk ( outclk1 )
);
Altclkctrl Altclkctrl_inst2 (
.clkselect ( Clkselect ),

```

```

.ena ( Ena[1] ),
.inclk2x ( clk_200M_45 ),
.inclk3x ( clk_200M_67_5 ),
.outclk ( outclk2 )
);
Altclkctrl Altclkctrl_inst3 (
.clkselect ( Clkselect ),
.ena ( Ena[2] ),
.inclk2x ( clk_200M_90 ),
.inclk3x ( clk_200M_112_5 ),
.outclk ( outclk3 )
);
Altclkctrl Altclkctrl_inst4 (
.clkselect ( Clkselect ),
.ena ( Ena[3] ),
.inclk2x ( clk_200M_135 ),
.inclk3x ( clk_200M_157_5 ),
.outclk ( outclk4 )
);
// OR gate with a symmetrical structure for clock
or(outclk1_2,outclk1,outclk2);
or(outclk3_4,outclk3,outclk4);
or(clk_out,outclk1_2,outclk3_4);
endmodule
module Phase_Shift_PWM_MUX (
input clk_out,
input rst_n,
input [11:0] D,
input PWM_Ref,
output PWMpn
);
reg PWMp;
reg PWMn;
//PWM_Ref is phase shifted with  $\theta$  degrees by the clk_out
always @(posedge clk_out or negedge rst_n) begin
if (!rst_n)
PWMp <= 1'd0;
else if(D[3])
PWMp <= 1'd0;
else PWMp <= PWM_Ref;
end
//PWM_Ref is phase shifted with  $\theta+180^\circ$  degrees by the clk_out
always @(negedge clk_out or negedge rst_n) begin
if (!rst_n)
PWMn <= 1'd0;
else if(D[3])
PWMn <= PWM_Ref;
else PWMn <= 1'd0;
end
//OR gate for ouput PWMpn
or(PWMpn,PWMp,PWMn);
endmodule

```

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