The High Voltage Gain Coupled Inductor Boost-Zeta DC/DC Converter

Xupeng FANG, Xuewen LAI, Xuchao WANG, and Hang ZHAO

***Abstract*—This paper presents boost-zeta DC/DC converters utilizing coupled inductors, suitable for applications in the field of new energy power generation. The converters have high voltage gain, lower power switch stress, and cost characteristics. The boost substructure of the converters contains a diode and buffer circuit, which can effectively suppress the voltage spike caused by leakage inductance, and ensure the power level and efficiency of the converters. This paper introduces the working principle and steady-state performance of the improved converter in the case of continuous and intermittent excitation inductor current, and compares it with other coupled inductor DC-DC converters in terms of voltage gain, power switch stress, efficiency, and circuit components. Finally, the improved converter is validated by simulation and experiment. A prototype is built in the laboratory to verify the correctness of the theoretical analysis.**

***Index Terms*—Boost-Zeta converter, coupled inductor, device stress, high voltage gain.**

I. Introduction

In recent years, in the face of rising global energy demand and rising prices of traditional fossil energy, countries around the world have shown unprecedented research interest in renewable energy [1], [2]. However, the output voltage of renewable energy generation such as photovoltaics and fuel cells is low voltage, and it needs to go through a first-stage DC boost converter to reach the grid-connected inverter DC bus voltage level. In order to meet this demand, DC converters are rapidly evolving towards higher gain, higher efficiency, and smaller size [3]–[6].

Although traditional boost converters have been widely used in low boost applications, their output voltage can only be adjusted by changing the on-duty cycle of the power switch, which often leads to increasing power loss and electromagnetic interference (EMI) when applied to higher voltage gains [7], [8]. Therefore, based on the traditional boost converter, scholars have proposed a variety of boost structures to improve the converter's performance. Currently, widely used boost technologies include multilevel voltage doubling technology (including staggered parallel, cascade, and topology combination), voltage doubling structure voltage doubling technology (including switched inductor, switched capacitor, and their combination), and magnetic coupling voltage doubling technology.

[9], [10] adopted the staggered parallel connection method, where the front stage of the converter is connected in parallel and the second stage in series. Such a structure has the advantages of small input current ripple, good stability, and high voltage gain. However, the ripples of the parallel connected output voltages of the converter are the same, which puts forward higher requirements for output capacitor and control strategy. [11]–[13] adopted a cascaded structure, and although the output voltage of the converter is greatly increased, the reliability is reduced by the large power switch and diode voltage stress in the post-stage structure. [14]–[16] adopted a switched inductor and capacitor structure, the proposed circuit structure is flexible and the voltage gain is further improved. However, the series and parallel switching of inductor or capacitor components will produce a large induced current and voltage, which will also lead to EMI deterioration. [17]–[19] embedded the coupled inductor into the converter, reducing the number of components used. The output voltage is determined by the cycle and the turns ratio of the coupling inductor, making the circuit structure more flexible and reliable while the voltage gain is high. However, it is necessary to introduce a snubber circuit to recover the leakage inductance energy of the coupled inductor to limit the voltage spike during the operation of the switch. [20]–[24] combined two basic DC converters and then added coupled inductor structures to obtain a variety of coupled inductor combination boost converters. There is also a passive buffer circuit that absorbs leakage inductor energy, and the steady-state performance of the converter is greatly improved.

In this paper, a class of high voltage gain coupled inductor Boost-Zeta converters is proposed by using topological combination technology and magnetic coupling voltage doubling technology. Among them, the I-type, II-type, and other extended converter structures are more complex. However, the improved converter structure is simplified, while still ensuring higher output voltage, lower component voltage stress, and good steady-state performance.

II. Converter Topology

To obtain a DC converter with a higher output voltage and

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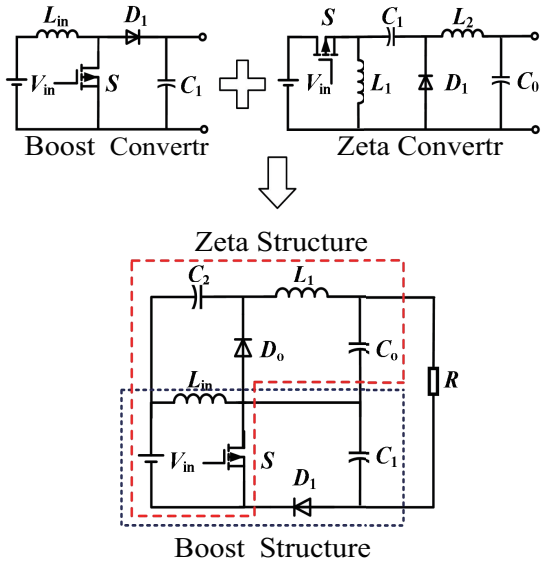


Fig. 1. Boost-zeta converter.

power density, the input side of the Boost-Zeta converters are shared, and the output side is connected in series to obtain the Boost-Zeta converter as shown in Fig. 1. To obtain a higher and more versatile output voltage, the input and output inductors in the Boost-Zeta converter are replaced with a coupled inductor, in conjunction with capacitors and diodes, forms a coupled inductor voltage multiplier Zeta structure (CI-ZETA). This results in two types of converters namely type I and type II, as shown in Fig. 2(a) and (b). Both types of converters resemble the converters mentioned in the [19]. Although the voltage gain is high, the circuit structure is slightly more complex.

Improve the circuit structure of the type II coupled inductor Boost-Zeta converter shown in Fig. 2(b) to increase the power density. Under the premise of following the charge and discharge law of the coupling inductor voltage doubling structure, the diode D_0 is moved to the output end. This changes the working process of the voltage doubler capacitor C_1 in one cycle from charging first and then discharging to first discharging and then charging. At this time, C_3 coupled inductor N_s terminal, and inductor L_{in} form a loop. According to the volt-sec balance principle of L_{in} and coupled inductor N_s terminal, the voltage of C_3 after steady state remains 0. Therefore C_3 can be omitted here and N_s with L_{in} are shared. Finally the improved converter is obtained and is shown in Fig. 2(c).

Compared with the two types I and II, the improved structure reduces the number of components used and improves the system efficiency while ensuring the same voltage gain. This paper analyzes such structures using the improved converter as an example and compares them with types I and II topologies and other coupled inductor converters.

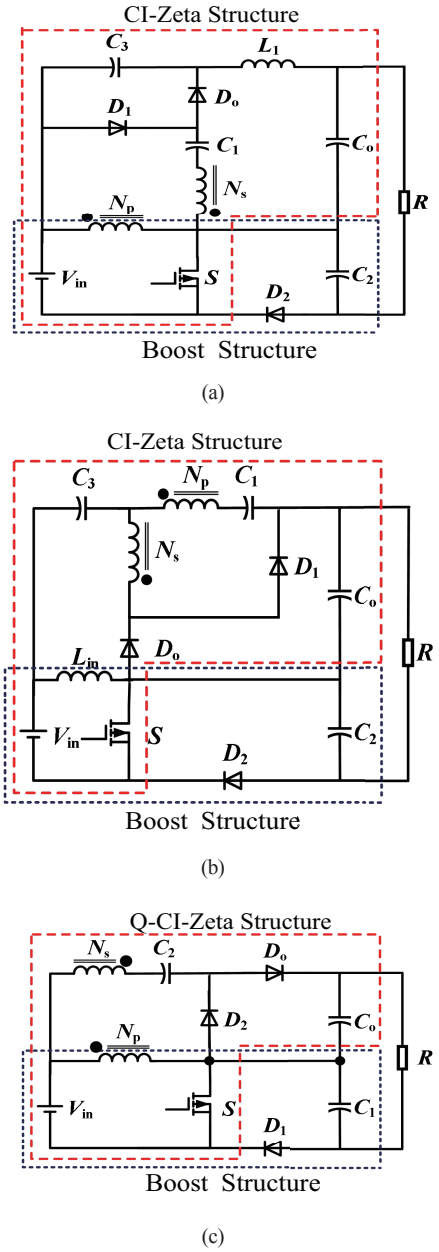


Fig. 2. Coupled inductor Boost-Zeta converters.

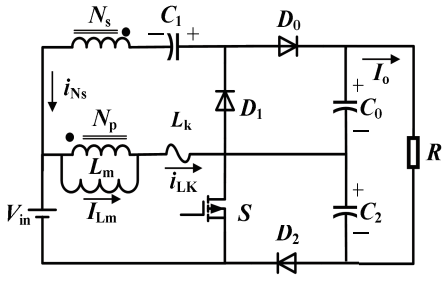
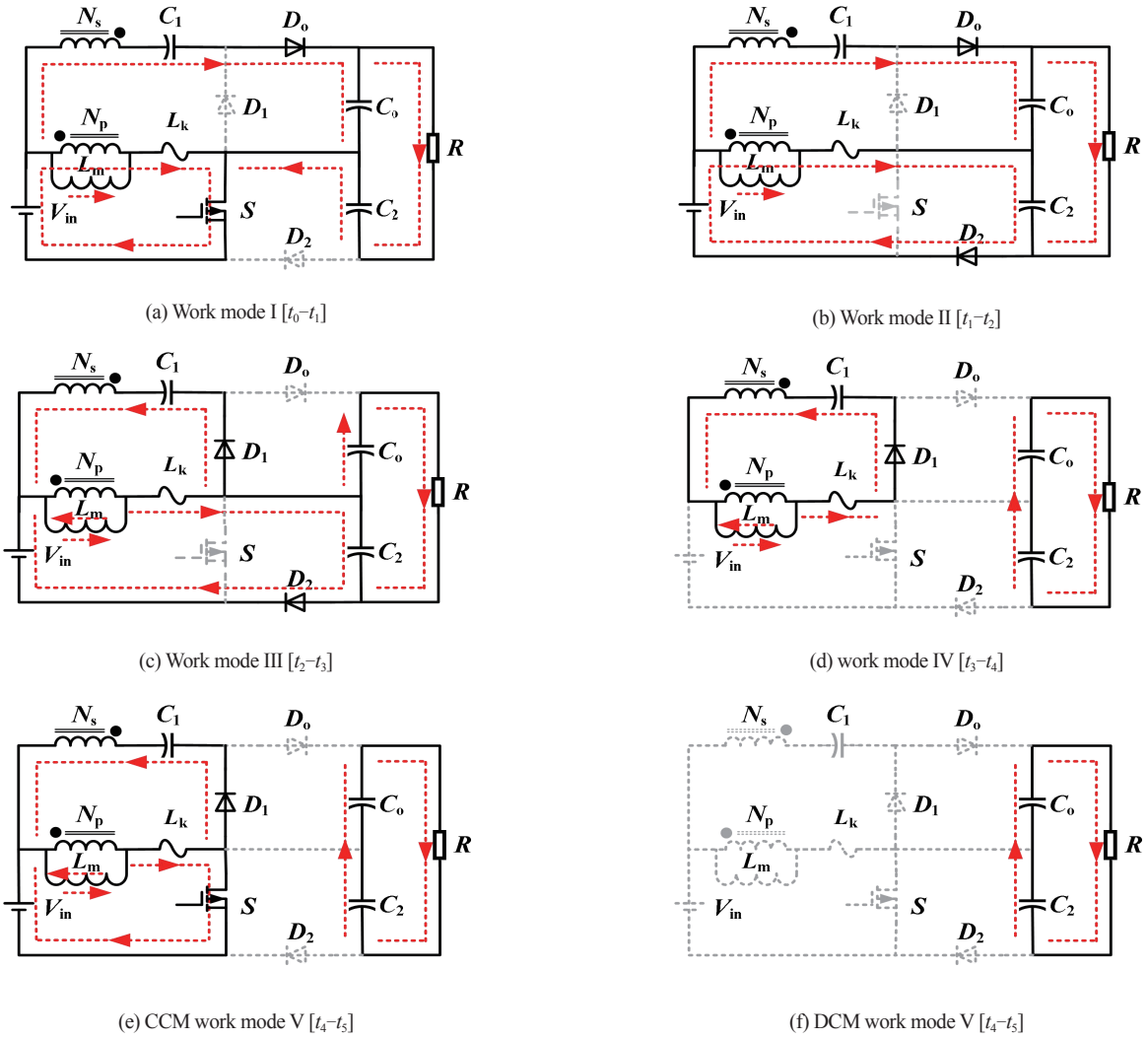


Fig. 3. Equivalent circuit of the improved coupled inductor Boost-Zeta converter.

III. Theoretical Analysis of Converter Topology

The equivalent circuit of the improved coupled inductor Boost-Zeta converter is shown in Fig. 3. According to whether the excitation inductor current I_{Lm} is continuous, it's divided into continuous operation mode (CCM) and discontinuous operation mode (DCM). The working modes and key waveforms of the converter in the two modes are shown in Figs. 4 and 5.



(a) Work mode I [t_0–t_1]

(b) Work mode II [t_1–t_2]

(c) Work mode III [t_2–t_3]

(d) work mode IV [t_3–t_4]

(e) CCM work mode V [t_4–t_5]

(f) DCM work mode V [t_4–t_5]

Fig. 4. Equivalent circuits of the working modes.

A. CCM Working Mode

The converter has 5 working modes in a switching cycle as shown in Fig. 4(a)–(e). The key waveforms for each working mode are shown in Fig. 5(a).

(1) Working mode I [t_0–t_1]: At the moment of t_0, the switch S has been turned on, the diodes D_1 and D_2 are cut-off, and D_0 started to turn on. The excitation inductor L_m and the leakage inductance L_k are charged and store energy, and the current flowing through increases linearly. The power supply, capacitors C_1 and C_2 supply power to the load through D_0, and also charge the coupled inductor N_s terminal and C_0.

(2) Working mode II [t_1–t_2]: At the moment of t_1, S is turned off, D_2 and D_0 are turned on, and D_1 is cut-off. C_2 absorbs the energy of L_k through D_2 and clamps the voltage on the power switch; The current flowing through the N_s terminal of the coupled inductor decreases to 0 at t_2, and D_0 turns off naturally.

(3) Working mode III [t_2–t_3]: At the moment of t_2, S remains off, D_2 is on, and D_0 is cut-off. The coupling inductor charges capacitor C_1 through D_1, and D_1 is turned on; C_2 continues to absorb the energy of the L_k and clamps the voltage across the power switch, and the current i_{Lk} decreases linearly. Since working mode II is a transient transition mode, this mode is the main mode in which C_2 absorbs leakage inductance energy and inhibits switch voltage spikes.

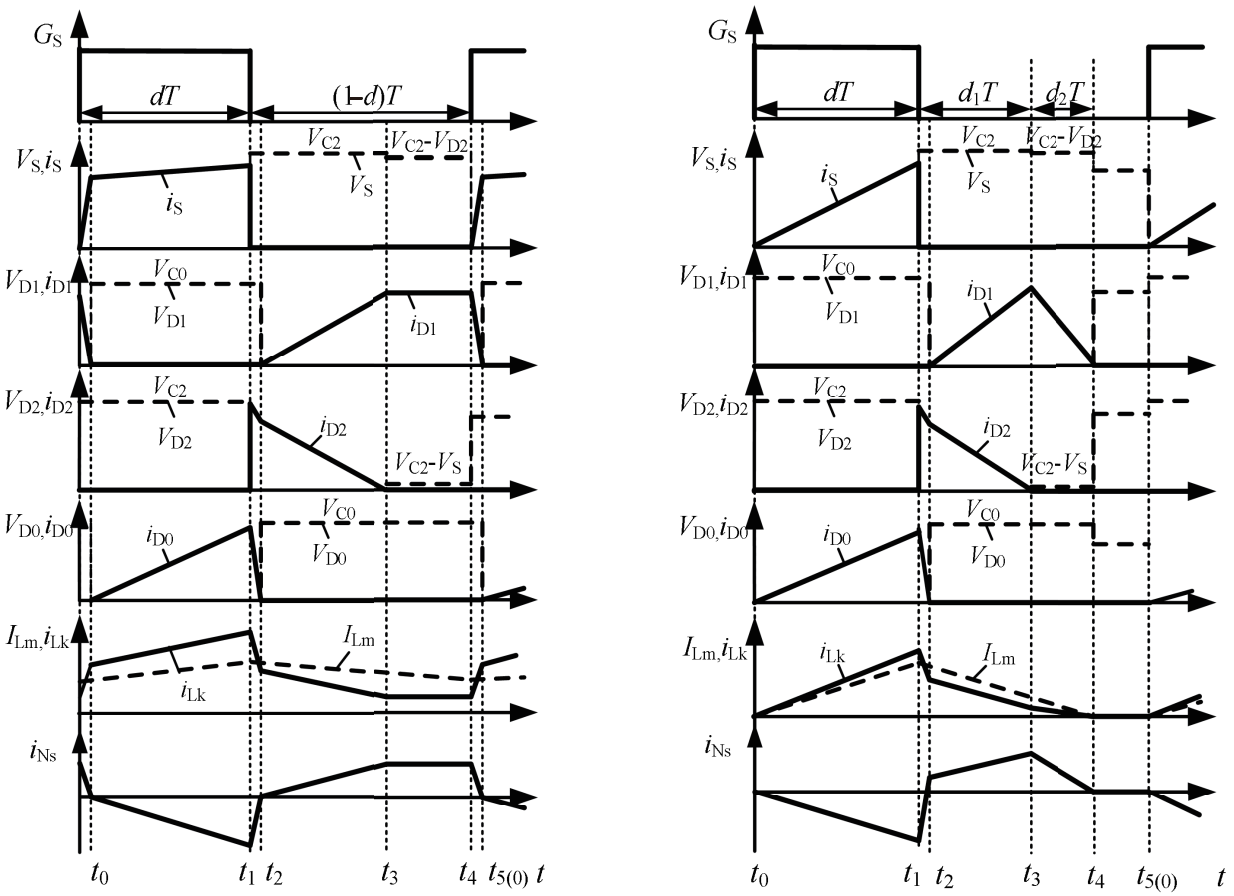
(4) Working mode IV [t_3–t_4]: At the moment of t_3, S and D_0 remain off, D_1 remains on, L_k no longer charges C_2, the current flowing through D_2 drops to 0, and D_2 is naturally turned off. The coupled inductor continues to charge C_1 through the D_1, and the loop current remains essentially unchanged.

(5) Working mode V [t_4–t_5]: At the moment of t_4, S starts to turn on, D_1 remains on, and D_2 and D_0 remain off. L_m and L_k begin to charge and store energy, and i_{Lk} increases rapidly and linearly. The charging current of C_1 decreases rapidly, at the t_5 moment decreases to 0, and D_1 is turned off.

B. DCM Working Mode

When the converter works in DCM mode, there are 5 working modes in one switching cycle, as shown in Fig. 4(a)–(d) and (f), and the key waveforms of each working mode are shown in Fig. 5(b). In DCM mode, the working modes I–III are the same as those in CCM mode, which will not be described here.

Working mode IV [t_3–t_4]: At the moment of t_3, S and D_0 keep



(a) Current continuous mode

(b) Current discontinuous mode

Fig. 5. Simplified key waveform of the converter.

cut-off, D_1 is turned on because the voltage at both ends of switch is slightly lower than the voltage at both ends of C_2, D_2 is cut-off; The coupled inductor continues to charge C_1 through D_1, and the loop current decreases linearly until it drops to 0 at the moment of t_4 and D_1 is turned off with zero current. The load is powered by C_2 and C_0.

Working mode V [t_4–t_5]: In this mode, all power devices in the converter are kept off, the energy exchange process of the coupling inductor and C_1 is temporarily stopped, and the excitation inductor current is interrupted. The load is powered by C_2 and C_0.

IV. Steady-State Performance Analysis

A. Voltage Analysis in CCM Mode

Set the turns ratio of the coupling inductor: $n = N_s/N_p$, and the coupling coefficient $k = L_m/(L_m + L_K)$, so $V_{Lm} = kV_{Np}$.

For convenience of analysis, transient modes II and V are ignored. According to Fig. 4(a), when the converter works in mode I, applying KVL, L_m voltage can be expressed as:

$$\begin{cases} V_{Lm}^{I} = kV_{in} \\ V_{Lm}^{I} = \dfrac{k}{1+n}\left(V_{C0} - V_{C1}\right) \end{cases} \tag{1}$$

According to Fig. 4(c) and (d), when the converter works in modes III and IV, applying KVL, the excitation inductance voltage can be expressed as:

$$\begin{cases} V_{Lm}^{III,\ IV} = k(V_{in} - V_{C2}) \\ V_{Lm}^{III,\ IV} + nV_{Lm}^{III,\ IV} = k(-V_{C1}) \end{cases} \tag{2}$$

According to the volt-sec balance law of L_m, we can get:

$$\int_0^{dT} V_{Lm}^{I}\mathrm{d}t + \int_{dT}^{T} V_{Lm}^{III,\ IV}\mathrm{d}t = 0 \tag{3}$$

By substituting (1) and (2) into (3), the expression of voltage of each capacitor of the converter can be obtained:

$$V_{C1} = \frac{(1+nk)d}{1-d}V_{in} \tag{4}$$

$$V_{C2} = \frac{1}{1-d}V_{in} \tag{5}$$

$$V_{C0} = \frac{1+nk}{1-d}V_{in} \tag{6}$$

From the working mode, the output voltage (V_0) can be expressed by V_{C2} plus V_{C0}, then the voltage gain at steady state (GCCM) can be expressed as:

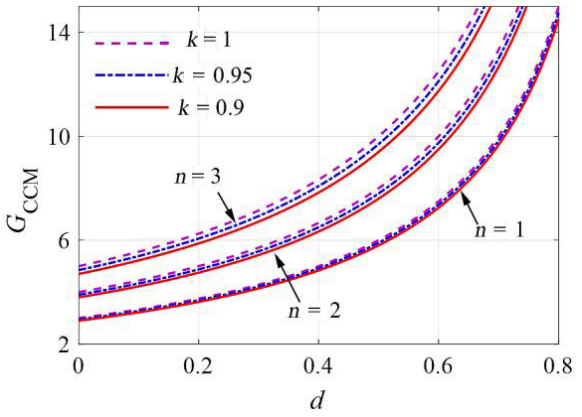


Fig. 6. Relation curves of voltage gain G_{CCM} versus on-duty ratio d in different turns ratio n and coupling coefficient k.

$$G_{CCM}=\frac{V_o}{V_{in}}=\frac{2+nk}{1-d} \tag{7}$$

According to (7), the relationship curves of the voltage gain G_{CCM} of the converter versus the on-duty ratio d in different the turns ratio n and the coupling coefficient k can be obtained, as shown in Fig. 6, from the demand output voltage, the on-duty ratio and the number of turns ratio can be determined. If adopt the coupling inductor with a higher coupling coefficient and less leakage inductance can further improve the output voltage.

When the coupling coefficient k = 1, the voltage stress of each capacitor, diode and power switch can be expressed as:

$$V_{vpsC1}=\frac{(1+n)d}{1-d}V_{in}=\frac{(1+n)d}{2+n}V_o \tag{8}$$

$$V_{vpsC2}=\frac{1}{1-d}V_{in}=\frac{1}{2+n}V_o \tag{9}$$

$$V_{vpsC0}=\frac{1+n}{1-d}V_{in}=\frac{1+n}{2+n}V_o \tag{10}$$

$$V_{vpsD1}=V_{vpsD0}=V_{C0}=\frac{1+n}{2+n}V_o \tag{11}$$

$$V_{vpsD2}=V_{vpsS}=V_{C2}=\frac{1}{2+n}V_o \tag{12}$$

According to the above equations, regardless of the values of d and n, the voltage stress of each capacitor and power device is smaller than V_0 and at a relatively low level.

B. Current Analysis in CCM Mode

Fig. 5(a) shows that the current in each working mode of the converter has a large degree of differentiation, and the current stress of each component and the duration of operating modes III and IV can be obtained by current calculation.

According to Fig. 4(a), when the converter works in mode I, the expression of each capacitor current is as follows:

$$i_{C1}=-i_{D0} \tag{13}$$

$$i_{C2}=-I_o \tag{14}$$

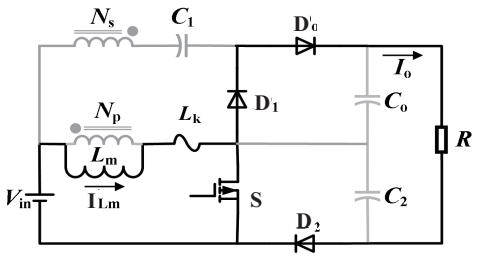


Fig. 7. Average current equivalent circuit of the converter.

$$i_{C0}=-i_{C1}-I_o \tag{15}$$

According to Fig. 4(c), when the converter works in mode III, the expression of each capacitor current is as follows:

$$i_{C1}=\frac{I_{Lm}-i_{D2}}{1+n} \tag{16}$$

$$i_{C2}=i_{D2}-I_o \tag{17}$$

$$i_{C0}=-I_o \tag{18}$$

According to Fig. 4(d),when the converter works in mode IV, the expression of each capacitor current is as follows:

$$i_{C1}=i_{Np}=i_{Ns}=\frac{I_{Lm}}{1+n} \tag{19}$$

$$i_{C2}=i_{C0}=-I_o \tag{20}$$

Set the period ratio of working mode III as d_1, and use ampere-second balance principle for capacitor C_1, as follows:

$$\int_0^{dT} i_{C1}^{I}\mathrm{d}t+\int_{dT}^{(d+d_1)T} i_{C1}^{III}\mathrm{d}t+\int_{(d+d_1)T}^{T} i_{C1}^{IV}\mathrm{d}t=0 \tag{21}$$

Substituting (13), (16) and (19) into (21) gives expressions for d_1 and I_o:

$$d_1=\frac{2(1-d)}{2+n} \tag{22}$$

$$I_o=\frac{1-d}{2+n}I_{Lm} \tag{23}$$

The ampere second balance principle is applied to all capacitors in the circuit, and the average current equivalent circuit of the converter is obtained as shown in Fig. 7.

It can be seen from Fig. 7 that the average value of the current flowing through each diode in a cycle is I_o, and the peak current of the main components in the converter can be obtained by combining (22) and (23).

The current flowing through D_2, D_0, S and coupling inductor reaches its peak value at the moment of t_1, the expression is as follows:

$$i_{cpsS}=\frac{2+(2-d)n}{(1-d)d}I_o \tag{24}$$

$$i_{cpsD2}=\frac{(2+n)}{1-d}I_o \tag{25}$$

$$i_{\text{cpsD0}} = -i_{\text{cpsNs}} = \frac{2}{d} I_{\text{o}} \tag{26}$$

$$i_{\text{cpsNp}} = \frac{(2-d)n + 2d}{(1-d)d} I_{\text{o}} \tag{27}$$

The current flowing through D_1 reaches its peak value at the moment of t_3, expressed as:

$$i_{\text{cpsD1}} = \frac{2+n}{(1+n)(1-d)} I_{\text{o}} \tag{28}$$

In practical application, the voltage gain of the converter is determined according to the demand, when selecting the values of the on-duty ratio d and the number of turns ratio n of the coupled inductor, it is necessary to consider the influence of them on the loss and volume weight of the converter, as well as the period proportion of the working mode III, to ensure the effective suppression of the voltage peak of the power switch. It is also necessary to calculate the voltage and current stress according to d and n values, to select the appropriate components.

C. Current and Voltage Analysis in DCM Mode

Fig. 5(b) shows the key waveform diagrams of the converter in DCM working mode. Here, the period proportion of operating mode III is set to d_1, and the period proportion of operating mode IV is set to d_2. The steady-state voltage and current analysis process of DCM mode is the same as that of CCM mode. The analysis is no longer carried out here. when the coupling coefficient is 1, the expression of each capacitor voltage and the voltage gain of the converter is:

$$V_{C1} = \frac{(1+n)d}{d_1 + d_2} V_{\text{in}} \tag{29}$$

$$V_{C2} = \frac{d + d_1 + d_2}{d_1 + d_2} V_{\text{in}} \tag{30}$$

$$V_{C0} = \frac{(1+n)(d + d_1 + d_2)}{d_1 + d_2} V_{\text{in}} \tag{31}$$

$$G_{\text{DCM}} = \frac{V_{\text{o}}}{V_{\text{in}}} = \frac{(2+n)(d + d_1 + d_2)}{d_1 + d_2} \tag{32}$$

Current peak expressions of diodes, power switch and coupling inductor are:

$$i_{\text{cpsD1}} = \frac{2}{d_1 + d_2} I_{\text{o}} \tag{33}$$

$$i_{\text{cpsD2}} = \frac{2}{d_1} I_{\text{o}} \tag{34}$$

$$i_{\text{cpsD0}} = -i_{\text{cpsNs}} = \frac{2}{d} I_{\text{o}} \tag{35}$$

$$i_{\text{cpsNp}} = \frac{2n(d_1 + d_2) + (n+2)d(d + d_1 + d_2)}{d(d_1 + d_2)} I_{\text{o}} \tag{36}$$

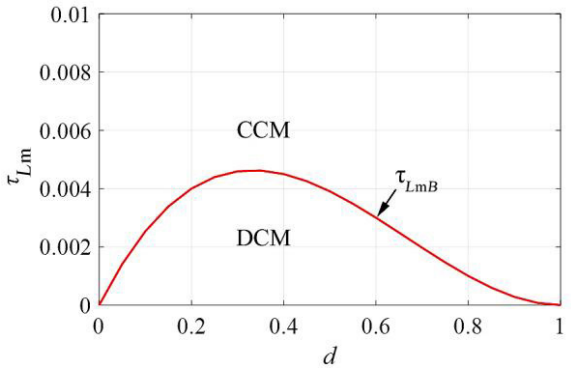


Fig. 8. Relation curve between critical time constant τ_{LmB} and the duty cycle d.

$$i_{\text{cpsS}} = \frac{2(2+n)(d_1 + d_2) + (2+n)d(d + d_1 + d_2)}{d(d_1 + d_2)} I_{\text{o}} \tag{37}$$

It can be seen from the above formulas that the voltage gain and the voltage and current stress of each component in the DCM mode are closely related to the duration of each mode. However, the complexity of calculating the cycle proportion of the operating modes III-V in practice leads to the difficulty in obtaining accurate results from the above formulas, which also requires the converter to often work in CCM mode. When the current break happens exactly at the end of the cycle, the above formula will have the same meaning as in the CCM mode.

D. Current Intermittent Critical Condition

Set the average excitation inductor current to be I_{Lm}, When the current ripple satisfies $\Delta i_{Lm} > 2I_{Lm}$, the converter works in CCM mode; Otherwise, the converter works in DCM mode. When $\Delta i_{Lm} = 2I_{Lm}$, the excitation inductor current is in a critical discontinuous state, and the current ripple can be expressed as:

$$\Delta i_{Lm} = \frac{dTV_{\text{in}}}{L_{\text{m}}} \tag{38}$$

The excitation inductor time constant τ_{Lm} is expressed as:

$$\tau_{Lm} = \frac{L_{\text{m}}}{RT} \tag{39}$$

Combining (38) and (39), and substituting (7) and (23), the critical time constant expression of the excitation inductor is obtained as follows:

$$\tau_{LmB} = \frac{d(1-d)^2}{2(2+n)^2} \tag{40}$$

Set $n = 2$, and from (40) can obtain the relationship between the critical time constant τ_{LmB} of the excitation inductor and the on-duty cycle d, as shown in Fig. 8. When $\tau_{Lm} \geqslant \tau_{LmB}$, the converter operates in CCM mode, and vice versa, the converter operates in DCM mode.

TABLE I
PERFORMANCE PARAMETERS OF EACH CONVERTER

Converter type	Voltage gain $G(V_o/V_{in})$	Power switch voltage stress(V_{vpsS}/V_o)	Number of components used($S/L/C/D$)	Efficiency/%
[16]	$2/(1-d)$	1/2	1/1/3/3	94.76
[18]	$(1+n)/(1-d)$	$1/(1+n)$	1/1/3/3	90.3
[21]	$(1+n+d)/(1-d)$	$1/(1+n+d)$	1/2/6/4	93.5
[22]	$[1+(1+n)d]/(1-d)$	$1/[1+(1+n)d]$	1/2/3/2	93.1
[24]	$(2+n)/(1-d)$	$1/(2+n)$	2/2/4/2	96.9
Type I and II converters (Fig. 2(a) and (b))	$(2+n)/(1-d)$	$1/(2+n)$	1/2/4/3	94.1
The improved converter (Fig. 2(c))	$(2+n)/(1-d)$	$1/(2+n)$	1/1/3/3	94.8
The Boost-Zeta-ECLDC converter (Fig. 12(b))	$(2+n+d)/(1-d)$	$1/(2+n+d)$	1/1/6/4	-
The Boost-ECLDC-Zeta converter (Fig. 12(a))	$(2+n)/(1-2d)$	$1/(2+n)$	1/3/6/4	-
The Boost-Zeta-ECI converter (Fig. 13)	$(2+n+nd)/(1-d)$	$1/(2+n+nd)$	1/2/5/4	-

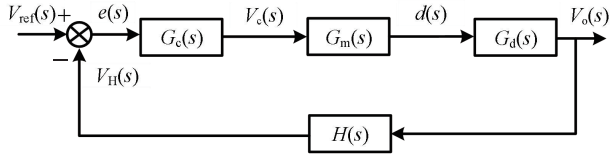


Fig. 9. Block diagram of the control system.

E. System Stability Analysis

In order to analyze the influence of converter parameters on system stability, the state space average method is used to the model of the converter, and the state space expression of the converter is established as follows:

$$\begin{cases} \dot{x} = Ax + Bu \\ y = Cx \end{cases} \tag{41}$$

In (27), the state variable x, u, and the output variable y can be expressed:

$$\begin{cases} x = [i_{Lm} \quad v_{c1} \quad v_{c2} \quad v_{c0}]^T \\ u = [v_{in}] \\ y = [v_o] \end{cases} \tag{42}$$

The state matrix A, input matrix B and output matrix C can be obtained by the working mode of converter.

$$A = \begin{bmatrix} 0 & 0 & \dfrac{-(1-d)}{L_m} & 0 \\ 0 & \dfrac{1}{nL_kC_2} & \dfrac{-(1+n)(1-d)}{nL_kC_1} & \dfrac{-d}{nL_kC_1} \\ \dfrac{1-d}{C_2} & \dfrac{(1+n)(1-d)}{nL_kC_2} & \dfrac{-(1+n)^2(1-d)R-(1-2d)nL_k}{nRL_kC_2} & \dfrac{-(1-2d)}{RC_2} \\ 0 & \dfrac{-d}{nL_kC_0} & \dfrac{1-2d}{RC_0} & \dfrac{dR+(1-2d)nL_k}{nRL_kC_0} \end{bmatrix} \tag{43}$$

$$B = \begin{bmatrix} 0 & 0 & \dfrac{-(1+n)^2}{nL_kC_2} & \dfrac{-(1+n)}{nL_kC_0} \end{bmatrix}^T \tag{44}$$

$$C = [0 \quad 0 \quad 1 \quad 1] \tag{45}$$

Taking Laplace transform for the AC small-signal state equation and output equation of the converter, assuming that the initial value of each state variable is 0, then can get:

$$\begin{cases} \hat{y}(s) = C\hat{x}(s) + [(C_1 - C_2)X]\hat{d}(s) \\ s\hat{x}(s) = A\hat{x}(S) + B\hat{u}(s) + [(A_1 - A_2)X + (B_1 - B_2)U]\hat{d}(s) \end{cases} \tag{46}$$

By further calculation of (46), the input-output transfer function $G_v(s)$ and control-output transfer function $G_d(S)$ of the converter can be obtained:

$$G_v(s) = \left.\frac{\hat{y}(s)}{\hat{v}_{in}(s)}\right|_{\hat{d}(s)=0} = C(sE - A)^{-1}B \tag{47}$$

$$G_d(s) = \left.\frac{y(s)}{d(s)}\right|_{\hat{v}(s)=0} = C(sE-A)^{-1}[(A_1-A_2)X+(B_1-B_2)U]+(C_1-C_2)X \tag{48}$$

Substitute the parameters of Table I into the above formulas:

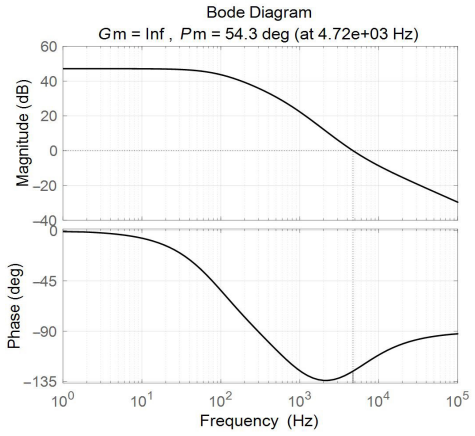
$$G_d(S) = \frac{2.078\times10^4 s + 6.429\times10^8}{S^2 + 5470s + 2.826\times10^6} \tag{49}$$

It can be seen from the transfer function of the small signal model of the converter that the converter is a nonlinear time-varying system, and the single-voltage closed-loop control is carried out to improve the stability and anti-interference ability of the improved converter.

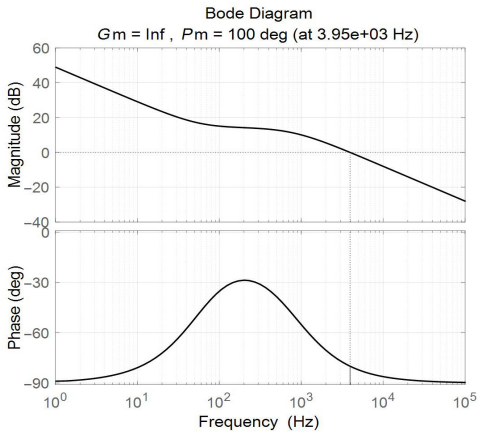
The system block diagram is shown in Fig. 9. In Fig. 9, $V_{ref}(s)$ is the reference voltage, $V_H(s)$ is the feedback voltage, and $e(s)$ is the error signal function. $G_c(s)$ is the controller regulation function, which obtains the error signal function from the previous stage and outputs the modulation signal function $V_c(s)$. The pulse-width modulation function $G_m(s)$ generates different switch turn-on duty cycles $d(s)$ according to $V_c(s)$ and acts on the control output transfer function $G_d(s)$ of the converter to generate a specific output voltage $V_o(s)$.

According to Fig. 9, the open-loop transfer function of the system is expressed as:

$$T(s) = G_c(s)G_m(s)G_d(s)H(s) \tag{50}$$

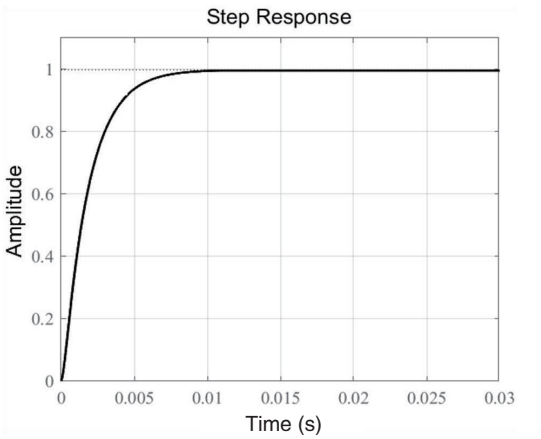


(a)

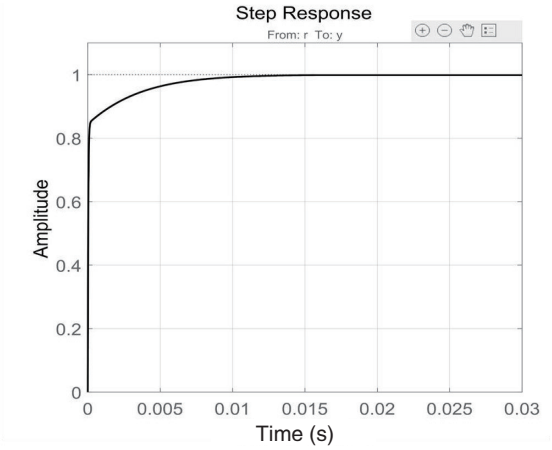


(b)

Fig. 10. (a) Bode diagram for open-loop transfer function. (b) Bode diagram for transfer function of compensation.



(a)



(b)

Fig. 11. (a) Step response curve for open-loop transfer function. (b) Step response curve for transfer function of compensation.

Before adding the compensation link, the $G_c(s)$ does not work, it can be taken as 1. The $G_m(s)$ is taken as the reciprocal of the saw tooth wave, that is, $G_m(s) = 1/V_m(s)$. Combined with (49), the Bode diagram and the step response curve of the open-loop transfer function of the improved converter are shown in Figs. 10(a) and 11(a).

In order to make the system have a better dynamic response, the compensation link G_c(s) is added to the system, and the PID compensation network is used here. The PID compensation network is a transfer function with a single pole and a double zero point, and its expression is:

$$G_c(s) = k\frac{(s+w_{z1})(s+w_{z2})}{s(s+w_p)} \tag{51}$$

With the help of the sisotool toolbox in Matlab, the zero-pole configuration of the open-loop transfer function of the improved converter is performed, and the compensation transfer functions of the converter are:

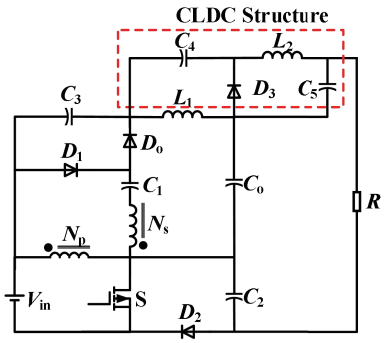
$$G_c(s) = 1.2066\frac{(s+444)^2}{s(s+30512)} \tag{52}$$

After compensation, the Bode diagram and the step response curve are shown in Figs. 10(b) and 11(b). From Fig. 10, The amplitude margin of the before compensation converter is infinite, the phase margin is 54.3°, the same crossing frequency is high, the high-frequency gain is large, and the system is susceptible to high-frequency noise. After compensation, the slope of the system in the low-frequency band increases, the gain becomes higher, and the steady-state accuracy is improved. The traversal frequency is reduced to about 1/10 of the system frequency, which not only ensures the good dynamic response speed of the system but also reduces the high-band gain of the system. From Fig. 11, The response speed of the step response of the system after compensation is faster than that before compensation.

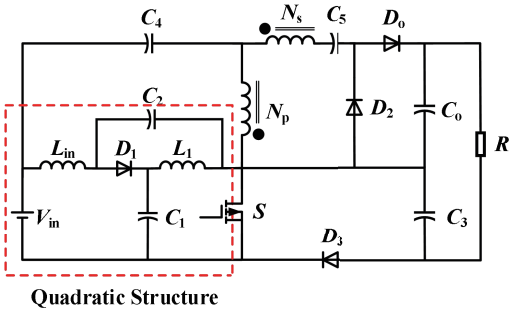
V. Converter Structure Expansion and Comparison

A. Converter Structure Expansion

When the converter needs to work on occasion with higher boost requirements, on the one hand, can adjust the switch-on duty cycle and the coupling inductor turns ratio of the converter to improve the voltage gain, but too high the power switch conduction duty cycle will increase the conduction loss,



(a) Boost-ECLDC-Zeta converter



(b) Boost-Zeta-ECLDC converter

Fig. 12. Two converters after superposition (CLDC) structure.

and too high the turns ratio will also reduce the linearity of the coupled inductor. On the other hand, can expand the structure of the converter. The structural expansion of the converter can be divided into two types: the superposition of the connected limited device configuration (CLDC) structure and the expansion of the coupled inductor multiplication structure.

1) Superposition of CLDC Structure

As shown in Fig. 12, the superposition of CLDC structure can be divided into two methods: one is to superimpose the CLDC structure on the output inductor (L_1) in type I coupled inductor Boost-Zeta converter called Boost-Zeta-ECLDC converter. The other is to superimpose the CLDC structure on the input inductor (L_{in}) in type II coupled inductor Boost-Zeta converter called Boost-ECLDC-Zeta converter, which is equivalent to changing the input side shared by the two sub-converters to a quadratic structure. The analysis of the working modes of the converter will not be repeated here.

2) Expansion of Coupling Inductor Voltage Doubling Structure

As shown in Fig. 13, the Boost-Zeta-ECI converter is formed by replacing the coupled inductor multiplier structure in type I coupled inductor Boost-Zeta converter with the coupling inductor multiplier structure on the right side of Fig. 13. The two coupling inductor multiplier structures on the right side of Fig. 13 use an additional diode and a voltage doubling capacitor, and the two stages of voltage doubling capacitors are alternately charged and discharged under the action of the coupled inductor, and finally, the output voltage is raised.

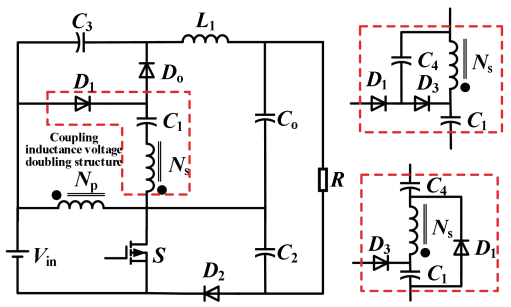


Fig. 13. Boost-Zeta-ECI converter.

B. Comparison of Steady-State Performance of Converters

In order to show the steady-state performance of the converter, the performance parameters of each converter mentioned in this paper are compared with the coupled inductor boost converter mentioned in [18], the coupled inductor Boost-Sepic converter mentioned in [21], the coupled inductor Boost-Zeta converter mentioned in [22], [23] and converter[24]. Table I lists the performance parameters.

The Boost-Zeta-ECLDC converter, the Boost-ECLDC-Zeta converter, and the Boost-Zeta-ECI converter have higher voltage gain than other converters and have lower power switch voltage stress at the same output voltage, but these advantages come at the cost of using more components. So subsequently the improved converter and converters of [18], [21]–[24] are used as the comparison object.

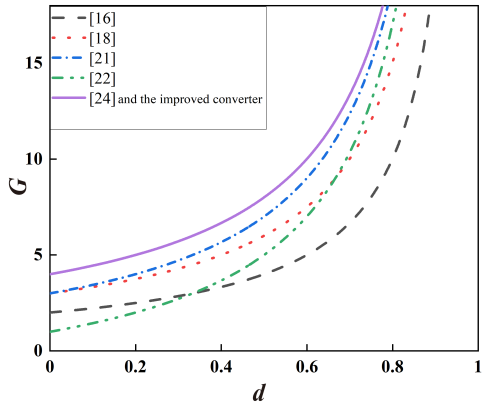
Set n = 2, and the voltage gain curve of each converter is shown in Fig. 14(a). Fig. 14(a) shows the improved converter and converter of [24] have higher voltage gain than others. The voltage stress curve of the switch transistor is shown in Fig. 14(b). Fig. 14(b) shows the improved converter and converter of [24] have lower voltage stress at any duty cycle than other converters. It can be seen from the data in Table II that the efficiency of the improved converter is slightly smaller than the converter of [24], but the improved converter uses fewer components and has a lower cost.

VI. Simulation and Experimentation of Improved Converter

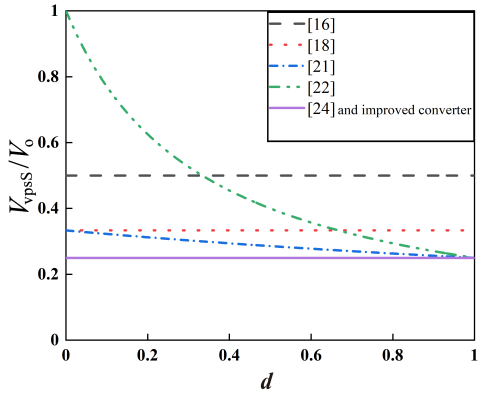
In order to verify the correctness of the theoretical analysis, a closed-loop simulation and experiment were carried out on the improved converter. Control block diagram of the improved converter is shown in Fig. 15. The parameters and component models used are shown in Table II.

A. Simulation Verification

The converter simulation waveforms are shown in Figs. 16–18. Fig. 16 shows the input and output waveforms of the converter. The converter increases the input voltage of 36 V to an output voltage of 220 V, realizing a high-gain conversion of voltage, with an output current of about 0.74 A and an output power of about 160 W. To verify the stability and response speed of the converter. The load sudden change is halved at 0.3 s, and the



(a) Converter voltage gain curve



(b) Voltage stress curve of each power switch

Fig. 14. Comparison curve of each converter.

TABLE II
CONVERTER PARAMETERS AND COMPONENTS

Parameters/Components	Value/Model
Input voltage V_{in}	36 V
Output voltage V_o	220 V
Output power P_o	80–160 W
On-duty ratio of power switch d	0.35
Switching frequency f_s	40 kHZ
Coupling inductor turns ratio n	2
Excitation inductance L_m	220 μH
Voltage doubler capacitors C_1	100 μF
Clamp capacitor C_2 and output capacitor C_0	220 μF
Power switch S	IRF540NPEF
Diode D_1、D_2、D_0	MBR10200CT

input voltage sudden change is reduced from 36 V to 26 V at 0.4 s. Under the sudden change of closed-loop compensation link, the output voltage of the converter is quickly restored to 220 V after small fluctuations, the output current changes according to the load change. In general, the converter can maintain rapid response under the influence of large interference, the output signal is stable and reliable.

Fig. 17 shows the coupling inductor current waveform of the converter, from which it can be seen that the converter works in CCM mode, and the five working modes of the converter are

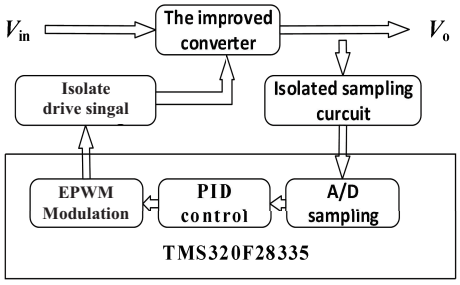


Fig. 15. Control block diagram of the improved converter.

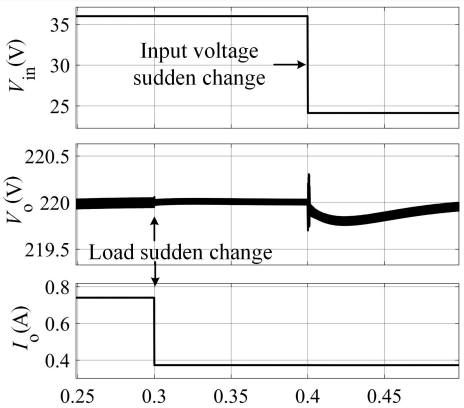


Fig. 16. Input/output voltage/current waveform of converter.

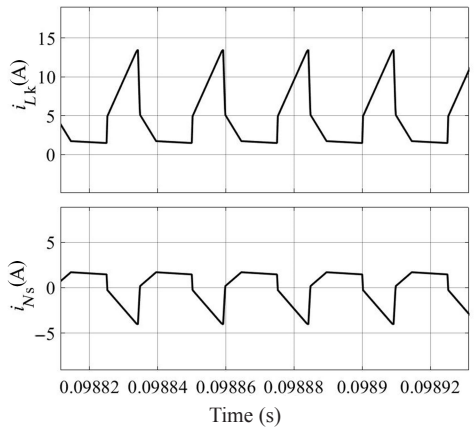
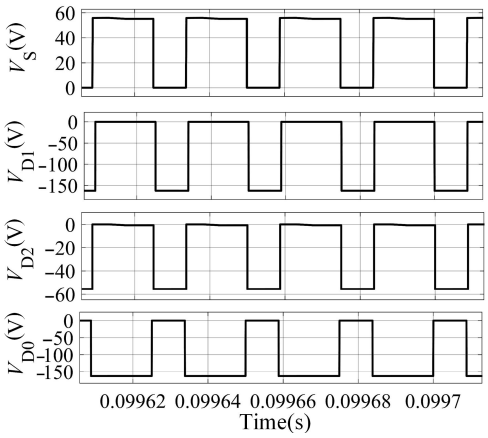


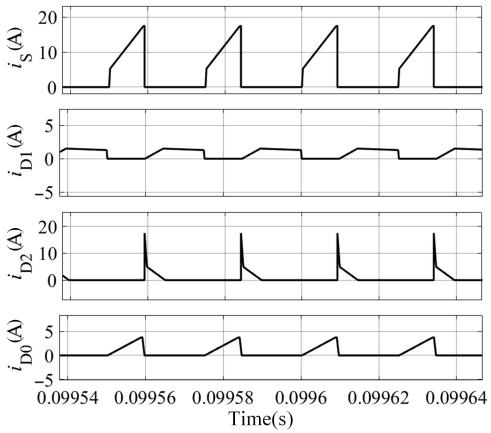
Fig. 17. Coupled inductor current waveform of converter.

clearly distinguished on the waveform, and their change trend and current peak are consistent with the theoretical analysis (the theoretical values of coupled inductor current are: i_{cpsLk} = 13.10 A, i_{cpsNs} = 4.29 A).

Fig. 18 shows the voltage and the current waveforms of the converter switch transistor and each diode. Each voltage and current waveform is consistent with the theoretical analysis, and the voltage and current stress values are the same as the calculated values (the theoretical values of each voltage stress are: V_{vpsS} = V_{vpsD2} = 54.96 V, V_{vpsD1} = V_{vpsD0} = 164.88 V, and the theoretical values of current stress are: i_{cpsS} = 17.39 A, i_{cpsD1} = 1.51 A, i_{cpsD2} = 4.52A, i_{cpsD0} = 4.29 A). From D_1 and D_2 current waveforms can be seen that the working mode III has



(a) Switch and diode voltage waveforms



(b) Switch and diode current waveforms

Fig. 18. The voltage and current waveforms of the converter power switch of each diode.

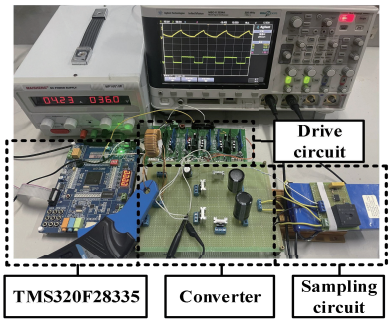
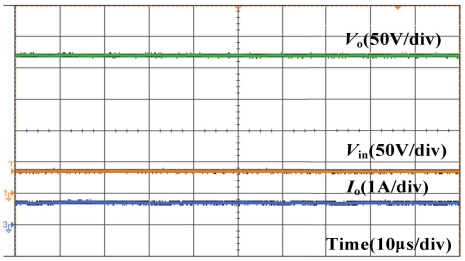
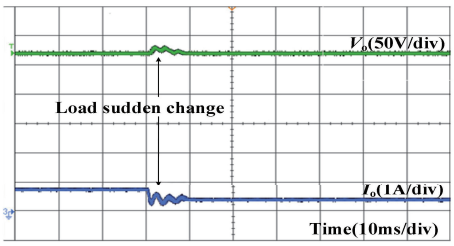


Fig. 19. The experimental prototype.



(a) Steady-state input and output waveforms



(b) Output dynamic waveform when load sudden change

Fig. 20. Input and output waveforms of the improved converter.

a large proportion of cycles to ensure the absorption of leakage inductance energy. The diagram also shows that after the power switch is turned off, the voltage at both ends will not appear spikes. In working modes III and IV, the power switch voltage does not significantly fluctuate and its value can be regarded as the voltage across C_2.

B. Experimental Verification

The experimental prototype of the improved coupled inductor Boost-Zeta converter includes the prototype system includes DC power supply, TMS320F28335 DSP main control circuit, TX-DA962D6 isolation drive circuit, isolated sampling circuit, Hantai CC-65 current probe, oscilloscope and load as shown in Fig. 19. The experimental waveforms of the converter are shown in Figs. 20–22.

The steady-state input and output waveforms of the converter are shown in Fig. 20. According to Fig. 20(a), it can be seen that the converter realizes the high voltage gain conversion from 36 V to 220 V and the output current value is about 0.74 A, which is unified with the calculation and simulation values. Fig. 20(b) shows that the output voltage can be stabilized in a short time when the load suddenly changes, which verifies the timeliness and stability of the converter control system.

The coupled inductor current waveforms of the converter are shown in Fig. 21, and the primary side current waveform shows that the converter operates in CCM mode. Under the influence of leakage inductance and snubber circuit, there are five working modes in the converter. The cycle ratio of working modes I and III is about 0.35 and 0.34 and the current stress value of the coupled inductor is about 13 A and 4.3 A which is consistent with theoretical analysis and simulation.

The voltage and current waveforms of the power switch and diodes of the converter are shown in Fig. 22. According to the voltage waveforms, the voltage stress of the power switch and D_2 is about 55 V, which is much lower than the output voltage of 220 V. The voltage stress of D_1 and D_0 is large but still less than the output voltage. Comparing the on-off time of the switch and the diode, it can be found that when the switch is turned off in working mode II, D_2 is turned on to provide a channel for C_2 to absorb leakage inductance energy. D_2 is turned off with zero current in working mode IV and the voltage across it remains basically 0. The switch voltage does not fluctuate significantly in mode IV. The current stress of the power switch in the current waveform is about 17 A

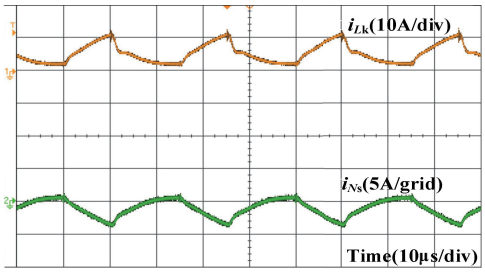


Fig. 21. Coupled inductor current waveform of the improved converter.

and the coupling inductor and leakage inductance limit the current value and the rate of change and reduce the switching loss. The current stress of each diode is less than 5 A. Unlike the simulation waveforms, the current of the power switch and diode has a certain drop time due to the influence of the inductance effect in the actual circuit.

C. Analysis of Power Loss and Efficiency

The diode model used in this article has a reverse recovery time of less than 5 ns and can be ignored for on-off loss. Power loss of the improved converter includes: power switch loss P_S between conduction loss P_{condS}, and on-off loss P_{SWS}, diode conduction loss P_D, inductor power loss P_{LS} and capacitor power loss P_{CS} which can be expressed as:

$$P_{Loss} = P_{condS} + P_{SWS} + P_D + P_{LS} + P_{CS} \tag{53}$$

$$P_{condS} = \frac{1}{T}\int_0^{dT} i_S^2(t) R_{DS(on)} \mathrm{d}t \tag{54}$$

$$P_{SWS} = \frac{1}{T}\left[\int_0^{t_{on}} v_S(t) i_{S(on)}(t)\mathrm{d}t\right] + \frac{1}{T}\left[\int_0^{t_{off}} v_S(t) i_{S(off)}(t)\mathrm{d}t\right] \tag{55}$$

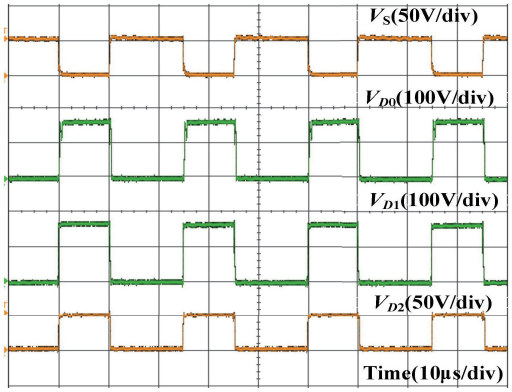
$$P_D = \frac{1}{T}\left[\int_0^{t_d} v_D(t) i_D(t)\mathrm{d}t\right] \tag{56}$$

$$P_{LS} = P_{FE} + P_{CU} = P_L A_e l_e + I_L^2 R_L \tag{57}$$

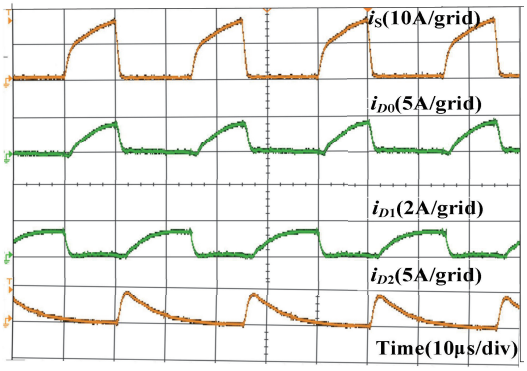
$$P_{CS} = I_C^2 R_{ESR} \tag{58}$$

In the above equation, i_s is the drain current, R_{DS} = 44 mΩ, t_{on} = 46 ns, t_{off} = 74 ns, $V_{D(t)}$ = 0.8 V, P_{FE} is the core loss and P_{CU} is the coil copper loss. Set P_o = 160 W, substitute the converter steady-state time parameters into (53)–(58), the power loss distribution of each element in the converter can be obtained as shown in Fig. 23.

To monitor the efficiency of the converter at different input voltages and power levels. By adjusting the load R and the input voltage, the efficiency of the converter at different power levels can be obtained. As shown in Fig. 24, at 160 W, the efficiency of the 36 V input and 48 V input is 94.8% and 95.5%, respectively. With the increase of 80 W to 160 W, the efficiency gradually increases. As can be also seen from Fig. 24, the efficiency curve at an input voltage of 48 V is higher than that at an input voltage of 36 V. This phenomenon shows the loss of the converter decreases and the efficiency increases as the input voltage rises. Efficiency can be further improved by using devices with smaller parasitic parameters and better performance.



(a) The voltage waveforms of switch S and diode D_0, D_1, D_2.



(b) The current waveforms of switch S and diode D_0, D_1, D_2.

Fig. 22. The waveforms of power switch and diodes of the improved converter.

VII. Conclusion

In this paper, a class of Boost-Zeta converters based on coupled inductor is proposed and the derivation process of the converter structure is introduced. The working principle and steady-state performance of the improved converter are analyzed in detail and compared with other coupled inductor combination converters. The results show that the converter proposed in this paper has the following characteristics:

1) Using the combined structure and coupled inductor voltage doubling structure, a higher voltage gain and more flexible adjustment can be obtained.

2) Not only can expand the structure to make the converter used in higher output voltage requirements but also improve topology to reduce the number of components used and the voltage stress of the components, and the efficiency and reliability of the converter are also improved.

3) There is a clamp circuit shared with the converter structure which can effectively absorb leakage inductance energy, this will suppress the voltage spike of the power switch, reduce the loss of the system, and help improve the power level and efficiency of the converter.

References

[1] Z. G. Shao and W. D. Huang,"A calculation method of harmonic prop-

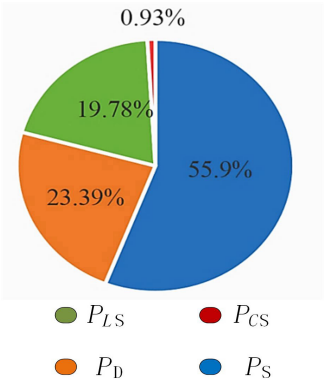


Fig. 23. Power loss distribution.

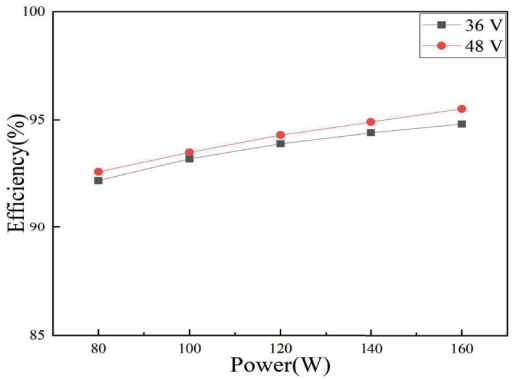


Fig. 24. Measured efficiency curve of the improved converter.

agation considering the uncertainty of distributed generation," in *Transactions of China Electrotechnical Society*, vol. 34, no. S2, pp. 674–683, 2019.

[2] S. H. Gan, J. Y. Wang, J. X. Chu, G. U. Wei, and Y. Q. Sun,"Z-source electrical propulsion system with high voltage boost ability for fuel cell boat," in *Electric Machines and Control*, vol. 22, no. 10, pp. 112–120, 2018.

[3] J. Ding, S. Gao, S. W. Zhao, et al,"A high step-up DC-DC converter with interleaved and coupled inductor based on topology combination," in *Proceedings of the CSEE*, vol. 41, no. 5, pp. 1860–1871, 2021.

[4] B. X. Zhu, S. Liu, Y. H. Huang, and Q. Zeng,"A high step-up DC-DC converter based on high degrees of freedom voltage multiplier cell," in *Proceedings of the CSEE*, vol. 38, no. 9, pp. 2707–2716, 2840, 2018.

[5] A. M. S. S. Andrade, H. L. Hey, L. Schuch, and M. L. D. S. Martins, "Comparative evaluation of single switch high voltage step-up topologies based on Boost and zeta PWM cells," in *IEEE Transactions on Industrial Electronics*, vol. 65, no. 3, pp. 2322–2334, 2018.

[6] Feng Miaomiao,"Pivotal technology research of high step-up DC/DC converter," Shanghai University of Electric Power, Shanghai, China, 2017.

[7] L. W. Zhou, B. X. Zhu, Q. M. Luo, and S. Chen,"Interleaved non-isolated high step-up DC/DC converter based on the diode-capacitor multiplier," in *IET Power Electronics*, vol. 7, no. 2, pp. 390–397, 2014.

[8] J. F. Huang and S. L. Liu,"Application of limitation control to the DC-DC converter," in *Electric Machines and Control*, vol. 19, no. 6, pp. 69–75, 2015.

[9] Y. Ai,"Research on key performance of novel interleaved parallel high-gain DC/DC converter," in *CPSS Transactions on Power Electronics and Applications*, vol. 5, no. 4, pp. 364–371, 2020.

[10] S. Z. Lu, L. Wu S. Q. Li, et al,"Zero voltage switching N-type interleaved three-level bidirectional DC-DC converter," in *Transactions of China Electrotechnical Society*, vol. 35, no. S2, pp. 461–469, 493, 2020.

[11] F. S. Tian, Y. D. Zeng, J. L. Tan, and H. J. Yang,"Research on a novel high gain DC/DC boost converter," in *Power Electronics*, vol. 53, no.12, pp. 1–3, 2019.

[12] M. Pandit, R. Kumari, and K. S. Sherpa,"A comprehensive study on evolution and advancement of DC/DC cascaded converters: a review," in *Australian Journal of Electrical and Electronics Engineering*, vol. 19, no. 1, pp. 40–55, 2022.

[13] H. Gholizadeh, R. S. Shahrivar, M. R. Hashemi, E. Afjei, and S. A. Gorji,"Design and implementation a single-switch step-up DC-DC converter based on cascaded boost and Luo converters," in *Energies*, vol. 14, no.12, pp. 1–18, 2021.

[14] S. M. Fardahar and M. Sabahi,"New expandable switched-capacitor/switched-inductor high-voltage conversion ratio bidirectional DC-DC converter," in *IEEE Transactions on Power Electronics*, vol. 35, no. 3, pp. 2480–2487, 2020.

[15] M. J. Liu, Y. F. Chen, B. Zhang, et al,"High-gian DC/DC cconverter with hybrid switched-inductor and switched-capacitor cell," in *Journal of Power Supply*, vol. 18, no. 4, pp. 85–93, 2020.

[16] Z. H. Yu, X. F. Hu, Z. J. Xu, et al,"Single switch high gain low voltage stress DC converter," in *Electrical Engineering*, vol. 23, no. 7, p. 8, 2022.

[17] Z. Li, W. Qian, and X. Zhang,"An optimized zero-voltage zero-current transition Boost converter realized by coupled inductor," in *IEEE Transactions on Power Electronics*,vol. 34, no. 9, pp. 8882–8893, 2018.

[18] K. Wu and T. Qian,"A cascaded high step-up DC-DC converter with three-winding coupled inductor," in *Transactions of China Electrotechnical Society*, vol. 32, no. 20, pp. 124–132, 2017.

[19] J. F. Huang, F. Xie, and Q. M. Luo,"High step-up improved low voltage-stress Boost converter with coupled inductors," in *Electric Machines and Control*, vol. 24, no. 10, pp. 69–76, 2020.

[20] D. S. Rong and X. J. Sun,"High gain coupled inductance combination buck-boost-Zeta converter," in *Proceedings of the CSEE*, vol. 40, no. 14, pp. 4590–4601,4734,4738, 2020.

[21] A. M. S. S. Andrade, J. C. Giacomini, C. Rech, L. Schuch, and M. L. D. S. Martins,"Boost-zeta high step-up PV module integrated converter," in *Proceedings of 2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Montreal, Canada, 2015, pp. 1046–1053.

[22] R. Guo, L. Z. Zhang, D. Han, et al,"High-gain boost-sepic DC-DC converter with coupled inductors," in *Journal of Power Supply*, vol. 10, no. 3, pp. 80–88, 2022.

[23] A. M. S. S. Andrade, L. Schuch, H. L. Hey, and M. L. D. S. Martins,"A new high voltage step-up gain non-isolated DC/DC Boost-2Zeta converter," in *Proceedings of 2015 IEEE 13th Brazilian Power Electronics Conference and 1st Southern Power Electronics Conference*, Fortaleza, Brazil, 2015, pp. 1–6.

[24] X. Sun, D. S. Ron, and N. Wang,"High gain coupled inductor combination with resonant soft switching Boost-Zeta converter," in *Transactions of China Electrotechnical Society*, pp. 1–13, 2021.

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