A Step-Up Multilevel Inverter Based on Switched Capacitor Technique With Reduced Components

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***Abstract*—This article introduces an innovative single-source-based 19-level switched capacitor multilevel inverter (SCMLI) and its generalized structure. Unlike other SCMLIs, this proposed SCMLI eliminates the need for an H-bridge circuit for polarity generation, thereby reducing the inverter's total standing voltage (TSV). The article provides a circuit description of the proposed inverter, its operating principle, and the modulation strategy employed. Furthermore, the article outlines an optimal capacitor selection method and conducts various power loss analyses for the 19-level proposed SCMLI. A detailed comparative study with similar SCMLIs shows that the proposed SCMLI achieves higher output voltage levels while utilizing fewer components such as switches, drivers, diodes and capacitors. Furthermore, it offers a more cost-effective function per output voltage level than recently reported similar SCMLIs. An extensive experimental study has been conducted on a prototype of the 19-level SCMLI to validate its performance.**

***Index Terms*—Multilevel inverter, reduced components, switched capacitor, total harmonic distortion, voltage boosting factor.**

I. Introduction

MULTILEVEL inverters (MLIs) are increasingly being used in a wide range of industrial applications today. These applications include distributed generation systems, motor drive applications, FACTS applications, induction heating systems, UPS systems, etc [1]–[4]. This is due to their unique features, such as the ability to generate output voltage waveforms with better harmonic spectra, higher power handling capability, the ability to withstand lower electromagnetic interfaces (EMIs), and the capacity to operate at higher efficiency over classic two-level inverters [5].

Traditional MLIs, including cascaded H-bridge MLI (CHB-MLI), flying capacitor MLI (FC-MLI), and neutral point clamped MLI (NPC-MLI), are widely used in various industrial applications but face challenges in generating higher-level output voltage waveforms due to the numerous components involved. This abundance of components leads to increased system size, cost, and complexity. For example, NPC-MLI relies on clamping diodes and DC link capacitors, FC-MLI requires multiple capacitors, and CHB-MLI necessitates independent DC power sources. Both FC and NPC MLIs also suffer from capacitor voltage unbalancing issues [6].

Moreover, conventional MLIs lack inherent output voltage boosting capabilities, which are advantageous for raising the output voltage of low-magnitude renewable sources like photovoltaic systems to match standard load or grid-end voltage levels. Achieving the desired output voltage typically requires the inclusion of a back-end transformer or a front-end DC-to-DC converter. This additional component further increases the size, cost, and complexity of the conversion system [7], [8].

In recent years, significant research has focused on advancing the topology of MLIs and addressing capacitor voltage imbalances. Some studies have proposed reduced device count (RDC) MLIs to minimize component count [9], [10]. However, RDC MLIs lack the ability to boost output voltage. Complex control strategies and additional circuits have been developed to manage capacitor voltage imbalances in NPC-MLI and FC-MLI, resulting in increased costs, larger system size, and complexity [11], [12].

The modular multilevel converter (MMC) stands out as a widely adopted power converter in contemporary applications. It offers a superior and more competitive solution compared to traditional two-level voltage source converters, particularly in high voltage direct-current transmission systems. The MMC, distinguished from other multilevel topologies, offers seamless scalability and achieves near sinusoidal output voltage synthesis through the utilization of cascaded modules comprised of semiconductor switches and floating capacitors. The asymmetric MMCs employ modules featuring asymmetric capacitor voltages to achieve elevated voltage levels with a diminished number of switching devices [13]–[15]. Nevertheless, the MMC lacks inherent capabilities for output voltage boosting and self-balancing of capacitor voltages. To address these limitations, auxiliary circuits or intricate control algorithms are necessitated for maintaining the desired voltages across the floating capacitors. The integration of such auxiliary circuits or complex control algorithms contributes to increased size, cost, and overall complexity of the converter structure.

A distinct category of MLIs, known as switched capacitor MLIs (SCMLIs), has emerged. SCMLIs can generate boosted output voltage using capacitors while requiring fewer power supplies. Furthermore, SCMLIs eliminate the need for intricate control algorithms or auxiliary circuitry to maintain capacitor

Manuscript received April 18, 2023; revised October 2, 2023 and November 18, 2023; accepted December 18, 2023. Date of publication June 30, 2024; date of current version January 2, 2024. No funding was received to assist with the preparation of this manuscript. *(Corresponding author: Tapas Roy.)*

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Digital Object Identifier 10.24295/CPSSTPEA.2023.00053

voltage balance [16], [17]. Recent literature reports numerous creative SCMLIs classified into single source-based and multiple source-based types. Among single source-based SCMLIs, two categories exist: extendable and non-extendable. Notably, the past few years have seen the emergence of pioneering single source-based extendable SCMLIs [18]–[28]. [18] introduces an innovative single-source-based extendable SCMLI consisting of a fundamental SC unit with three switches and one capacitor. Multiple such units interconnect in a cascaded manner to achieve higher output voltage levels. However, this approach necessitates a significant number of switches and driver circuits, thereby increasing the inverter's cost and complexity. Moreover, the inverter relies on an H-bridge circuit to generate both load voltage polarities, leading to an increase in the total standing voltage (TSV) and the maximum switch voltage stress (MSV) rating of the inverter.

In [19], a novel SC cell was introduced, featuring two switches, one diode, and one capacitor. These cells are sequentially linked to construct a generalized cell, forming the basis of a single source-based extendable SCMLI along with an H-bridge circuit. The H-bridge circuit used in this structure enhances the inverter's TSV and MSV. Furthermore, achieving a high-quality output voltage waveform in the inverter requires several switches, drivers, diodes, and capacitors, resulting in increased inverter's cost and complexity. Similarly, in [20], a novel SC cell is proposed, requiring only one switch, two diodes, and one capacitor. Several of these cells are cascaded to form the generalized cell. However, the construction of a single source-based extendable SCMLI necessitates an H-bridge circuit at the load end, which also enhances the inverter's TSV and MSV. In [21], a step-up switched capacitor converter (SCC) is proposed, forming the basis of a single source-based extendable SCMLI along with an H-bridge circuit. Notably, the capacitors in this structure can be charged in a binary asymmetrical pattern, enhancing the inverter's boosting factors and output voltage levels. Nevertheless, this structure is susceptible to higher switch voltage stress and TSV. Similarly, a single source-based SCC with reduced components has been proposed in [22]. However, the converter requires an H-bridge circuit for generating both voltage polarities at the load end. This H-bridge requirement enhances the MSV and TSV of the structure. Furthermore, as the output voltage level enhances, the structure suffers from high switch voltage stress for some of the switches in the SCC circuit.

In recent years, innovative single source-based extendable SCMLIs have emerged, eliminating the need for an H-bridge circuit. An innovative H-bridge-free single source-based extendable SCMLI was proposed in [23], offering reduced MSV and TSV compared to similar structures. However, achieving higher output voltage levels still requires numerous switching devices, driver circuits, and capacitors. Despite its favorable TSV and MSV characteristics, the elevated component count limits its suitability for achieving higher voltage levels. [24] introduces a novel single source-based extendable SCMLI configuration, distinct from the traditional use of an H-bridge circuit. This structure employs a unique binary asymmetrical capacitor charging technique, resulting in an increased boosting factor. This enables the generation of higher output voltage levels while reducing the need for additional switching devices. However, it's essential to note that certain switches in this innovative structure experience elevated voltage stress due to the enhanced output voltage levels and boost factors.

Fig. 1 illustrates recently proposed single source-based extendable SCMLIs without H-bridge circuits. [25] presents an innovative H-bridge-free single source-based extendable SCMLI as shown in Fig. 1(a). This structure charges two series-connected capacitors (C_{a1} and C_{b1}) simultaneously, each reaching half of the source voltage. Consequently, the structure can attain more output voltage levels with smaller voltage steps by integrating additional SC cells, as depicted in Fig. 1(a). However, this results in a limited boosting factor due to the smaller voltage steps. Moreover, to achieve higher output voltage levels, the inverter requires multiple capacitors and diodes, significantly increasing the component cost per level per boosting factor. In [26], an innovative single source-based extendable SCMLI structure is proposed without utilizing an H-bridge circuit as depicted in Fig. 1(b). The capacitors in this design can be charged to the supply voltage level, reducing the inverter's TSV and MSV. Nonetheless, achieving higher output voltage levels still requires multiple unidirectional and bidirectional switches, driver circuits, and capacitors, contributing to increased complexity and cost.

[27] introduced an innovative single-source-based SCMLI without an H-bridge circuit as shown in Fig. 1(c), inspired by the Marx inverter. This structure achieves higher output voltages while reducing MSV and TSV. However, it cannot add the supply voltage to all the capacitor voltages. Furthermore, some capacitors (such as C_{b1} and C_{b2}) in this structure have a passive role, enhancing the boosting factor by energizing other capacitors. Achieving high-quality voltage waveforms requires a substantial number of switches, driver circuits, diodes, and capacitors. Furthermore, a novel SCMLI was proposed in [28], depicted in Fig. 1(d). This variant eliminates the need for an H-bridge configuration and achieves even higher voltage levels while minimizing switch voltage stress and TSV. Nonetheless, it still requires a significant quantity of switching elements, driver circuits, and capacitors to realize enhanced voltage levels.

In summary, the key challenges in single source-based extendable SCMLIs include the need for larger components to achieve higher output voltage levels, high MSV and TSV in H-bridge circuit-based SCMLIs, and limitations in boosting output. This article introduces an innovative single source-based extendable SCMLI configuration that eliminates the need for an H-bridge circuit at the load end. This structure charges capacitors in a trinary asymmetrical pattern, enabling higher output voltage levels and a greater boosting factor with fewer components. This reduced component count results in a cost-effective, highly efficient, compact, and lightweight structure compared to similar structures.

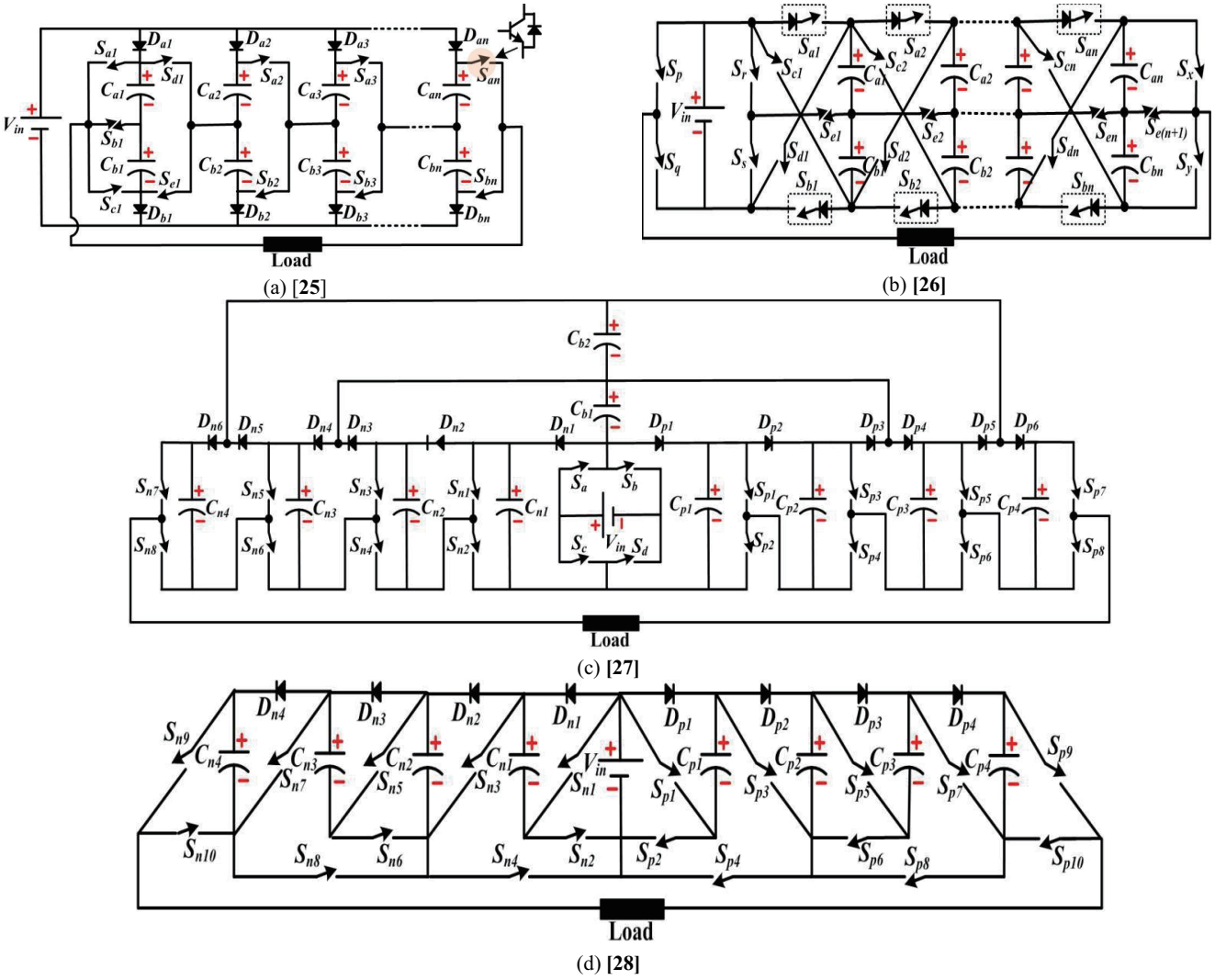


Fig. 1. Recently proposed various single source based SCMLI structures.

The article is structured as follows: Section I presents the introduction, while Section II delves into the 19-level proposed SCMLI. Moving on to Section III, the generalized proposed SCMLI is discussed comprehensively. The modulation strategy for the proposed SCMLI is described in Section IV. Section V elucidates the optimal procedure for selecting capacitors. Section VI describes the power losses analysis of the proposed SCMLI. The inrush current analysis of the proposed SCMLI is presented in Section VII. A comparative analysis between the proposed SCMLI and alternative configurations is outlined in Section VIII. Section IX presents the experimental findings of the 19-level proposed SCMLI. Lastly, the conclusions and references are presented.

II. Proposed 19-Level SCMLI Stucture

A. Circuit Description

Fig. 2 illustrates the proposed 19-level single-source SCMLI, consisting of two capacitor legs (CL#1 and CL#2), twelve switches, and four series-connected diodes. Each capacitor leg comprises three series-connected capacitors: CL#1 includes ca-

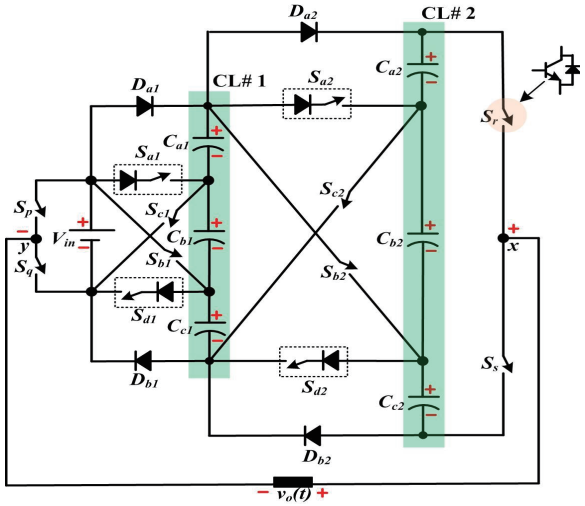


Fig. 2. Proposed 19-level SCMLI.

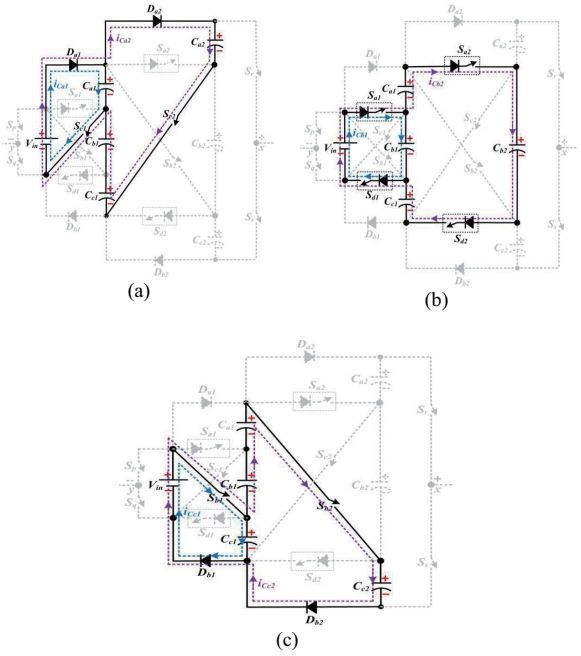


Fig. 3. Figure presents the equivalent circuit for simulataneous charging of (a) C_{a1} and C_{a2}, (b) C_{b1} and C_{b2}, and (c) C_{c1} and C_{c2}.

pacitors C_{a1}, C_{b1}, and C_{c1}, while CL#2 includes capacitors C_{a2}, C_{b2}, and C_{c2}. The switches associated with CL#1 are S_{a1}, S_{b1}, S_{c1}, and S_{d1}, while CL#2 features S_{a2}, S_{b2}, S_{c2}, and S_{d2}, as shown in Fig. 2. The switches S_{b1}, S_{c1}, S_{b2}, and S_{c2} exhibit MOSFET-like characteristics, enabling conduction in both directions while inhibiting voltage in a singular direction. Conversely, switches S_{a1}, S_{d1}, S_{a2}, and S_{d2} lack antiparallel diodes, facilitating current flow in a single direction and impeding voltage in both directions. The realization of these switches involves incorporating a diode in series with a control switch MOSFET, as illustrated in Fig. 2. Additionally, individual series diodes D_{a1} and D_{b1} are connected to CL#1, and D_{a2} and D_{b2} are connected to CL#2. A DC power source, V_{in} (e.g., a battery, PV panel, or fuel cell), supplies energy to the inverter. One leg with switches S_p and S_q is connected to V_{in}, while the other leg has switches S_r and S_s connected to CL#2. The load is connected between the midpoints of these legs, labeled as *x* and *y* in Fig. 2.

B. Capacitor Charging Process

Simultaneous charging of capacitors in CL#1 and CL#2 is a key feature in the proposed SCMLI. Fig. 3 shows the switching states for this simultaneous charging. In Fig. 3(a), when switches S_{c1} and S_{c2} are activated together, C_{a1} connects to V_{in} via diode D_{a1}, and C_{a2} connects to CL#1 via diode D_{a2}. Consequently, C_{a1} charges to approximately V_{in}, while C_{a2} charges to around $3V_{in}$ by drawing energy from V_{in}, C_{b1}, and C_{c1}.

Similarly, the simultaneous charging of C_{b1} and C_{b2} happens when switches S_{a1}, S_{d1}, S_{a2}, and S_{d2} are engaged simultaneously, as seen in Fig. 3(b). Fig. 3(c) illustrates the current flow during C_{c1} and C_{c2}'s simultaneous charging. By employing a similar approach, it's possible to achieve simultaneous charging for pairs like (C_{a1}, C_{b2}), (C_{a1}, C_{c2}), (C_{b1}, C_{a2}), (C_{b1}, C_{c2}), (C_{c1}, C_{a2}), and (C_{c1}, C_{b2}) within the SCMLI configuration. This diverse simultaneous charging strategy allows each capacitor in CL#1 to be charged to V_{in}, while capacitors in CL#2 can be charged to $3V_{in}$.

C. Operating Principle

The proposed SCMLI can realize 19 output voltage levels with a peak magnitude of $9V_{in}$. The switching states with the capacitor states for various voltage levels are shown in Table I. Where '1' and '0' stand for the ON and OFF state of a switch, 'R' and 'F' stand for the reverse and forward bias of a series-connected diode, and 'C', 'N' and 'D' stands for the charging, not-connected and discharging state of a switched capacitor. Furthermore, Fig. 4 depicts the equivalent circuit and current flow paths for realizing the various voltage levels. The line in dotted red color presents the positive load current path whereas the lines in dotted sky-blue and dotted violet present the capacitor charging paths. Some of the voltage level generations are explained in detail.

Fig. 4(a) shows the equivalent circuit whenever the output voltage is $+1V_{in}$. When the switches S_q, S_{c1}, S_{c2}, and S_r conduct, diodes D_{a1} and D_{a2} become forward-biased. Hence, C_{a1} becomes parallel to V_{in} and C_{a2} becomes parallel to CL#1. So, C_{a1} stores energy from the source and charges to near V_{in} whereas C_{a2} charges by CL#1 and rises its voltage to near $3V_{in}$. Further, with this switching state, V_{in} appears across the load terminals resulting in the load voltage becoming V_{in}. During this switching state, the capacitors C_{b1}, and C_{c1} of CL#1 are in discharging state.

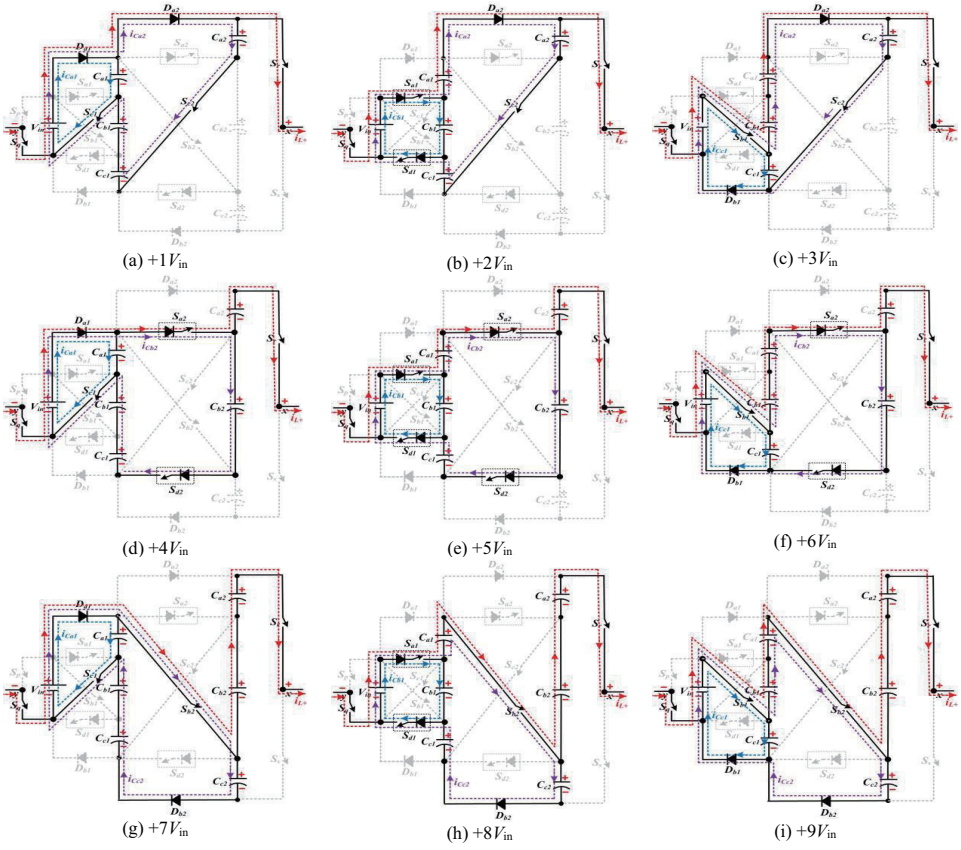
Fig. 4(e) shows the equivalent circuit when the load voltage is $+5V_{in}$. When the switches S_q, S_{a1}, S_{d1}, S_{a2}, S_{d2}, and S_r conduct, connecting C_{b1} in parallel with supply voltage V_{in} and C_{b2} in parallel with CL#1. Furthermore, C_{a2}, C_{a1}, and V_{in} are linked in series and come across the load terminals. As C_{a1} and C_{a2} are previously charged to V_{in} and $3V_{in}$ respectively, the load voltage becomes $+5V_{in}$. In this circuit state, C_{b1} stores energy from V_{in} and rises its voltage to near V_{in}. Similarly, C_{b2} stores its energy from CL#1 and rises its voltage to $3V_{in}$. During this voltage level, C_{a1}, C_{c1}, and C_{a2} are in discharging state as tabulated in Table I.

The generation of the $+6V_{in}$ voltage level at load is presented in Fig. 4(f). According to this figure, C_{a2}, C_{a1}, C_{b1}, and V_{in} are linked in series and come across the load terminal whenever the switches S_q, S_{b1}, S_{a2}, and S_r are turned ON. As C_{a2}, C_{a1} and C_{b1} are charged to $3V_{in}$, V_{in}, and V_{in} respectively, the load voltage becomes $+6V_{in}$. Furthermore, C_{c1} enters into a charging state through the diode D_{b1} and rises its voltage to V_{in}. Also, C_{b2} is in a charging state whenever S_{d2} conducts. The realization of $+9V_{in}$ voltage level at load is presented in Fig. 4(i). As per this figure, C_{a2}, C_{b2}, C_{a1}, C_{b1}, and V_{in} are linked in series and come across the load terminals whenever S_q, S_{b1}, S_{b2}, and S_r are turned ON. As C_{a2}, C_{b2}, C_{a1}, and C_{b1} are previously charged to $3V_{in}$, $3V_{in}$, V_{in}, and V_{in} voltage levels, the load voltage becomes $+9V_{in}$. Furthermore, C_{c1} and C_{c2} enter into a charging state through D_{b1} and D_{b2} respectively, as shown in Fig. 4(i). Hence, C_{c1} rises its voltage to

TABLE I
SWITCH AND CAPACITOR STATES FOR 19-LEVEL PROPOSED-TYPE SCMLI

S/D/C*	Output voltage level (×V_{in})																			
	+9	+8	+7	+6	+5	+4	+3	+2	+1	+0	0	−1	−2	−3	−4	−5	−6	−7	−8	−9
Switch state																				
S_p	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1	1
S_q	1	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0
S_{a1}	0	1	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0	0	1	0
S_{b1}	1	0	0	1	1	0	1	0	0	0	1	1	0	0	1	0	0	1	0	0
S_{c1}	0	0	1	0	0	1	0	0	1	1	0	0	0	1	0	0	1	0	0	1
S_{d1}	0	1	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0	0	1	0
S_{a2}	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0	0	0
S_{b2}	1	1	1	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0
S_{c2}	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	1	1	1
S_{d2}	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0	0	0
S_r	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
S_s	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
Diode state																				
D_{a1}	R	R	F	R	R	F	R	R	F	F	R	R	R	F	R	R	F	R	R	F
D_{b1}	F	R	R	F	R	R	F	R	R	R	F	F	R	R	F	R	R	F	R	R
D_{a2}	R	R	R	R	R	R	F	F	F	F	R	R	R	R	R	R	R	F	F	F
D_{b2}	F	F	R	R	R	R	R	R	R	R	F	F	F	F	R	R	R	R	R	R
Capacitor state																				
C_{a1}	D	D	C	D	D	C	D	D	C	C	D	D	D	C	D	D	C	D	D	C
C_{b1}	D	C	D	D	C	D	D	C	D	D	D	D	C	D	D	C	D	D	C	D
C_{c1}	C	D	D	C	D	D	C	D	D	D	C	C	D	D	C	D	D	C	D	D
C_{a2}	D	D	D	D	D	D	C	C	C	C	N	N	N	N	N	N	N	C	C	C
C_{b2}	D	D	D	C	C	C	N	N	N	N	N	N	N	N	C	C	C	D	D	D
C_{c2}	C	C	C	N	N	N	N	N	N	N	C	C	C	C	D	D	D	D	D	D

C=charging, D=discharging, N=not-connected, F=forward biased, and R=reverse biased



(a) $+1V_{in}$ (b) $+2V_{in}$ (c) $+3V_{in}$
(d) $+4V_{in}$ (e) $+5V_{in}$ (f) $+6V_{in}$
(g) $+7V_{in}$ (h) $+8V_{in}$ (i) $+9V_{in}$

Fig. 4. Realizing of some of the voltage levels of 19-level proposed SCMLI.

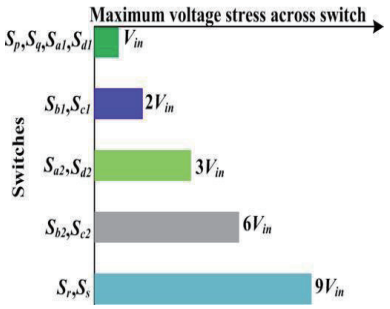


Fig. 5. Maximum voltage stress across various switches of 19-level SCMLI.

near V_{in} whereas C_{c2} rises its voltage to $3V_{in}$.

In a similar way, all the positive as well as negative voltage levels can be achieved across the load terminals. The various switching states and capacitor states for the rest of the positive and negative voltage levels are depicted in Table I. In addition, the maximum voltage stress of various switches are shown in Fig. 5. The *TSV* of the 19-level proposed structure is 44 V_{in}.

III. Generalized Proposed SCMLI

The generalized proposed SCMLI is depicted in Fig. 6. It comprises *n* number of capacitor legs (CL#1 to CL#*n*). Each CL consists of 3 series-connected capacitors. Each capacitor of a CL is charged by the previous CL capacitors except CL#1. For example, C_{a3} of CL#3 is charged by capacitors of CL#2. With this charging process, the voltage across the capacitors of *i*th CL can be represented by (1).

$$V_{Cai} = V_{Cbi} = V_{Cci} = 3^{i-1}V_{in} \quad \text{for } i = 1 \text{ to } n \tag{1}$$

With these capacitor voltages, the number of output voltage level (N_L), maximum output voltage (v_{omax}), and boosting factor (B) of the structure in terms of n can be represented by (2) to (4). Furthermore, the number of required switches (N_{sw}) or drivers (N_{dr}), diodes (N_{dio}), and capacitors (N_{cap}) in terms of n can be expressed by (5) to (7), respectively. The *TSV* of the structure is expressed in (8).

$$N_L = (2\times 3^n)+1 \tag{2}$$

$$v_{o\max} = 3^n V_{in} \tag{3}$$

$$B = \frac{v_{o\max}}{V_{in}} = 3^n \tag{4}$$

$$N_{sw} = N_{dr} = 4(n+1) \tag{5}$$

$$N_{dio} = 4n \tag{6}$$

$$N_{cap} = 3n \tag{7}$$

$$TSV = \left[5(3^n)-1\right]V_{in} \tag{8}$$

IV. Modulation Strategy of the Proposed SCMLI

This section outlines the modulation strategy for the proposed 19-level SCMLI, opting for the half-height fundamental switching (HHFS) strategy for its advantages in reduced switching losses and implementation simplicity. HHFS employs nine positive and nine negative DC signals, compared with the reference sinusoidal signal. Fig. 7(a) illustrates this process for the positive half-cycle, triggering inverter switching when the reference signal reaches halfway between voltage levels.

Fig. 7(b) shows cases sub-circuit-I, responsible for comparing the reference signal with positive DC signals and processing the output through logical gates (AND, XOR, and NOT) to generate logic signals (I_0 to I_9) corresponding to voltage levels from $0V_{in}$ to $9V_{in}$. Similarly, sub-circuit-II (Fig. 7(b)) compares the reference signal with negative DC signals, resulting in logic signals (I_{00} to I_{99}) corresponding to voltage levels from $0V_{in}$ to $-9V_{in}$. To derive the inverter's switching pulses, these logic signals from sub-circuits I and II are ORed together. The determination of which logic signals participate in realizing a specific switching signal is governed by the 19-level SCMLI switching table (Table I). Fig. 7(d)–(g) provides an illustration of the ORing operation generating some of the switching signals.

V. Selection Procedure of Optimum Capacitance for Capacitors of 19-Level Proposed SCMLI

This section outlines the capacitor selection process for 19-level proposed SCMLI. For evaluating the optimum capacitor sizes, the largest discharge period (LDP) of the capacitor over the output voltage cycle needs to be evaluated. Fig. 7 displays the LDP for different capacitors utilized in the 19-level SCMLI under a half-height (HH) fundamental switching frequency modulation scheme [19].

According to Fig. 8, LDP for C_{a1} is (t_{12}–t_8) whereas the LDP for C_{c1} is (t_{32}–t_{28}). It can be evident from Fig. 8 that the (t_{12}–t_8) time is equal to the (t_{32}–t_{28}) time. Hence, the LDP of C_{a1} and C_{c1} are the same. Similarly, the LDPs for C_{a2} and C_{c2} are the same and are equal to either (t_{16}–t_4) or (t_{36}–t_{24}) as shown in Fig. 8. The LDP for C_{b1} is equal to either (t_{11}–t_9) or (t_{31}–t_{29}). Similarly, the LDP for C_{b2} is either (t_{13}–t_7) or (t_{33}–t_{27}). During LDP, the capacitors release their accumulated energy toward the load. Hence, the capacitor discharging current is equal to the load current during LDP. The amount of charge released by the capacitors in 19-level SCMLI can be expressed by (9) and (10). Here, ΔQC_{a1} (or ΔQC_{c1}), and ΔQC_{b1} are the amount of charge released from C_{a1}(or C_{c1}) and C_{b1} respectively. Similarly, ΔQC_{a2} (or ΔQC_{c2}), and ΔQC_{b2} are the amount of charge released from C_{a2} (or C_{c2}) and C_{b2} respectively. The symmetry of the output voltage waveform can be used to find the limit of integration for (9) and (10). Where T is the fundamental time period for the output voltage cycle.

Considering the inverter is supplied a resistive load (R), the expression for the amount of charge released from the utilized capacitors can be expressed by (11) to (14). Using the HHFS modulation scheme, the various times (t_1 to t_9) in a quarter cycle of output voltage cycle can be evaluated by (15). The optimum capacitance for the utilized capacitors in 19-level SCMLI under *R*-load can be evaluated by (16) and (17). Here,

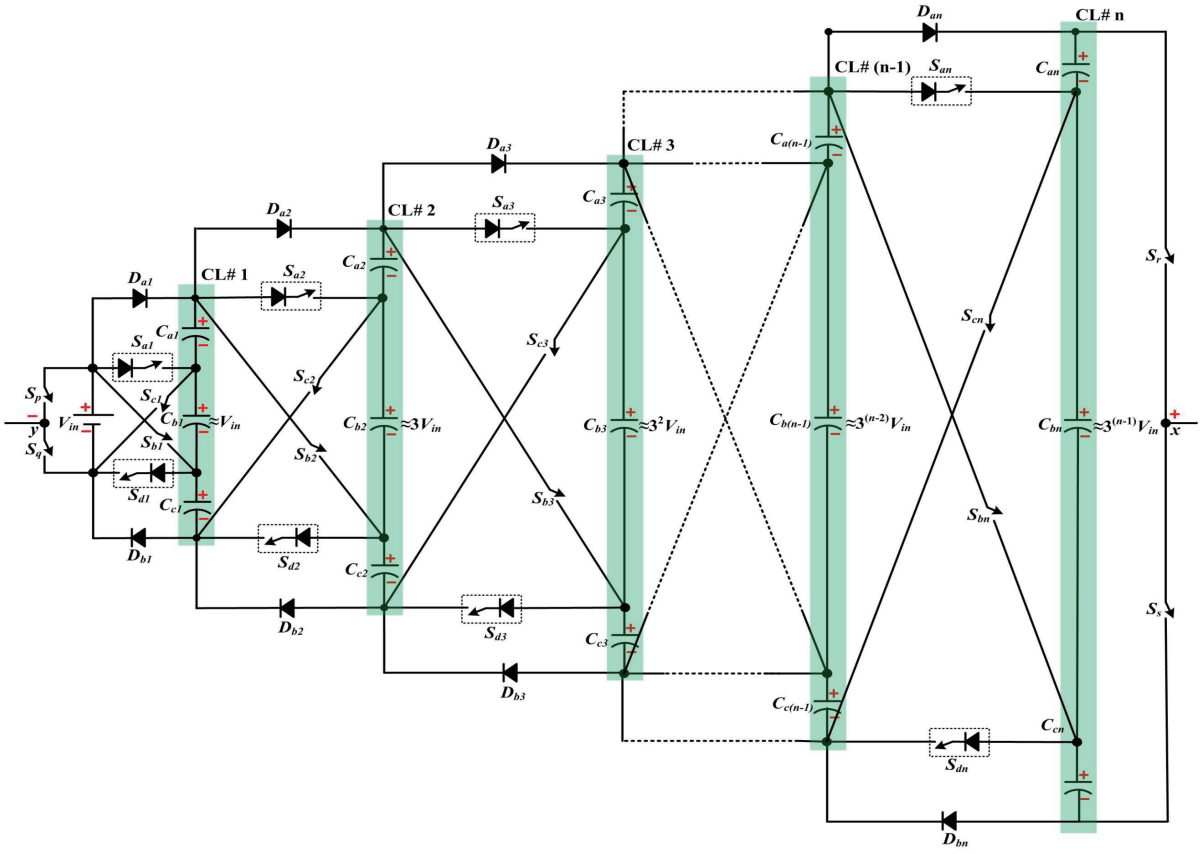
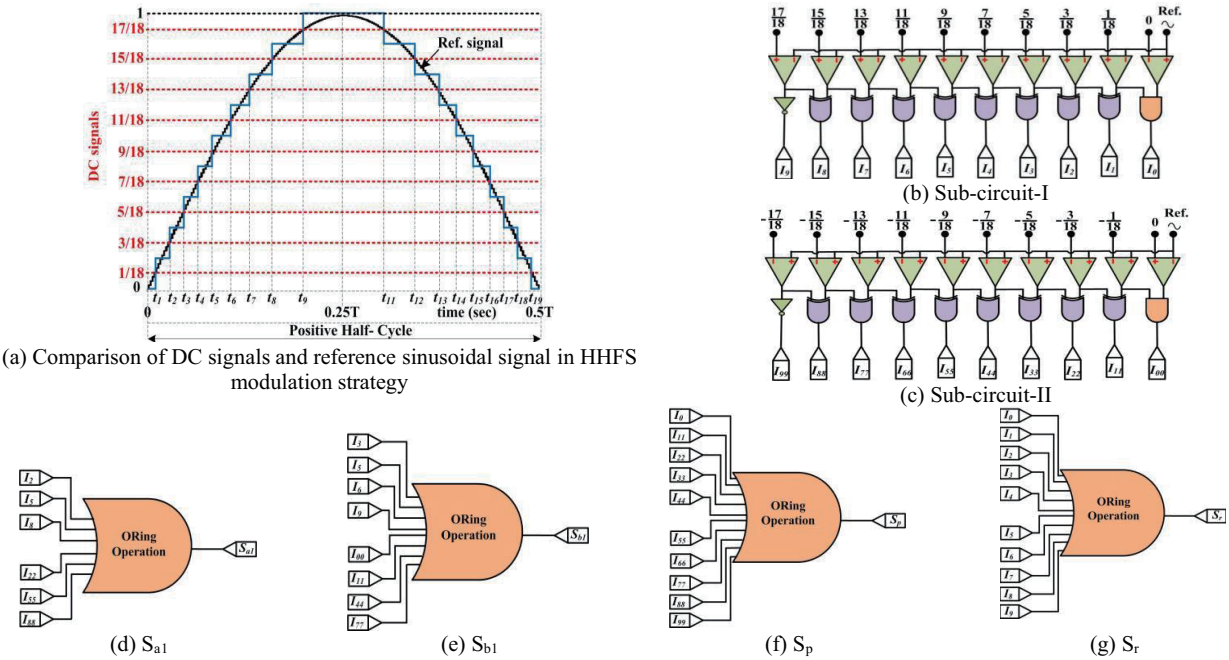


Fig. 6. Generalized proposed SCMLI.



(a) Comparison of DC signals and reference sinusoidal signal in HHFS modulation strategy

(b) Sub-circuit-I

(c) Sub-circuit-II

(d) S_{a1} (e) S_{b1} (f) S_p (g) S_r

Fig. 7. Implementation of HHFS modulation strategy for proposed 19-level SCMLI.

τ is the percentage capacitor voltage ripple under steady-state conditions and f is the output voltage frequency. Based on (16) and (17), the variation of optimum capacitance for different capacitors is depicted in Fig. 9. The plots provide the variation of optimum capacitance for five τ values (5%, 7%, 10%, 15%, and 20%) and load resistance variation range of 50 Ω to 400 Ω.

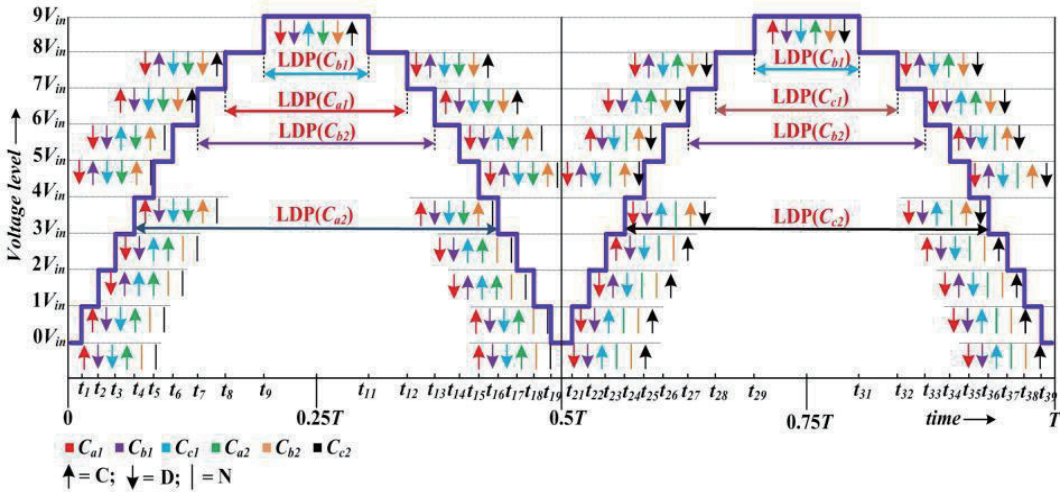


Fig. 8. LDP of various capacitors utilized in 19-level proposed SCMLI.

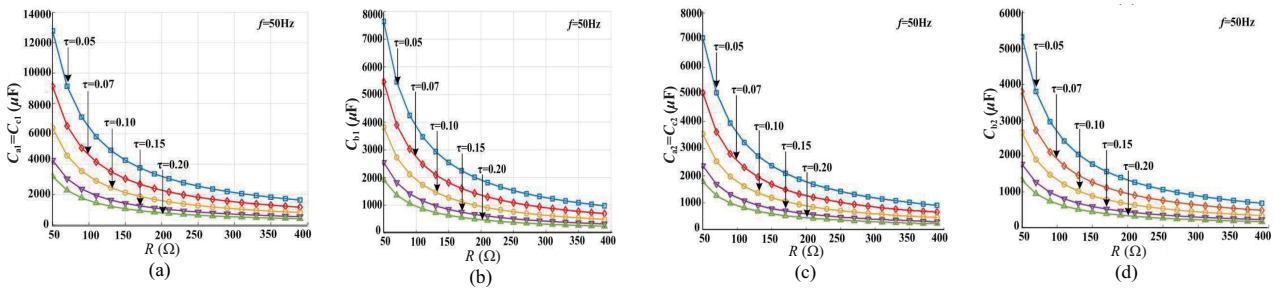


Fig. 9. Variation of optimum capacitance for 19-levele SCMLI.

According to Fig. 9, the optimum capacitance value decreases as the R increases for a particular τ value. Similarly, the optimum capacitance value decreases as the τ value increases for a particular value of R.

$$\Delta Q_{Ca1} = \Delta Q_{Cc1} = 2\times\left[\int_{t_8}^{0.25T} i_o(t)\,dt\right];\ \Delta Q_{Cb1} = 2\times\left[\int_{t_9}^{0.25T} i_o(t)\,dt\right] \quad (9)$$

$$\Delta Q_{Ca2} = \Delta Q_{Cc2} = 2\times\left[\int_{t_4}^{0.25T} i_o(t)\,dt\right];\ \Delta Q_{Cb2} = 2\times\left[\int_{t_7}^{0.25T} i_o(t)\,dt\right] \quad (10)$$

$$\Delta Q_{Ca1} = \Delta Q_{Cc1} = \frac{2V_{in}}{R}\left(2.25T - 8t_8 - t_9\right) \quad (11)$$

$$\Delta Q_{Cb1} = \frac{2V_{in}}{R}\left(2.25T - 9t_9\right) \quad (12)$$

$$\Delta Q_{Ca2} = \Delta Q_{Cc2} = \frac{2V_{in}}{R}\left(2.25T - 4t_4 - t_5 - t_6 - t_7 - t_8 - t_9\right) \quad (13)$$

$$\Delta Q_{Cb2} = \frac{2V_{in}}{R}\left(2.25T - 7t_7 - t_8 - t_9\right) \quad (14)$$

$$t_i = \frac{\sin^{-1}\left(\frac{2i-1}{18}\right)}{18}\ \forall i = 1\text{ to }9 \quad (15)$$

$$C_{a1} = C_{c1} \geqslant \frac{5.02}{\pi\times f\times R\times\tau};\ C_{b1} \geqslant \frac{3}{\pi\times f\times R\times\tau} \quad (16)$$

$$C_{a2} = C_{c2} \geqslant \frac{2.78}{\pi\times f\times R\times\tau};\ C_{c2} \geqslant \frac{2.09}{\pi\times f\times R\times\tau} \quad (17)$$

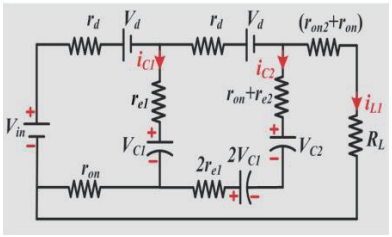
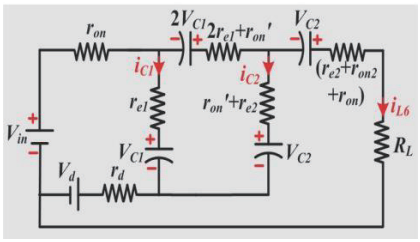
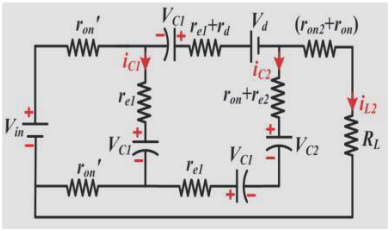
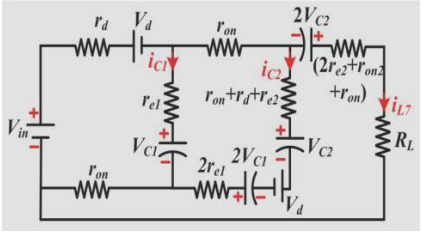
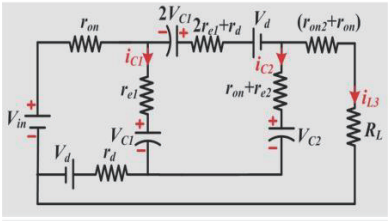
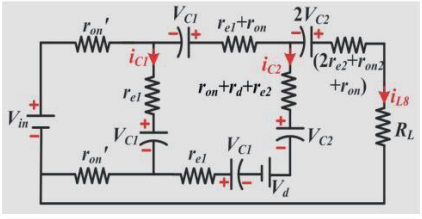
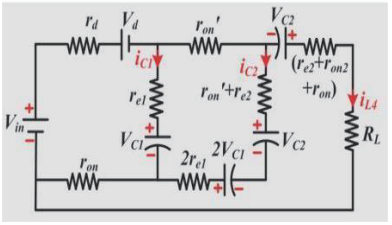
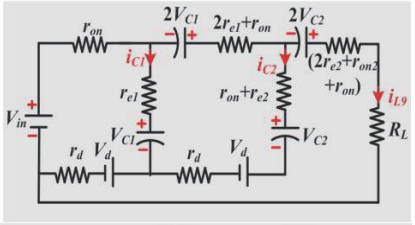
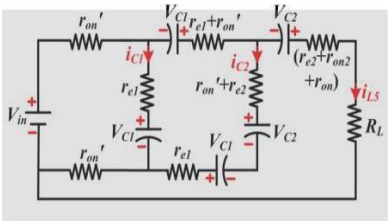
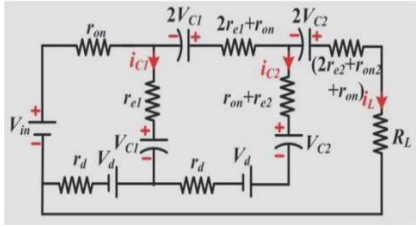
VI. Analysis of Power Losses of Proposed 19-Level SCMLI

The power losses analysis of the proposed 19-level SCMLI structure is presented in this section. Conduction losses, capacitor voltage ripple losses, and switching losses are the main losses associated with SCMLI [19]. The method for evaluating the various losses for the proposed 19-level SCMLI is provided in the ensuing subsections.

A. Evaluation of Conduction Losses

To evaluate the conduction losses of the proposed 19-level SCMLI, the equivalent circuits for each of the proposed converter's modes are developed while taking into account the parasitic resistances of different components. The proposed converter, as shown in Table II, has 10 operational modes (OM), (OM0 to OM9). The equivalent circuit with parasitic components for each mode is depicted in Table II. Here, r_d, r_{on}, r_{on}', r_{e1}, r_{e2}, and r_{on2} are the diode resistance, on-state resistance of

TABLE II
VARIOUS OPERATING MODES AND EQUIVALENT CIRCUITS FOR PROPOSED 19-LEVEL SCMLI

Operating mode (OM)	Equivalent circuits with parasitics	Operating mode (OM)	Equivalent circuits with parasitics
OM1 ($\pm 1V_{in}$)		OM6 ($\pm 6V_{in}$)	
OM2 ($\pm 2V_{in}$)		OM7 ($\pm 7V_{in}$)	
OM3 ($\pm 3V_{in}$)		OM8 ($\pm 8V_{in}$)	
OM4 ($\pm 4V_{in}$)		OM9 ($\pm 9V_{in}$)	
OM5 ($\pm 5V_{in}$)		OM0 ($\pm 0V_{in}$)	

switch that have an anti-parallel diode, on-state resistance of switch that do not have an anti-parallel diode, equivalent series resistance (ESR) of capacitor associated with CL#1, ESR of capacitor associated with CL#2, and on-state resistance of the high stress switches such as S_r or S_s. Similarly, V_d represents the forward voltage drop of the diode. One positive and one negative voltage level corresponds to each working mode. The OM1, for instance, is equivalent to $\pm 1V_{in}$ voltage levels. Table III tabulates the instantaneous conduction losses resulting from the load current for different modes of evaluation. Table III also shows the average conduction losses across a cycle for various levels of voltage. The sum of all average conduction losses, as shown by (18), is the overall conduction losses for the proposed 19-level SCMLI.

$$P_{cd} = \sum_{i=1}^{9} P_{av,i} \tag{18}$$

B. Evaluation of Capacitor Voltage Ripple Losses

One of the prime losses of SCMLIs is capacitor voltage ripple losses (P_{ripple}). These losses are occurred due to the energy losses associated with the charging process of the capacitor [19]. For a

TABLE III
EXPRESSIONS FOR INSTANTANEOUS AND AVERAGE CONDUCTION LOSSES FOR VARIOUS OPERATING MODES OF PROPOSED 19-LEVEL SCMLI

Operating mode (OM)	Instantaneous conduction losses	Average conduction losses
OM1 ($\pm 1V_{in}$)	$p_{cd1} = (2r_d + r_{on2} + r_{on}){i_{L1}}^2 + (2V_d i_{L1})$	$p_{avg1} = \frac{4(t_2 - t_1)}{T} p_{cd1}$
OM2 ($\pm 2V_{in}$)	$p_{cd2} = (r_{on}' + r_{on} + r_{e1} + r_d + r_{on2}){i_{L2}}^2 + (V_d i_{L2})$	$p_{avg2} = \frac{4(t_3 - t_2)}{T} p_{cd2}$
OM3 ($\pm 3V_{in}$)	$p_{cd3} = (2r_{on} + 2r_{e1} + r_d + r_{on2}){i_{L3}}^2 + (V_d i_{L3})$	$p_{avg3} = \frac{4(t_4 - t_3)}{T} p_{cd3}$
OM4 ($\pm 4V_{in}$)	$p_{cd4} = (r_d + r_{on}' + r_{on} + r_{e2} + r_{on2}){i_{L4}}^2 + (V_d i_{L4})$	$p_{avg4} = \frac{4(t_5 - t_4)}{T} p_{cd4}$
OM5 ($\pm 5V_{in}$)	$p_{cd5} = (2r_{on}' + r_{e1} + r_{on} + r_{e2} + r_{on2}){i_{L5}}^2$	$p_{avg5} = \frac{4(t_6 - t_5)}{T} p_{cd5}$
OM6 ($\pm 6V_{in}$)	$p_{cd6} = (2r_{on} + 2r_{e1} + r_{on}' + r_{e2} + r_{on2}){i_{L6}}^2$	$p_{avg6} = \frac{4(t_7 - t_6)}{T} p_{cd6}$
OM7 ($\pm 7V_{in}$)	$p_{cd7} = (r_d + 2r_{on} + 2r_{e2} + r_{on2}){i_{L7}}^2 + (V_d i_{L7})$	$p_{avg7} = \frac{4(t_8 - t_7)}{T} p_{cd7}$
OM8 ($\pm 8V_{in}$)	$p_{cd8} = (r_{on}' + 2r_{on} + 2r_{e2} + r_{on2}){i_{L8}}^2$	$p_{avg8} = \frac{4(t_9 - t_8)}{T} p_{cd8}$
OM9 ($\pm 9V_{in}$)	$p_{cd9} = (3r_{on} + 2r_{e1} + 2r_{e2} + r_{on2}){i_{L9}}^2$	$p_{avg9} = \frac{4(0.25T - t_9)}{T} p_{cd9}$

non-zero initial voltage of the capacitor, the energy losses due to the charging process can be evaluated by (19). Here, E_{rip} is the energy losses due to the capacitor's charging process and Δv_c is the voltage difference between the final value and the initial value of capacitor voltage. The Δv_c can be evaluated by (20). Where $(t_{j+1} - t_j)$ is the charging time duration for C.

$$E_{rip} = \frac{1}{2} C (\Delta v_c)^2 \tag{19}$$

$$\Delta v_c = \frac{1}{C} \int_{t_j}^{t_{j+1}} i_c(t) \mathrm{d}t \tag{20}$$

If the inverter has an N_c number of capacitors, then the overall ripple losses are equal to the summation of individual capacitor ripple losses as expressed by (21).

$$P_{rip(inv)} = \frac{1}{T} \sum_{i=1}^{N_C} E_{rip,i} \tag{21}$$

C. Evaluation of Switching Losses

This subsection presents the evaluation of switching losses. When a switch is turned ON from an OFF state or turned OFF from a ON state, it takes a certain amount of time, which is indicated as t_{on} and t_{off}. These times are referred to as switching times. During these switching times, the switch experiences certain power losses, which are referred to as switching power losses. Considering switch voltage and current are linearly varying during the switching times, the energy losses in the kth switch ($E_{k,on}$ and $E_{k,off}$) can be evaluated by (22) and (23).

$$E_{k,on} = \int_0^{t_{on}} V_{swk} \left(1 - \frac{t}{t_{on}}\right) I_k \left(\frac{t}{t_{on}}\right) \mathrm{d}t = \frac{1}{6} V_{swk} I_k t_{on} \tag{22}$$

$$E_{k,off} = \int_0^{t_{off}} I_k' \left(1 - \frac{t}{t_{off}}\right) V_{swk} \left(\frac{t}{t_{off}}\right) \mathrm{d}t = \frac{1}{6} V_{swk} I_k' t_{off} \tag{23}$$

In (22), I_k is the kth switch's current when the switch becomes ON from the OFF state. Similarly, in (23), I_k' is the kth switch's current before the switch becomes OFF from the ON state. The average switching losses are the losses over an output voltage cycle. For finding the average switching losses, the switching transitions of a switch over an output cycle need to be evaluated. Let, $N_{on,k}$ and $N_{off,k}$ are the ON transition and the OFF transition over an output cycle for the kth switch. The average switching energy losses for the kth switch ($E_{k,sw}$) can be expressed by (24). Then, the average switching power loss ($P_{k,sw}$) is the ratio of average switching energy losses and output cycle's time period. (25) depicts the average switching power losses for the kth switch. The switching losses of the inverter are the sum of all switch's average switching losses as expressed by (26).

$$E_{k,sw} = (N_{on,i} \times E_{i,on}) + (N_{off,i} \times E_{i,off}) \tag{24}$$

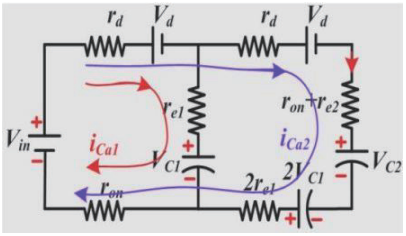


Fig. 10. Equivalent circuit of charging currents.

$$P_{k,\mathrm{sw}} = \frac{(N_{\mathrm{on},k} \times E_{k,\mathrm{on}}) + (N_{\mathrm{off},k} \times E_{k,\mathrm{off}})}{T}$$
$$= \frac{1}{6T} V_{\mathrm{sw}k} I_k (N_{\mathrm{on},k} t_{\mathrm{on}} + N_{\mathrm{off},k} t_{\mathrm{off}}) \quad (25)$$

$$P_{\mathrm{sw}} = \sum_{k=1}^{N_{\mathrm{sw}}} P_{k,\mathrm{sw}} \quad (26)$$

VII. Evaluation of Inrush Current and Supression Method

One of the major challenges for the SCMLIs is the inrush currents present in the circuit. These inrush currents flow through the charging loops of the circuit. As the capacitors behave like short circuits at the start of the inverter, the inrush current becomes very high magnitude and flows through the switches, diodes, capacitors, and the source. Also, under steady-state conditions, whenever the capacitors enter into the charging state, the high inrush currents flow through the charging loop due to the low equivalent series resistance associated with the charging path. These high values of inrush current can damage the switches, diodes, capacitors and source's life span.

As per the charging process of the proposed converter, simultaneous charging of capacitors for CL#1 and CL#2 happens. As per switching states, the capacitors C_{a1} and C_{c1} have more LDP than that for C_{b1} in CL#1, whereas C_{a2} and C_{c2} have more LDP than that for C_{b2} in CL#2. So the charging inrush current will be more when simultaneous charging of (C_{a1}, C_{b1}) or (C_{c1}, C_{c2}) will happen. So evaluation of inrush current due to capacitor charging for Fig. 2(a) or (c) is explained. The equivalent circuit for simultaneous charging of C_{a1} and C_{a2} can be redrawn in Fig. 10. By applying the Kirchhoff's voltage law (KVL), the magnitude of the charging currents can be expressed by (12). To mitigate this inrush current, a small value of the inductor in the range of 33 μH to 100 μH can be connected in series with the source for soft charging of the capacitors [29].

$$\begin{cases} i_{Ca1} = [V_{\mathrm{in}}(r_{\mathrm{eq}2} - r_{\mathrm{e}1}) + V_{\mathrm{d}}(r_{\mathrm{eq}1} - r_{\mathrm{eq}2}) + V_{C1}(4r_{\mathrm{e}1} - r_{\mathrm{eq}2} - 3r_{\mathrm{eq}1}) + \\ \qquad V_{C2}(r_{\mathrm{eq}1} - r_{\mathrm{e}1})] \times (r_{\mathrm{eq}1} r_{\mathrm{eq}2} - r_{\mathrm{e}1}^{\,2})^{-1} \\ i_{Ca2} = [V_{\mathrm{in}} r_{\mathrm{e}1} - V_{\mathrm{d}}(r_{\mathrm{eq}1} + r_{\mathrm{e}1}) - V_{C2} r_{\mathrm{eq}1} + 3V_{C1}(3r_{\mathrm{eq}1} - r_{\mathrm{e}1})] \times \\ \qquad (r_{\mathrm{eq}1} r_{\mathrm{eq}2} - r_{\mathrm{e}1}^{\,2})^{-1} \end{cases} \quad (27)$$

where $r_{\mathrm{eq}1} = r_{\mathrm{d}} + r_{\mathrm{e}1} + r_{\mathrm{on}}$, $r_{\mathrm{eq}2} = r_{\mathrm{d}} + 3r_{\mathrm{e}1} + r_{\mathrm{on}} + r_{\mathrm{e}2}$.

VIII. Comparison Study

In this section, the proposed SCMLI (PT) has been compared with popular asymmetric MMC [13], [14] and with recently developed single-source-based extendable SCMLIs [19], [21], [22], [24]–[28]. The comparison covers various aspects, including output voltage levels, required components, active switches for the highest voltage levels (N_{p}), active switches in the capacitor charging path ($N_{\mathrm{p\_c}}$), boosting factor (B), maximum capacitor voltage (MCV), maximum switch voltage stress (MSV), per unit TSV (TSV_{pu} i.e., total TSV per maximum output voltage), and the necessity of an H-bridge for negative voltage generation.

Table IV quantitatively compares PT with asymmetric MMCs and similar SCMLIs. The asymmetric MMCs presented in [13]. [14] required significantly higher number of switching devices and driver circuits for generating higher output voltage levels. Furthermore, they do not provide any boosting feature and self-capacitor voltage balancing ability as compared to PT. As compared to SCMLIs, PT requires fewer switches compared to most of the suggested SCMLIs. For 19-level output voltage, PT uses only 12 switches, while [19], [22], [26] require 20 or more switches. Similarly, for 21-level output voltage, [27] and [28] use 20 switches, while PT uses only 12 for 19-level output. In terms of driver circuits, PT requires fewer than most topologies in Table IV. For diodes and capacitors, PT also demands fewer compared to the presented SCMLIs.

In comparing N_{p} and $N_{\mathrm{p\_c}}$, PT needs only 4 conducting switches to achieve the highest voltage level, and 2 conducting semiconductor devices to charge capacitors, both of which are lower than most suggested SCMLIs in Table IV. These lower N_{p} and $N_{\mathrm{p\_c}}$ values in PT enhance the highest output voltage level, consequently improving the boosting factor of the inverter.

Referring to Table IV, PT achieves a maximum boosting factor for a 19-level output voltage waveform, akin to most suggested SCMLIs. Moreover, PT delivers a notably higher boosting factor compared to the SCMLI in [25]. In terms of TSV_{pu}, PT yields lower values than [19], [21], [22], [26], [28] due to the absence of an H-bridge. Table IV also presents a comparison of MCV and MSV. PT's MCV is $3V_{\mathrm{in}}$, while the MSV is $9V_{\mathrm{in}}$ for realizing 19-level output voltage levels.

In the cost function (CF) comparison, a standard CF comprising component count and TSV components is outlined in (28). In this equation, α represents the weightage factor for TSV. When $\alpha > 1$, TSV carries more weight; when $\alpha < 1$, component count has more weight. The topologies have been compared for α values of 0.5 and 1. According to Table IV, *PT* demonstrates lower CF per level per boosting factor ($CF/(N_{\mathrm{L}} \times B)$) values for both $\alpha = 0.5$ and $\alpha = 1$, outperforming most suggested SCMLIs and asymmetric MMCs.

$$CF = N_{\mathrm{sw}} + N_{\mathrm{dr}} + N_{\mathrm{d}} + N_{\mathrm{cap}} + \alpha TSV_{\mathrm{pu}} \quad (28)$$

Additionally, PT has been compared with [19], [22], [24], [26]–[28] across various output voltage levels, as shown in Fig. 11.

TABLE IV
COMPARISON STUDY OF PROPOSED SCMLI WITH OTHER SINGLE-SOURCE-BASED EXTENDABLE SCMLIS AND MMCS

SCMLI	N_L	N_{sw}	N_{dr}	N_{dio}	N_{cap}	N_p	N_{p_c}	B	MCV	MSV	TSV_{pu}	$CF/(N_L \times B)$ $\alpha=0.5$	$CF/(N_L \times B)$ $\alpha=1.5$	Negative level
[13]	19	24	24	0	12	6	1	1	$2V_{in}$	$2V_{in}$	4.00	3.26	3.47	Inherent
[14]	32	32	32	0	8	7	1	1	$8V_{in}$	$8V_{in}$	9.25	2.39	2.68	Inherent
[19]	19	20	20	8	8	10	2	9	$1V_{in}$	$9V_{in}$	5.77	0.28	0.32	H-bridge
[21]	17	12	12	3	3	5	4	8	$4V_{in}$	$8V_{in}$	6.50	0.24	0.29	H-bridge
[22]	19	20	20	20	8	3	2	9	$1V_{in}$	$9V_{in}$	13.30	0.43	0.51	H-bridge
[24]	17	10	10	6	6	5	2	8	$4V_{in}$	$8V_{in}$	4.00	0.25	0.28	Inherent
[25]	17	10	9	6	6	4	4	4	$2V_{in}$	$4V_{in}$	4.12	0.49	0.55	Inherent
[26]	19	28	23	8	8	6	3	9	$1V_{in}$	$2V_{in}$	5.00	0.40	0.43	Inherent
[27]	21	20	20	12	10	8	6	10	$5V_{in}$	$5V_{in}$	4.40	0.31	0.33	Inherent
[28]	21	20	20	8	8	8	3	10	$4V_{in}$	$4V_{in}$	5.20	0.28	0.30	Inherent
PT	19	12	12	8	6	4	2	9	$3V_{in}$	$9V_{in}$	4.88	0.23	0.26	Inherent

TABLE V
EXPRESSIONS OF VARIOUS PARAMENETS IN TERMS OF NL FOR VARIOUS SINGLE-SOURCE-BASED EXTENDABLE SCMLIS

SCMLI	N_{sw}	N_{dr}	N_{dio}	N_{cap}	$TSV(\times V_{in})$
[19]	N_L+1	N_L+1	$(N_L-3)/2$	$(N_L-3)/2$	$3N_L-5$
[22]	N_L+1	N_L+1	N_L+1	$(N_L-3)/2$	$\left[(N_L-3)(5N_L+21)+64\right]/16$
[26]	$(3N_L+7)/2$	$(5N_L+13)/4$	$(N_L-3)/2$	$(N_L-3)/2$	$(9N_L+9)/4$
[27]*	$4m_1+12$	$4m_1+12$	$8m_1+16$	$3m_1+4$	$4m_1^2+8m_1+12$
[28]	$8\log_2^{[(N_L+3)/6]}+4$	$8\log_2^{[(N_L+3)/6]}+4$	$4\log_2^{[(N_L+3)/6]}$	$4\log_2^{[(N_L+3)/6]}$	$(8N_L-12)/3$
[24]	$2\log_2^{[(N_L-1)/2]}+4$	$2\log_2^{[(N_L-1)/2]}+4$	$2\log_2^{[(N_L-1)/2]}$	$2\log_2^{[(N_L-1)/2]}$	$2N_L-2$
PT	$4\log_3^{[(N_L-1)/2]}+4$	$4\log_3^{[(N_L-1)/2]}+4$	$4\log_3^{[(N_L-1)/2]}$	$3\log_3^{[(N_L-1)/2]}$	$2.5N_L-3.5$

*$m_1=-1+\sqrt{(N_L-3)/2}$

Table IV also presents generalized parameter expressions in terms of N_L for PT and the suggested SCMLIs. Fig. 11(a) illustrates semiconductor device requirements (sum of switches and diodes) versus the output voltage level for PT and the suggested structures. Notably, PT requires significantly fewer semiconductor devices for a given output voltage level compared to [19], [22], [26]–[28]. Nevertheless, PT exhibits a slightly greater number of semiconductor devices compared to [24]. Fig. 11(b) shows the capacitor requirement across a range of output voltage levels, highlighting that PT necessitates the fewest capacitors compared to the suggested SCMLIs. Fig. 11(c) displays the variation of TSV concerning N_L for all compared topologies. PT exhibits lower TSV than [22], [19], [28] but higher TSV than [24], [26], [27]. In Fig. 11(d), the variation of *CF* per level (*CF*/N_L) with output voltage level is shown. PT achieves significantly lower *CF*/N_L compared to [19], [22], [26]–[28].Nonetheless, PT exhibits a marginally higher *CF*/N_L value in comparison to the topology outlined in [24].

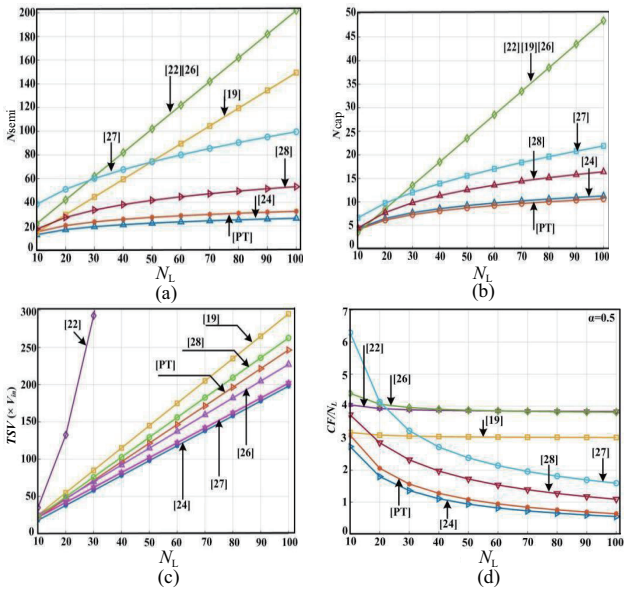


Fig. 11. Variation of (a) required semiconductors, (b) capacitors, (c) *TSV* and (d) *CF*/N_L with output voltage levels for proposed SCMLI and suggested SCMLIs in [19], [22], [24], [26]–[28].

IX. EXPERIMENTAL VERIFICATION

To experimentally validate the proposed SCMLI, a 19-level

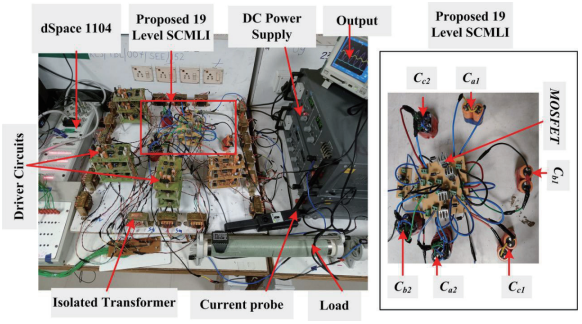


Fig. 12. Experimental set-up for proposed 19-level SCMLI.

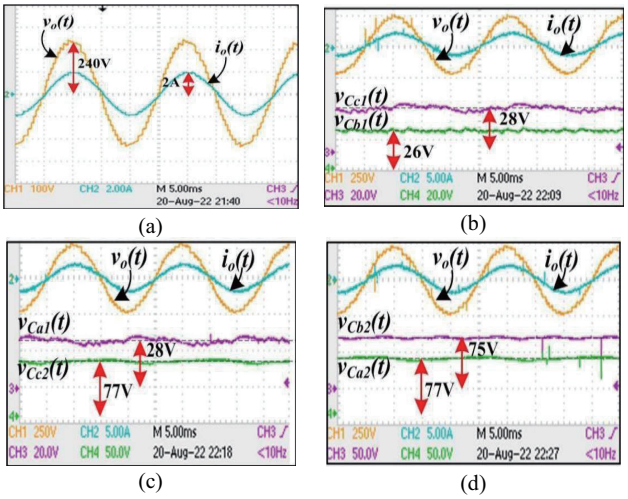


Fig. 13. Experimental waveforms for (a) 19-level output voltage and output current (100 V/div and 2 A/div), (b)–(d) capacitor voltages (20 V/div, 50 V/div) for resistive (R = 120 Ω) load condition.

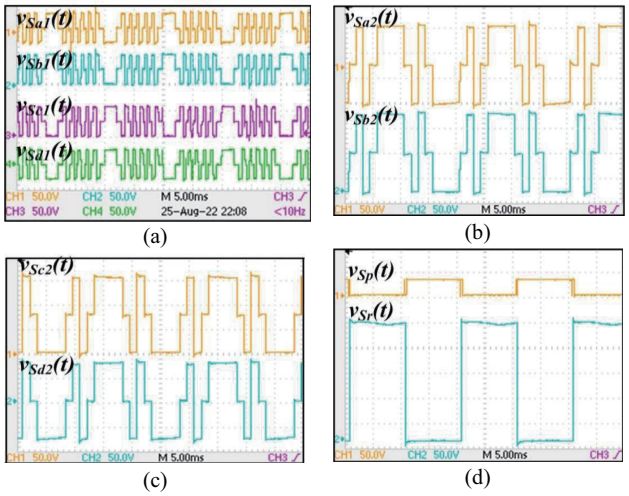


Fig. 14. Experimental stress voltage profiles for (a) S_{a1}, S_{b1}, S_{c1} and S_{d1} (50 V/div), (b) S_{a2} and S_{b2} (50 V/div), (c) S_{c2} and S_{d2} (50 V/div) and (d) S_p, S_r and S_{1c2} (50 V/div), for resistive (R = 120 Ω) load condition.

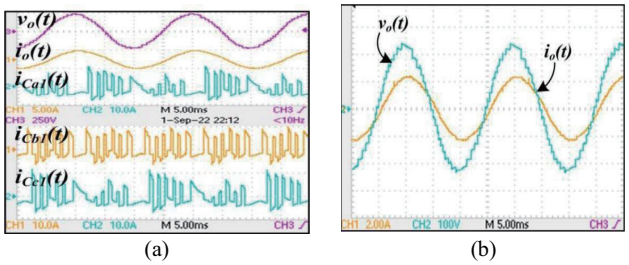
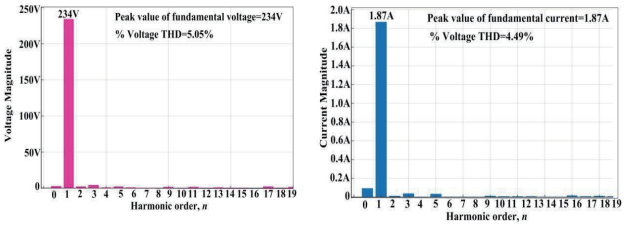


Fig. 15. Experimental waveforms for (a) various capacitor currents (10 A/div) for resistive (R = 120 Ω) load. (b) 19-level output voltage and output current (100 V/div and 2 A/div) for R-L load (R = 120 Ω, L = 50 mH).

prototype was constructed, as depicted in Fig. 12. IRF640 MOSFETs (18 A, 200 V) were employed as switching devices for the switches S_{b1}, S_{c1}, S_{b2}, S_{c2}, S_p, and S_q whereas S_{a1}, S_{d1}, S_{a2}, and S_{d2} have been implemented by IRF640 in series with a diode (MUR 460). For S_r and S_s, IRF840 MOSFETs (8 A, 500 V) were chosen due to their higher voltage stress requirements. The inverter operated with a 31 V input voltage. Capacitance values of 2500 µF each were selected for C_{a1}, C_{b1}, and C_{c1}, while C_{a2}, C_{b2}, and C_{c2} were equipped with 1880 µF each.

Fig. 13(a) shows the 19-level output voltage ($v_o(t)$) along with the load current ($i_o(t)$) when the inverter supplies a resistive load (R) of 120 Ω. As per this figure, the peak $v_o(t)$ is 240 V, whereas the peak $i_o(t)$ is 2 A. The $v_o(t)$ waveform has 19 voltage steps and it is in-phase with $i_o(t)$. With the same load, the steady state capacitor voltage waveform with $v_o(t)$ and $i_o(t)$ is depicted in Fig. 13(b)–(d). Fig. 13(b) shows the voltage across the capacitors C_{c1}, and C_{b1} whereas Fig. 13(c) depicts the voltage profiles for C_{a1} and C_{c2}. As per these figures, the voltage across C_{c1} and C_{a1} are 28 V each whereas that for C_{b1} is 26 V. Also, the voltage across C_{a2} and C_{c2} are equal to 77 V each whereas the voltage across C_{b2} is equal to 75 V as shown in Fig. 13(d). According to Fig. 13, the capacitor voltages are balanced and stable with the switching states as described in Table I. The experimental boosting factor of the structure is (240/31) = 7.74 which is lower than the theoretical boosting factor (B = 9) due to the voltage drops in the parasitic resistances in the current flow paths.

Under the same load condition, the voltage stresses of various switches are observed and depicted in Fig. 14. Fig. 14(a) presents the voltage stresses of S_{a1}, S_{b1}, S_{c1}, and S_{d1}. As per this figure, the voltage stresses across S_{a1} and S_{d1} are bipolar, whereas the voltage stresses for S_{b1} and S_{c1} are unipolar. In addition, the peak stress voltages incurred in S_{a1} and S_{d1} are within 31 V, whereas the peak stress voltages for S_{b1} and S_{c1} are within 61 V. Similarly, Fig. 14(b) and (c) depicts the voltage stress profiles for S_{a2}, S_{b2}, S_{c2}, and S_{d2}. As per these figures, the voltage stresses across S_{a2} and S_{d2} are bipolar, whereas the voltage stresses for S_{b2} and S_{c2} are unipolar. Further, the peak stress voltages across S_{a2} and S_{d2} are within 85 V , whereas the peak stress voltages across S_{b2} and S_{c2} are within 160 V. Fig. 14(d) shows the voltage stress profiles for S_p and S_r. As per this figure, the peak stress voltage for S_p is within 31 V, whereas the peak stress voltage for S_r is within 240 V. The experimental TSV of the proposed 19-level SCMLI is 1191 V. Considering the same load condition, the current profiles for C_{a1}, C_{b1} and C_{c1} are depicted in Fig. 15(a). The capacitor currents are pulsating in nature due to the charging state of the capacitors. The maximum peak current passing through C_{a1}, C_{b1} and C_{c1} are within 10 A. Similarly, the current profiles for C_{a2}, C_{b2}, and C_{c2} have



(a) (b)

Fig. 16. FFT analysis for (a) output voltage and (b) output current under resistive (R = 120 Ω) load condition.

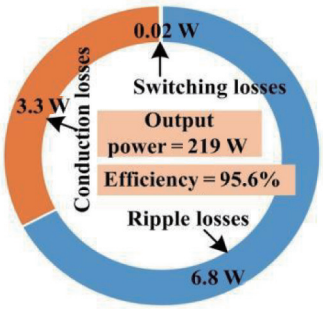


Fig. 17. Distribution of power losses in 19-level SCMLI.

been observed, and the peak current passing through C_{a2}, C_{b2} and C_{c2} are within 20 A.

For verifying the performance of the 19-level structure under the *R-L* load condition, the inverter supplies an *R-L* load of 120 Ω and 50 mH. The $v_o(t)$ and $i_o(t)$ under this load condition are observed as depicted in Fig. 15(b). According to this figure, the $i_o(t)$ is lagging behind $v_o(t)$. Under the resistive load of 120 Ω, the FFT analysis of the experimental $v_o(t)$ is shown in Fig. 16(a). According to this figure, the output voltage waveform has a 234 V peak fundamental component with a voltage THD of 5.05%. Similarly, the FFT analysis of $i_o(t)$ is shown in Fig. 16(b). As per this figure, the peak value of fundamental current is 1.87 A with a current THD of 4.49%.

The proposed 19-level SCMLI has three types of power losses, namely conduction losses, capacitor voltage ripple losses, and switching losses. Fig. 17 depicts the proportion of various losses in the 19-level inverter. As the inverter has been switched using a low switching frequency modulation strategy, the switching losses in the structure with a resistive load of 120 Ω are negligible (0.02 W). The conduction and ripple losses in the inverter are 3.3 W and 6.8 W, respectively. From FFT analysis, the output power of the inverter for 120 Ω load is 219 W. The total loss of the inverter is 10.12 W. The experimental efficiency of the proposed inverter is 95.6%.

X. Conclusion

This paper proposes a novel single-source-based SCMLI structure. The structure can realize higher output voltage levels with a lower number of components such as switches, and capacitors. It also provides a higher boosting factor. In addition, it can be easily extended for higher voltage level generation. The absence of an H-bridge circuit makes the TSV of the structure lower than other similar SCMLIs. The paper discusses the circuit description, charging process, and operating principle for the 19-level proposed SCMLI. Also, the generalized structure has been developed. A detailed discussion of the modulation strategy, the optimum capacitor selection procedure, and power loss analysis have been presented. Further, the paper presents the current evaluation and its mitigation. An extensive comparison study shows that the proposed inverter is more cost-effective than most of the recently developed similar SCMLIs for a range of output voltage levels. The performances of the proposed SCMLI have been verified by an extensive experimental study of the 19-level proposed SCMLI. For an output power of 219 W, the 19-level SCMLI provides 96.5% efficiency.

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