Circulating Current Suppression of Power Conversion Systems Under Unbalanced Conditions: Large-Signal Model-Based Analysis

Guangyu SONG, Xinghua LIU, Gaoxi XIAO, Liansong XIONG, Badong CHEN, and Peng WANG

***Abstract*—This paper proposes a large-signal model-based circulating current control approach to achieve the circulating current suppression and power quality improvement for power conversion systems (PCSs) under unbalanced conditions. Specifically, first of all, the adaptive capacitive virtual impedance (VI) is developed based on the change of the current difference to minimize the positive-sequence circulating current (PSCC). The robust droop control is introduced to tune the positive-sequence voltage output and implement the load sharing. Secondly, the negative-sequence reference signal is generated to enable negative-sequence current sharing. The secondary control signal is integrated with the positive-sequence voltage output to modify the voltage reference of the PCS and realize the unbalanced voltage compensation. Finally, the zero-sequence circulating current (ZSCC) controller is proposed by introducing the Q-PR controller and the feedforward term to suppress the ZSCC and attenuate the effect of filtering parameters on zero-axis current. The Lyapunov theory-based stability analysis is provided to prove the stabilization of the system modeled by a large signal. Experiments are presented to demonstrate the effectiveness of the proposed approach.**

***Index Terms*—Adaptive virtual impedance, circulating current suppression, large-signal model, power conversion systems, unbalanced voltage compensation.**

C_{dc}	DC voltage-stabilized capacitor
U_{dc}	DC bus voltage
L_f , L_g	LCL filter inductances
R_f , R_g	Parasitic resistances of inductors
C_f	LCL filter capacitor
Z_L, Z_{LCL}	Feeder impedance and filter impendance
e_a, e_b, e_c	There-phase grid voltage
i, u	Output current and voltage of inverter
u_C	Capacitor voltage
i_g	Grid current
j	jth inverter module
i_{ga}, i_{gb}, i_{gc}	There-phase currents
i_g^+, i_g^-, i_g^z	Positive-sequence, negative-sequence, and zero sequence current components
i_{gc}^+, i_{gc}^-, i_{gc}^z	Positive-sequence, negative-sequence, and zero sequence circulating currents
p, q	Instantaneous power
ω_j, ω^*	Angular frequency and rated angular frequency of PCSs
U_j, U^*	RMS values of inverter output and rated voltage
P_j^+, Q_j^+	Rated power
P_j^+, Q_j^+	Positive-sequence power
γ_j, ℓ_j	Droop coefficients
ω_c	Cut-off frequency of LPF
K_U	Voltage gain
u_{Cj}^+	Droop controller positive-sequence output voltage
Z_v, R_v, C_v	Virtual impedance, resistance and capacitance
R_0, C_0	Initial values of virtual resistance and capacitance
μ, ν	Adaptive VI coefficients
$\bar{i}_{gj}^-$, $\bar{i}_{gk}^-$	Mean negative-sequence current estimations of jth and kth modules
$\bar{\lambda}$	Estimation weight
N_j	Set of neighbors of jth module
ΔU_c^-	Negative-sequence current reference
k_{drp}, k_{dri}	Proportional and integral gains of droop controller
k_{cp}, k_{ci}	Proportional and integral gains of current sharing
δU_j^+, δU_j^-	Positive-sequence and negative-sequence compensation voltage
U_{refj}^-, I_{refj}^-, I_{refj}^z	Negative-sequence reference voltage and current and zero-sequence reference current
k_{up}, k_{ip}, k_{ui}, k_{ii}	Proportional and integral gains of negativesequence module
k_v, k_{vr}, k_c, k_{cr}	Proportion and resonance gains of Q-PR control
ω_r, ω_0, ω_z	Cut-off frequency, resonant bandwidths of NSCC and ZSCC
k_z, k_{zr}	Proportion and resonance gains of ZSCC controller
u_{refj}^*	Voltage reference
T_s	Sampling time
$'$,□	Necessary and unnecessary submatrices
$\hat{\delta}_j$, ω_{ref}	Power angle and global reference angular frequency
$f(\cdot)$	Dynamical system
R^n	N-dimensional real number set
R_+	Set of positive real numbers
P_j, Q_j	Positive definite and symmetrical matrix
K_1, K_2	Gain matrices
τ	Eigenvalue of matrices

Manuscript received September 1, 2023; revised November 17, 2023; accepted December 18, 2023. Date of publication June 30, 2024; date of current version January 2, 2024. This work was supported in part by National Natural Science Foundation of China under grant U2003110. *(Corresponding author: Xinghua Liu.)*

G. Song and X. Liu are with the School of Electrical Engineering, Xi'an University of Technology, Xi'an 710048, China (e-mail: songgy@stu.xaut.edu.cn; liuxh@xaut.edu.cn).

G. Xiao and P. Wang are with the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore (e-mail: egxxiao@ntu.edu.sg; epwang@ntu.edu.sg).

L. Xiong is with the School of Electrical Engineering, Xi'an Jiaotong University, Xi'an 710049, China, and also with the School of Automation, Nanjing Institute of Technology, Nanjing 211167, China (e-mail: xiongliansong@xjtu.edu.cn).

B. Chen is with the Institute of Artificial Intelligence and Robotics, Xi'an Jiaotong University, Xi'an 710049, China (e-mail: chenbd@mail.xjtu.edu.cn).

Digital Object Identifier 10.24295/CPSSTPEA.2023.00051

I. Introduction

With the development of distributed generation, the grid-forming power conversion system (PCS) has been extensively applied in microgrids and low-voltage distribution networks [1]–[4]. Hybrid energy supplies are generally connected by the common DC bus to improve the energy conversion efficiency in the PCS [5]. Due to the limitation of the rated power of a single grid-forming inverter, the parallel framework is generalized to achieve high-power transmission [6], [7]. The parallel configurations significantly reduce the energy loss. However, there exists a major challenge in that the circulating current can be produced between parallel modules and access the inverters. While only the zero-sequence circulating current (ZSCC) shall be considered under balanced operation conditions, the positive-sequence circulating current (PSCC), negative-sequence circulating current (NSCC), and ZSCC should be concerned under unbalanced operation conditions [8]. The generation of circulating current can result in current distortions, switching losses, lower efficiency of PCSs, etc. Consequently, the circulating current suppression remains as a research hotspot.

The suppression schemes mainly consist of passive techniques, modulation strategies, and other control approaches. The passive device isolation transformers are adopted to the AC terminal to cut off the circulating current loop [9]. However, it increases the hardware cost and size. Also, the synchronous operation of parallel modules is realized by cutting the power supplies to suppress the ZSCC in [10]. However, the high-frequency ZSCC cannot be eliminated.

Different from the passive techniques, the modulation strategies aim to eliminate the circulating current by using vector control rather than by adding hardware circuits [11]–[14]. Zhang et al. [15] proposed a carrier-waves-based pulse width modulation (PWM) strategy combined with the bias voltage injection. However, the high-frequency circulating currents are not considered to eliminate. Wang et al. [16] presented a unified online calculation technique of the nominal circulating current injection to analyze the impact of circulating current on the power losses and voltage ripples. In such an approach, however, there is a need for the instantaneous data of converters, which significantly increases the calculation difficulty and burdens. Jiang et al. [17] developed a hybrid PWM scheme with the same zero-sequence injection voltage to attenuate the ZSCC. A deadbeat control method for multi-parallel inverters was presented to suppress the ZCSS in [18]. The method can suppress the ZCSS spike to improve the power quality. In [19], the deadbeat control was integrated with the close-loop control to suppress the high-frequency ZSCC produced by the carrier phase difference. It can also address the low-frequency ZSCC.

Except for the above techniques and strategies, many control approaches have also been developed to tackle circulating current mitigation under unbalanced operating conditions [20]. Castilla et al. [21] proposed a hybrid voltage and current control approach by utilizing only the measured currents to complete the negative-sequence current sharing. In [22], a hybrid control approach was introduced to tune the dwell times of small signals in real time for ZSCC suppression under unbalanced conditions. In the existing studies, VI control has been extensively applied in circulating current mitigation [23]. Zhang et al. [24] proposed a VI distributed control approach to compensate for the voltage deviation and minimize the ZSCC. The approach has no demand for extra communication. However, it does not consider the impact of the voltage drop produced by the VI. The PSCC and NSCC under unbalanced conditions are not addressed. Aquib et al. [25] proposed an adaptive VI control scheme to reduce the ZSCC produced by output impedance differences. A comprehensive control scheme combining the improved droop control with the adaptive VI was proposed to cover the circulating current generated by the mismatched feeder impedance in [26]. However, this scheme requests the calculation of the equivalent feeder impedance. The calculation complexity is large.

To investigate the PCS stabilization under unbalanced conditions, the small-signal models have been constructed to conduct stability analysis [27], [28]. Wang et al. [29] presented a characteristic-equation-based small-signal modeling scheme for parallel converters to realize system stability assessment. Peng et al. [30] developed a voltage unbalanced compensation approach based on a small-signal analysis to eliminate the voltage imbalance at PCC. Akhavan et al. [31] proposed a stability analysis for inverters in unbalanced grids by decoupling the multi-input multi-output system into the single-input single-output systems. However, the small-signal analysis can only study the stability of the system suffering from small disturbances near a steady-state operating point. It can't handle the stability problem of nonlinear systems with multiple equilibrium states. The Lyapunov-based large-signal stabilization analysis therefore has been studied [32]–[34]. Kabalan et al. [35] proposed a Lyapunov-based large-signal stability analysis approach for parallel inverters to improve the transient stability of the grid terminal. In [36], a dual-layer back-stepping control approach was proposed for the static synchronous compensator to attenuate the circulating current. This approach ensures the Lyapunov stabilization of the system.

As can be seen from the above, circulating current suppression and voltage compensation in an inverter system are essential when operating under unbalanced conditions. Unbalanced conditions may lead to poor power quality, causing voltage sags, harmonics, and other issues. Circulating current suppression and voltage compensation help maintain the system stable operation and ensure longer component life while minimizing losses, improving system efficiency, and achieving more effective energy conversion [37]. Moreover, voltage and current imbalances can result from grid disturbances, such as faults or transient events. In such cases, effective control measures can help mitigate the impact of these disturbances on the inverter system and maintain continuous operation [38]. In response to the circulating current issues of PCSs under unbalanced conditions, this article proposes a large-signal model-based circulating current control approach to achieve the circulating current mitigation and ensure the Lyapunov stabilization of PCSs. It mainly comprises the robust droop controller, current sharing part, ZSCC suppressor, and

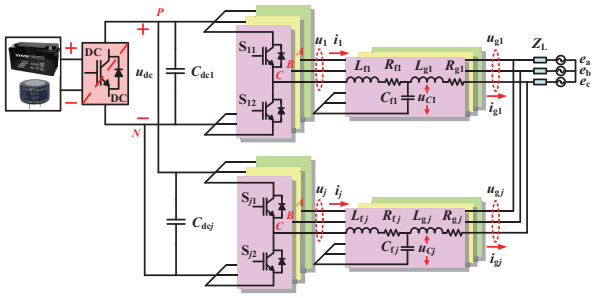


Fig. 1. Topology of grid-connected PCSs.

voltage compensation units. An adaptive capacitive VI is designed based on the change of the current difference among different modules to mitigate the PSCC. The robust droop control accomplishes the load sharing and low-frequency filtering to eliminate the impact of the high-order harmonics. The compensation signals are combined with the positive-sequence voltage output to attenuate the negative-sequence components such that the bus output voltage can be tuned to its reference trajectory. The ZSCC controller is developed by adding the quasi-proportional resonant (Q-PR) controller and a feedforward term to achieve the ZSCC suppression and eliminate the disturbance to zeroaxis current. The main contributions of the article can be summarized as follows:

1) Unlike other VIs [23], [26], [31], the proposed adaptive capacitive VI is constructed based on the change of the current difference among different modules to selfupdate the VI value. The proposed secondary signal can both achieve the unbalanced voltage compensation and the reference voltage tracking.
2) The ZSCC controller is developed by introducing the Q-PR controller and the feedforward term to suppress the ZSCC and eliminate the disturbance of the filtering capacitor on zero-axis current.
3) Different from the small-signal modeling approach [28]–[31], the proposed control approach is based on large signal modeling to preciously track the reference trajectory and guarantee system Lyapunov stability.

The remaining parts of the article are organized as follows: Section II gives the system description. The large-signal model-based control approach is explored and the Lyapunov theory-based stability analysis is provided in Section III. Experimental verification is demonstrated in Section IV. Finally, Section V summarizes the article.

II. System Description

Fig. 1 illustrates the topology of parallel energy storage inverters. The system employs a framework of sharing DC sides and AC sides. The dynamic model is acquired as

$$\begin{cases} L_{\mathrm{f}j}\dfrac{\mathrm{d}i_j}{\mathrm{d}t} = u_j - R_{\mathrm{f}j}\,i_j - u_{\mathrm{C}j} \\ C_{\mathrm{f}j}\dfrac{\mathrm{d}u_{\mathrm{C}j}}{\mathrm{d}t} = i_j - i_{\mathrm{g}j} \\ L_{\mathrm{g}j}\dfrac{\mathrm{d}i_{\mathrm{g}j}}{\mathrm{d}t} = u_{\mathrm{C}j} - R_{\mathrm{g}j}\,i_{\mathrm{g}j} - u_{\mathrm{g}j} \end{cases} \tag{1}$$

Hence, the system state equation is given as

$$\begin{cases} \dot{x}_{\mathrm{LCL}j}(t) = A_{\mathrm{LCL}j}\,x_{\mathrm{LCL}j}(t) + B_{\mathrm{LCL}j}\,\vec{u}_{\mathrm{LCL}j}(t) \\ y_{\mathrm{LCL}j}(t) = C_{\mathrm{LCL}j}\,x_{\mathrm{LCL}j}(t) \end{cases} \tag{2}$$

where there exist $x_{\mathrm{LCL}j}(t) = [i_j(t)\ u_{\mathrm{C}j}(t)\ i_{\mathrm{g}j}(t)]^{\top}$, $\vec{u}_{\mathrm{LCL}j}(t) = [u_j(t)\ 0\ u_{\mathrm{g}j}(t)]^{\top}$, $y_{\mathrm{LCL}j}(t) = [i_{\mathrm{g}j}(t)\ u_{\mathrm{C}j}(t)]^{\top}$.

$$A_{\mathrm{LCL}j} = \begin{bmatrix} -\dfrac{R_{\mathrm{f}j}}{L_{\mathrm{f}j}} & -\dfrac{1}{L_{\mathrm{f}j}} & 0 \\ \dfrac{1}{C_{\mathrm{f}j}} & 0 & -\dfrac{1}{C_{\mathrm{f}j}} \\ 0 & \dfrac{1}{L_{\mathrm{g}j}} & -\dfrac{R_{\mathrm{g}j}}{L_{\mathrm{g}j}} \end{bmatrix},\ B_{\mathrm{LCL}j} = \begin{bmatrix} \dfrac{1}{L_{\mathrm{f}j}} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & -\dfrac{1}{L_{\mathrm{g}j}} \end{bmatrix},$$

$$C_{\mathrm{LCL}j} = \begin{bmatrix} 0 & 0 & 1 \\ 0 & 1 & 0 \end{bmatrix}.$$

The mathematical formulation of the grid terminal from Fig. 1 in the abc coordinates can be represented as

$$\begin{bmatrix} u_{\mathrm{ga}} \\ u_{\mathrm{gb}} \\ u_{\mathrm{gc}} \end{bmatrix} - \begin{bmatrix} e_{\mathrm{a}} \\ e_{\mathrm{b}} \\ e_{\mathrm{c}} \end{bmatrix} = \begin{bmatrix} Z_{\mathrm{La}} & 0 & 0 \\ 0 & Z_{\mathrm{Lb}} & 0 \\ 0 & 0 & Z_{\mathrm{Lc}} \end{bmatrix} \begin{bmatrix} i_{\mathrm{ga}} \\ i_{\mathrm{gb}} \\ i_{\mathrm{gc}} \end{bmatrix} \tag{3}$$

Referring to [17], the circulating current of phase a of two parallel PCSs is defined as $i_{\mathrm{ca}} = 1/2\,(i_{\mathrm{g1}} - i_{\mathrm{g2}})$.

The method of symmetrical components is employed to decouple the asymmetric components [39]. The output currents under unbalanced operation can be derived as

$$\begin{bmatrix} i^{+}_{\mathrm{ga}j} \\ i^{-}_{\mathrm{ga}j} \\ i^{z}_{\mathrm{ga}j} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & \rho & \rho^2 \\ 1 & \rho^2 & \rho \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} i_{\mathrm{ga}j} \\ i_{\mathrm{gb}j} \\ i_{\mathrm{gc}j} \end{bmatrix} \tag{4}$$

where $\rho = e^{j2\pi/3}$. Considering the impedance factors, there exists Z_{LCL} such that $i^{(+/-)}_{\mathrm{gc}} = (u^{(+/-)}_{\mathrm{g}1} - u^{(+/-)}_{\mathrm{g}2})/[3(Z_{\mathrm{LCL1}} + Z_{\mathrm{LCL2}})]$.

When a three-phase unbalance or ground fault occurs, the voltage difference between different modules acts on the output impedance, generating the circulating current. Under unbalanced conditions, there are not only ZSCC but also PSCC and NSCC. It is noted that the circulating current and unbalanced components can be eliminated by increasing system damping or injecting voltage.

By adopting Park coordinate transformation [20], the dynamic model can be transformed into

$$\begin{cases} u_{jdq0} - u_{\mathrm{C}jdq0} = R_{\mathrm{f}j}\,i_{jdq0} + L_{\mathrm{f}j}\,\dot{i}_{jdq0} - L_{\mathrm{f}j}\begin{bmatrix} 0 & \omega & 0 \\ -\omega & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} i_{jdq0} \\ i_{jdq0} - i_{\mathrm{g}jdq0} = C_{\mathrm{f}j}\,\dot{u}_{\mathrm{C}jdq0} - C_{\mathrm{f}j}\begin{bmatrix} 0 & \omega & 0 \\ -\omega & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} u_{\mathrm{C}jdq0} \\ u_{\mathrm{C}jdq0} - e_{jdq0} = R_{\mathrm{g}j}\,i_{\mathrm{g}jdq0} + L_{\mathrm{g}j}\,\dot{i}_{\mathrm{g}jdq0} - L_{\mathrm{g}j}\begin{bmatrix} 0 & \omega & 0 \\ -\omega & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} i_{\mathrm{g}jdq0} \end{cases} \tag{5}$$

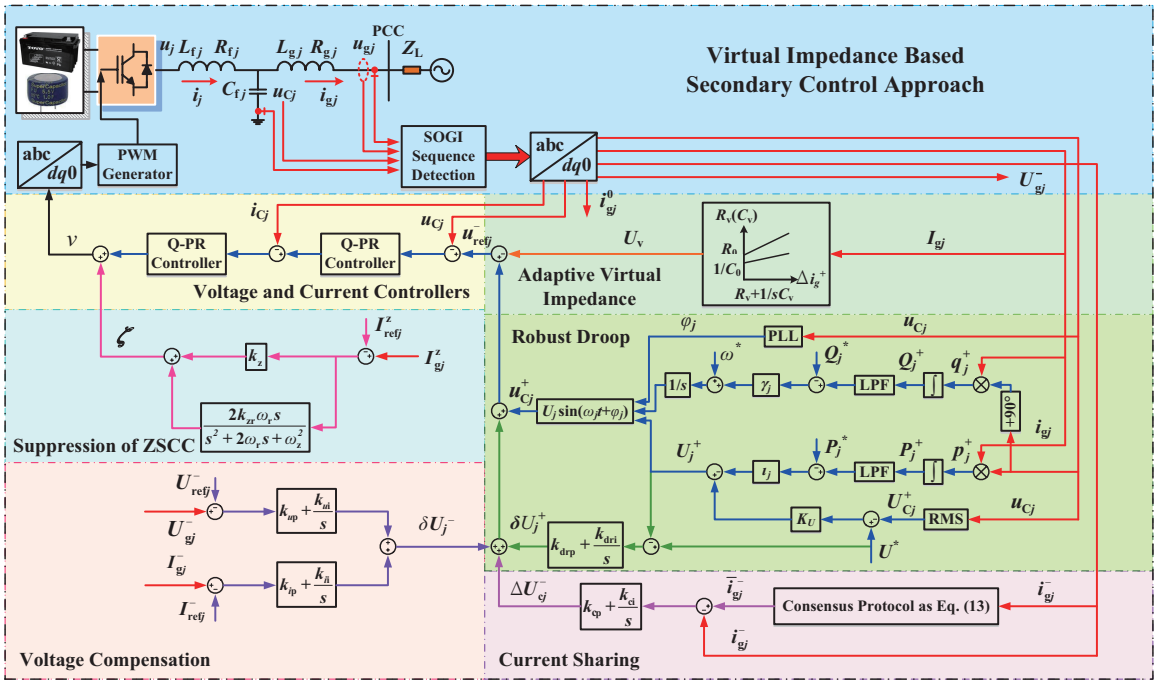


Fig. 2. Control diagram of the proposed control approach.

The instantaneous power of PCSs in the *dq* coordinates is generated as [35].

$$\begin{bmatrix} p_j \\ q_j \end{bmatrix} = \frac{3}{2} \begin{bmatrix} u_{Cdj} & u_{Cqj} \\ -u_{Cqj} & u_{Cdj} \end{bmatrix} \begin{bmatrix} i_{gdj} \\ i_{gqj} \end{bmatrix} \tag{6}$$

In (6), the calculated instantaneous power comprises DC and AC components. The instantaneous power is decomposed by the second-order general integrator (SOGI) [40] to acquire the positive-sequence and negative-sequence fundamental components (u^+_{dq}, i^+_{dq}, u^-_{dq}, i^-_{dq}) and filter out the second-harmonic components. SOGI can accurately track the input signals and strongly suppress the signal noise.

III. Proposed Control Approach

In this section, the circulating current control scheme for parallel PCSs is proposed to achieve the circulating current suppression and ensure the system Lyapunov stability. The control diagram of the proposed control approach is exhibited in Fig. 2, which mainly contains the positive-sequence robust droop and adaptive VI control unit, negative-sequence current sharing unit, voltage compensation unit, and ZSCC suppression unit.

A. Circulating Current Suppression and Voltage Compensation

Assumption 1: The reference signals are equivalent for PCSs, i.e., $u^*_{refk} = u^*_{refj}, \forall\, k \in N_j$.

1) Designing Adaptive Virtual Impedance and Minimizing PSCC

To support the low-voltage PCSs, positive-sequence robust droop control is introduced to generate a sinusoidal voltage output. Due to the resistive properties of the output impedance, the $P-\omega$ and $Q-U$ characteristics are no longer applicable. The implemented form of positive-sequence robust droop control is expressed as:

$$\omega_j = \omega^* + \gamma_j \frac{\omega_c}{s + \omega_c}(Q_j^+ - Q_j^*) \tag{7}$$

$$U_j^+ = -\ell_j \frac{\omega_c}{s + \omega_c}(P_j^+ - P_j^*) + K_U(U^* - U_{Cj}^+) \tag{8}$$

where there exists a cycle T such that $P_j^+ = \frac{1}{T}\int_t^{t+T} p_j^+(\tau)\,\mathrm{d}(\tau)$ and $Q_j^+ = \frac{1}{T}\int_t^{t+T} q_j^+(\tau)\mathrm{d}(\tau)$.

In order to increase the system damping, a VI loop is added to change the total output impedance of the PCS. The adaptive VI is designed based on the change of the current difference among different modules to mitigate the PSCC. It is constructed as:

$$Z_v(s) = R_v + \frac{1}{sC_v} \tag{9}$$

The self-updating parameters R_v and $1/sC_v$ are defined as:

$$R_v = R_0 + \mu(i^+_{g1} - i^+_{g2}) \tag{10}$$

$$\frac{1}{sC_v} = \frac{1}{sC_0} + v(i^+_{g1} - i^+_{g2}) \tag{11}$$

(7) and (8) inherit the superiorities of the droop control and compensate for the terminal voltage drop produced by total output impedances. The VI is designed according to the change of the current difference to improve the dynamic performance

of the circulating current suppression, which is more conducive to minimizing the PSCC. The VI voltage is fed to the droop control output.

In fact, the voltage drop (8) can be reformulated as

$$\delta U_j^+ = U^* - U_j^+ = \ell_j (P_j^+ - P_j^*) + (1 - K_U) U^* + K_U U_{\mathrm{C}j}^+ \tag{12}$$

The voltage loss produced by droop control is compensated to the output voltage reference to implement voltage recovery. This unit compensates for not only the load voltage drop but also the voltage drop caused by inverter control.

Remark 1: Circulating currents will increase system loss and reduce system performance, thus the capacitive VI is able to mitigate this issue. Moreover, the capacitive VI provides voltage support by injecting capacitive reactive power into the system, which can help stabilize grid voltage and improve power quality, especially in situations where voltage sags, disturbances occur, or load rapidly changes [41]. The capacitive element of VI reduces harmonic distortion in the grid by suppressing positive circulating currents while enhancing the system stability, especially in the presence of unbalanced loads or grid disturbances [42], [43]. Therefore, the capacitive VI is a promising construction method.

2) Sharing Negative-Sequence Current and Compensating Unbalanced Voltage

Due to the mismatched output impedance of parallel systems, the NSCC will be produced under unbalanced conditions. It is clear from Fig. 2 that the dynamic consensus protocol is used to generate the mean value of the negative-sequence current [44], as follows:

$$\bar{i}_{\mathrm{g}j}^-(t) = i_{\mathrm{g}j}^-(t) + \bar{\lambda}^- \int_0^t \sum_{k \in N_j}^{\infty} [i_{\mathrm{g}k}^-(\tau) - i_{\mathrm{g}j}^-(\tau)] \mathrm{d}\tau \tag{13}$$

It can be noted that the negative-sequence current reference $\Delta\tilde{U}_{cj}^-$ is generated by the deviation $\bar{i}_{gj}^- - i_{gj}^-$ via PI controller to achieve the negative-sequence currents sharing, i.e., there exists $\Delta\tilde{U}_{cj}^- = (k_{cp} + k_{ci}/s)(\bar{i}_{gj}^- - i_{gj}^-)$. In the case of mismatched line impedance, the reference still has applicability in current sharing. $\Delta\tilde{U}_{cj}^-$ is fed to the droop control output.

The negative-sequence voltage of the system is jointly acted by the negative-sequence voltages of the PCC and PCS. Normally, the PCC voltage is obtained by the lowbandwidth communication network. However, there will be communication delays or interruptions. Hence, the negativesequence voltage of the PCS can be controlled to achieve the coordinated compensation of the negative-sequence voltage of the PCC.

The voltage deviation between $U_{\mathrm{ref}j}^-$ and U_{gj}^- and the current deviation between $I_{\mathrm{ref}j}^-$ and I_{gj}^- are integrated with PI controllers to construct the unbalanced voltage compensation term. The negative-sequence signals can track the reference values configured to zero to eliminate the voltage unbalance of the PCS. The negative-sequence compensation term is constructed as

$$\delta U_j^- = (k_{u\mathrm{p}} + \frac{k_{u\mathrm{i}}}{s})(U_{\mathrm{ref}j}^- - U_{gj}^-) + (k_{i\mathrm{p}} + \frac{k_{i\mathrm{i}}}{s})(I_{\mathrm{ref}j}^- - I_{gj}^-) \tag{14}$$

where $U_{\mathrm{ref}j}^-$ and $I_{\mathrm{ref}j}^-$ are configured to zero.

In the positive-sequence dq rotating coordinate frame, the grid frequency is 50 Hz. Thus, there exist 100 Hz negativesequence components and 150 Hz zero-sequence components under unbalanced conditions. Since the PI control cannot track the AC reference value without static error, the Q-PR control with the corresponding resonant frequency is adopted to achieve zero steady-state error. The expression of the Q-PR controller is written as [16].

$$G_{\mathrm{v}}(s) = k_{\mathrm{v}} + \frac{2k_{\mathrm{vr}}\omega_{\mathrm{r}} s}{s^2 + 2\omega_{\mathrm{r}} s + \omega_0^2} \tag{15}$$

where ω_0 is set to $2\pi \times 100 = 628$ rad/s to eliminate the negative-sequence components. Considering the frequency fluctuation of ±2% in the national power supply business rules, ω_{r} is configured to $\omega_{\mathrm{r}} = 2\pi \times 50 \times 2\% = 6.28$ rad/s.

3) Suppression of ZSCC

When there is a zero-sequence loop and the zero-sequence voltage acts on the output impedance, the ZSCC components are generated in the system current. The ZSCC is defined as [13].

$$i_{\mathrm{gc}}^{\mathrm{z}} = \frac{1}{3}(i_{\mathrm{ga}} + i_{\mathrm{gb}} + i_{\mathrm{gc}}) \tag{16}$$

Based on [20], there exists a Park transform matrix such that $i_{\mathrm{c}}^{\mathrm{z}} = i_0$ holds. It is noted that the ZSCC can be suppressed by controlling the 0-axis current. Therefore, the ZSCC model can be rewritten as

$$i_{\mathrm{gc}j}^{\mathrm{z}}(s) = -\frac{sC_{\mathrm{f}j} u_{gj}^{\mathrm{z}}}{\Theta_j} + \frac{u_j^{\mathrm{z}} - u_{\mathrm{C}j}^{\mathrm{z}}}{\Theta_j \chi_j} \tag{17}$$

where $\Theta_j = s^2 L_{gj} C_{\mathrm{f}j} + sR_{gj} C_{\mathrm{f}j} + 1$ and $\chi_j = R_{\mathrm{f}j} + sL_{\mathrm{f}j}$.

A control signal ζ is proposed to achieve the ZSCC suppression. It yields

$$i_{\mathrm{gc}j}^{\mathrm{z}}(s) = \frac{u_{gj}^{\mathrm{z}}}{\Theta_j}(\zeta - sC_{\mathrm{f}j} + \frac{u_j^{\mathrm{z}} - u_{\mathrm{C}j}^{\mathrm{z}}}{u_{gj}^{\mathrm{z}} \chi_j}) \tag{18}$$

Taking into account the frequency characteristics of the zero-sequence current, the Q-PR term is added to the ZSCC controller, whose transfer function can be expressed as

$$G_{\mathrm{z}}(s) = k_{\mathrm{z}} + \frac{2k_{\mathrm{zr}}\omega_{\mathrm{r}} s}{s^2 + 2\omega_{\mathrm{r}} s + \omega_{\mathrm{z}}^2} \tag{19}$$

where ω_{z} is set to $2\pi \times 150 = 942$ rad/s to suppress the ZSCC. The block diagram of the ZSCC control is illustrated in Fig. 3. $I_{\mathrm{ref}j}^{\mathrm{z}}$ is configured to zero. Then, the compensation signals are combined with the positive-sequence voltage output and the VI voltage to tune the voltage reference of the PCS. The voltage reference $u_{\mathrm{ref}dqj}^*$ is expressed as:

$$u_{\mathrm{ref}\,dqj}^* = u_{\mathrm{C}\,dqj}^+ + \delta U_{dqj}^+ + \Delta\tilde{U}_{\mathrm{c}\,dqj}^- + \delta U_{dqj}^- - U_{\mathrm{v}dqj} \tag{20}$$

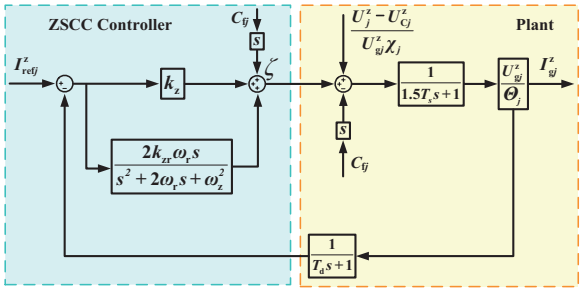


Fig. 3. Block diagram of ZSCC suppression.

Remark 2: The control approach mainly consists of five parts, namely positive-sequence robust droop and adaptive VI control, voltage compensation, negative-sequence current sharing, circulating current suppression, and voltage and current control. The voltage reference is yielded by integrating the voltage compensation terms and the VI voltage into the positive-sequence voltage output produced by the robust droop control. The reference signal is input to the voltage and current controllers, which use the Q-PR controller to complete error-free tracking. $G_{\text{plant}} = 1/(1.5T_s s+1)$ represents the transfer function of the plant.

B. Large-Signal Stability Analysis

To achieve the Lyapunov theory-based stability analysis, the accurate large-signal model is established in the *dq* coordinate frame. The state space equation of LCL in the PCS can be rewritten as

$$\begin{cases} \dot{x}_{\text{LCL}j}(t) = \widetilde{A}_{\text{LCL}j}\, x_{\text{LCL}j}(t) + \widetilde{B}_{\text{LCL1}j}\, \vec{u}_{\text{LCL1}j}(t) + \\ \qquad\qquad \widetilde{B}_{\text{LCL2}j}\, \vec{u}_{\text{LCL2}j}(t) \\ y_{\text{LCL}j}(t) = \widetilde{C}_{\text{LCL}j}\, x_{\text{LCL}j}(t) \end{cases} \tag{21}$$

where $x_{\text{LCL}j}(t) = [i_{dj}(t)\ i_{qj}(t)\ u_{Cdj}(t)\ u_{Cqj}(t)\ i_{gdj}(t)\ i_{gqj}(t)]^{\top}$, $\vec{u}_{\text{LCL1}j}(t) = [u_{dj}(t)\ u_{qj}(t)]^{\top}$, $\vec{u}_{\text{LCL2}j}(t) = [u_{gdj}(t)\ u_{gqj}(t)]^{\top}$, $y_{\text{LCL}j}(t) = [i_{gdj}(t)\ i_{gqj}(t)\ u_{Cdj}(t)\ u_{Cqj}(t)]^{\top}$.

$$\widetilde{A}_{\text{LCL}j} = \begin{bmatrix} -\frac{R_{fj}}{L_{fj}} & \omega_c & -\frac{1}{L_{fj}} & 0 & 0 & 0 \\ -\omega_c & -\frac{R_{fj}}{L_{fj}} & 0 & -\frac{1}{L_{fj}} & 0 & 0 \\ \frac{1}{C_{fj}} & 0 & 0 & \omega_c & -\frac{1}{C_{fj}} & 0 \\ 0 & \frac{1}{C_{fj}} & -\omega_c & 0 & 0 & -\frac{1}{C_{fj}} \\ 0 & 0 & \frac{1}{L_{gj}} & 0 & -\frac{R_{gj}}{L_{gj}} & \omega_c \\ 0 & 0 & 0 & \frac{1}{L_{gj}} & -\omega_c & -\frac{R_{gj}}{L_{gj}} \end{bmatrix}$$

$$\widetilde{B}_{\text{LCL1}j} = \begin{bmatrix} \frac{1}{L_{fj}} & 0 \\ 0 & \frac{1}{L_{fj}} \\ 0_{4\times 1} & 0_{4\times 1} \end{bmatrix},\quad \widetilde{B}_{\text{LCL2}j} = \begin{bmatrix} 0_{4\times 1} & 0_{4\times 1} \\ -\frac{1}{L_{fj}} & 0 \\ 0 & -\frac{1}{L_{gj}} \end{bmatrix},$$

$$\widetilde{C}_{\text{LCL}j} = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \end{bmatrix}.$$

The positive-sequence robust droop control has been described in the previous section. The state space equation of the robust droop controller can be constructed as

$$\begin{cases} \dot{x}_{\text{RD}j}(t) = \widetilde{A}_{\text{RD}j}\, x_{\text{RD}j}(t) + \widetilde{B}_{\text{RD}j}\, \vec{u}_{\text{RD}j}(t) + \widetilde{F}_{\text{RD}j}\, \widetilde{\omega}_{\text{RD}j}(t) \\ y_{\text{RD}j}(t) = \widetilde{C}_{\text{RD}j}\, x_{\text{RD}j}(t) + \widetilde{W} \end{cases} \tag{22}$$

where there exists the power angle $\hat{\delta}_j$ such that $\mathrm{d}\hat{\delta}_j/\mathrm{d}t = \omega_j - \omega_{\text{ref}}$. We have the definition as $x_{\text{RD}j} = [\hat{\delta}_j\ P_j^{+}\ Q_j^{+}]^{\top}$, $y_{\text{RD}j} = [\omega_j\ u_{Cdj}^{+}\ u_{Cqj}^{+}]^{\top}$, $\vec{\omega}_{\text{RD}j} = [\omega^{*} - \omega_{\text{ref}} - \gamma_j Q^{*}]^{\top}$, $\vec{u}_{\text{RD}j} = [i_{dj}\ i_{qj}\ u_{Cdj}\ u_{Cqj}\ i_{gdj}\ i_{gqj}]^{\top}$. u_{Cqj}^{*} is configured to 0. The parameter matrices $\widetilde{A}_{\text{RD}j}$, $\widetilde{B}_{\text{RD}j}$, $\widetilde{F}_{\text{RD}j}$, and $\widetilde{C}_{\text{RD}j}$ are given as

$$\widetilde{A}_{\text{RD}j} = \begin{bmatrix} 0 & 0 & \gamma_j \\ 0 & -\omega_c & 0 \\ 0 & 0 & -\omega_c \end{bmatrix},\quad \widetilde{F}_{\text{RD}j} = \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix},$$

$$\widetilde{B}_{\text{RD}j} = \begin{bmatrix} 0_{1\times 4} & 0 & 0 \\ 0_{1\times 4} & 1.5\,\omega_c u_{Cdj} & 1.5\,\omega_c u_{Cqj} \\ 0_{1\times 4} & -1.5\,\omega_c u_{Cqj} & 1.5\,\omega_c u_{Cdj} \end{bmatrix},$$

$$\widetilde{C}_{\text{RD}j} = \begin{bmatrix} 0 & 0 & \gamma_j \\ 0 & -\ell_j & 0 \\ 0 & 0 & 0 \end{bmatrix},\ \widetilde{W} = \begin{bmatrix} \omega^{*} - \gamma_j Q^{*} \\ \ell_j P^{*} + K_U(U^{*} - U_{gj}) \\ 0 \end{bmatrix}.$$

The LPF is used for the VI loop to filter out harmonics and produce the VI voltage. The state equation can be given as

$$\begin{cases} \dot{x}_{\text{VI}j}(t) = \widetilde{A}_{\text{VI}j}\, x_{\text{VI}j}(t) + \widetilde{B}_{\text{VI}j}\, \vec{u}_{\text{VI}j}(t) \\ y_{\text{VI}j}(t) = \widetilde{C}_{\text{VI}j}\, x_{\text{VI}j}(t) \end{cases} \tag{23}$$

where there exist $x_{\text{VI}j} = [I_{gdj}\ I_{gqj}]^{\top}$, $y_{\text{VI}j} = [U_{vdj}\ U_{vqj}]^{\top}$, $\vec{u}_{\text{VI}j} = [i_{gdj}\ i_{gqj}]^{\top}$.

$$\widetilde{A}_{\text{VI}j} = \begin{bmatrix} -\omega^{*} & 0 \\ 0 & -\omega^{*} \end{bmatrix},\ \widetilde{B}_{\text{VI}j} = \begin{bmatrix} \omega^{*} & 0 \\ 0 & \omega^{*} \end{bmatrix},\ \widetilde{C}_{\text{VI}j} = \begin{bmatrix} R_v & -\frac{1}{\omega^{*} C_v} \\ R_v & \frac{1}{\omega^{*} C_v} \end{bmatrix}.$$

The voltage compensation parts are developed in the previous section, as exhibited in Fig. 2. Define the error deviations $\mathrm{d}\sigma_{dj}/\mathrm{d}t = U_{Cdj}^{*} - U_{Cdj}^{+}$, $\mathrm{d}\sigma_{qj}/\mathrm{d}t = U_{Cqj}^{*} - U_{Cqj}^{+}$, $\mathrm{d}\varrho_{dj}/\mathrm{d}t = U_{\text{ref}dj} - U_{gdj}$, $\mathrm{d}\varrho_{qj}/\mathrm{d}t = U_{\text{ref}qj} - U_{gqj}$, $\mathrm{d}\phi_{dj}/\mathrm{d}t = I_{\text{ref}dj} - I_{gdj}$, $\mathrm{d}\phi_{qj}/\mathrm{d}t = I_{\text{ref}qj} - I_{gqj}$. The state space model of the compensators can be constructed as

$$\begin{cases} \dot{x}_{\text{R}j}(t) = \widetilde{A}_{\text{R}j}\, x_{\text{R}j}(t) + \widetilde{B}_{\text{R}j}\, \vec{u}_{\text{R}j}(t) + \widetilde{F}_{\text{R1}j}\, \vec{w}_{\text{R}j}(t) \\ y_{\text{R}j}(t) = \widetilde{C}_{\text{R}j}\, x_{\text{R}j}(t) + \widetilde{D}_{\text{R}j}\, \vec{u}_{\text{R}j}(t) + \widetilde{F}_{\text{R2}j}\, \vec{w}_{\text{R}j}(t) \end{cases} \tag{24}$$

where there exist $x_{\text{R}j} = [\sigma_{dj}\ \sigma_{qj}\ \varrho_{dj}\ \varrho_{qj}\ \phi_{dj}\ \phi_{qj}]^{\top}$, $\vec{\omega}_{\text{R}j} = [U_{Cdj}^{*}\ U_{Cqj}^{*}\ U_{\text{ref}dj}\ U_{\text{ref}qj}\ I_{\text{ref}dj}\ I_{\text{ref}qj}]^{\top}$, $y_{\text{R}j} = [\delta U_{dj}^{+}\ \delta U_{qj}^{+}\ \delta U_{dj}\ \delta U_{qj}]^{\top}$, $\vec{u}_{\text{R}j} = [U_{Cdj}^{+}\ U_{Cqj}^{+}\ U_{gdj}\ U_{gqj}\ I_{gdj}\ I_{gqj}]^{\top}$.

$$\widetilde{A}_{\text{R}j} = [\,0_{6\times 6}\,],$$

$$\widetilde{B}_{\text{R}j} = diag\{\underbrace{-1, \cdots, -1}_{6}\},\ \widetilde{F}_{\text{R1}j} = diag\{\underbrace{1, \cdots, 1}_{6}\},$$

$$\widetilde{C}_{\text{R}j} = \begin{bmatrix} k_{\text{dri}} & 0 & 0 & 0 & 0 & 0 \\ 0 & k_{\text{dri}} & 0 & 0 & 0 & 0 \\ 0 & 0 & k_{ui} & 0 & k_{ii} & 0 \\ 0 & 0 & 0 & k_{ui} & 0 & k_{ii} \end{bmatrix},$$

$$\widetilde{D}_{\mathrm{R}j}=\begin{bmatrix}-k_{\mathrm{drp}}&0&0&0&0&0\\0&-k_{\mathrm{drp}}&0&0&0&0\\0&0&-k_{up}&0&-k_{ip}&-\omega^{*}L_{gj}\\0&0&0&-k_{up}&\omega^{*}L_{gj}&-k_{ip}\end{bmatrix},$$

$$\widetilde{F}_{\mathrm{R}2j}=\begin{bmatrix}k_{\mathrm{drp}}&0&0&0&0&0\\0&k_{\mathrm{drp}}&0&0&0&0\\0&0&k_{up}&0&k_{ip}&0\\0&0&0&k_{up}&0&k_{ip}\end{bmatrix}.$$

According to (13), considering the current sharing simplified model, the state equation of the current sharing module are acquired as

$$\begin{cases}\dot{x}_{\mathrm{CS}j}(t)=\widetilde{A}_{\mathrm{CS}j}x_{\mathrm{CS}j}(t)+\widetilde{B}_{\mathrm{CS}j}\vec{u}_{\mathrm{CS}j}(t)+\widetilde{B}_{\mathrm{CS}k}\vec{u}_{\mathrm{CS}k}(t)\\ y_{\mathrm{CS}j}(t)=\widetilde{C}_{\mathrm{CS}j}x_{\mathrm{CS}j}(t)+\widetilde{D}_{\mathrm{CS}j}\vec{u}_{\mathrm{CS}j}(t)+\widetilde{F}_{\mathrm{CS}j}\vec{\omega}_{\mathrm{CS}j}(t)\end{cases}\tag{25}$$

where $\mathrm{d}\bar{\sigma}_{dj}/\mathrm{d}t=\bar{i}_{gdj}(t)-\bar{i}_{gdj}(t)$, $\mathrm{d}\bar{\sigma}_{qj}/\mathrm{d}t=\bar{i}_{gqj}(t)-\bar{i}_{gqj}(t)$ and $x_{\mathrm{CS}j}=[\bar{\sigma}_{dj}\ \bar{\sigma}_{qj}]^{\top}$, $y_{\mathrm{CS}j}=[\Delta\bar{U}_{cdj}\ \Delta\bar{U}_{cqj}]^{\top}$, $\vec{u}_{\mathrm{CS}j}=[\bar{i}_{gdj}\ \bar{i}_{gqj}]^{\top}$, $\vec{u}_{\mathrm{CS}k}=[\bar{i}_{gdk}\ \bar{i}_{gqk}]^{\top}$, $\vec{\omega}_{\mathrm{CS}j}=[\bar{i}_{gdj}\ \bar{i}_{gqj}]^{\top}$.

$$\widetilde{A}_{\mathrm{CS}j}=\begin{bmatrix}0&0\\0&0\end{bmatrix},\ \widetilde{D}_{\mathrm{CS}j}=\begin{bmatrix}-k_{\mathrm{cp}}&-\omega^{*}L_{gj}\\\omega^{*}L_{gj}&-k_{\mathrm{cp}}\end{bmatrix},$$

$$\widetilde{B}_{\mathrm{CS}j}=\begin{bmatrix}-\bar{\lambda}\sum_{k\in N_j,\,j\neq k}^{\infty}&0\\0&-\bar{\lambda}\sum_{k\in N_j,\,j\neq k}^{\infty}\end{bmatrix},\ \widetilde{C}_{\mathrm{CS}j}=\begin{bmatrix}k_{\mathrm{ci}}&0\\0&k_{\mathrm{ci}}\end{bmatrix},$$

$$\widetilde{B}_{\mathrm{CS}k}=\begin{bmatrix}\bar{\lambda}\sum_{k\in N_j,\,j\neq k}^{\infty}&0\\0&\bar{\lambda}\sum_{k\in N_j,\,j\neq k}^{\infty}\end{bmatrix},\ \widetilde{F}_{\mathrm{CS}j}=\begin{bmatrix}k_{\mathrm{cp}}&0\\0&k_{\mathrm{cp}}\end{bmatrix}.$$

The voltage error dynamics are defined as $\mathrm{d}\xi_{dj}/\mathrm{d}t=u^{*}_{\mathrm{ref}dj}-u_{\mathrm{C}dj}$ and $\mathrm{d}\xi_{qj}/\mathrm{d}t=u^{*}_{\mathrm{ref}qj}-u_{\mathrm{C}qj}$. Therefore, there exist $u^{*}_{\mathrm{ref}dj}=u^{+}_{\mathrm{C}dj}+\delta U^{+}_{dj}+\Delta U^{-}_{cdj}+\delta U^{-}_{dj}-U_{vdj}$ and $u^{*}_{\mathrm{ref}qj}=u^{+}_{\mathrm{C}qj}+\delta U^{+}_{qj}+\Delta U^{-}_{cqj}+\delta U^{-}_{qj}-U_{vqj}$.

Considering the voltage and current loop modules, the output dynamics can be listed as

$$\begin{cases}i^{*}_{dj}=G_{\mathrm{PR}}(u^{*}_{\mathrm{ref}dj}-u_{\mathrm{C}dj})-\omega^{*}C_{\mathrm{f}j}u_{\mathrm{C}qj}+i_{\mathrm{g}dj}\\ i^{*}_{qj}=G_{\mathrm{PR}}(u^{*}_{\mathrm{ref}qj}-u_{\mathrm{C}qj})+\omega^{*}C_{\mathrm{f}j}u_{\mathrm{C}dj}+i_{\mathrm{g}qj}\\ u^{*}_{dj}=G_{\mathrm{PR}}(i^{*}_{dj}-i_{dj})-\omega^{*}L_{\mathrm{f}j}i_{qj}+u_{\mathrm{g}dj}\\ u^{*}_{qj}=G_{\mathrm{PR}}(i^{*}_{qj}-i_{qj})-\omega^{*}L_{\mathrm{f}j}i_{dj}+u_{\mathrm{g}qj}\end{cases}\tag{26}$$

The state space equation of the voltage controller can be expressed as:

$$\begin{cases}\dot{x}_{\mathrm{U}j}(t)=\widetilde{A}_{\mathrm{U}j}x_{\mathrm{U}j}(t)+\widetilde{B}_{\mathrm{U}j}\vec{u}_{\mathrm{U}j}(t)+\widetilde{F}_{\mathrm{U}1j}\vec{\omega}_{\mathrm{U}j}(t)\\ y_{\mathrm{U}j}(t)=\widetilde{C}_{\mathrm{U}j}x_{\mathrm{U}j}(t)+\widetilde{D}_{\mathrm{U}j}\vec{u}_{\mathrm{U}j}(t)+\widetilde{F}_{\mathrm{U}2j}\vec{\omega}_{\mathrm{U}j}(t)\end{cases}\tag{27}$$

where $x_{\mathrm{U}j}=[\xi_{dj}\ \xi_{qj}]^{\top}$, $y_{\mathrm{U}j}=[i^{*}_{dj}\ i^{*}_{qj}]^{\top}$, $\vec{\omega}_{\mathrm{U}j}=[u^{*}_{\mathrm{ref}dj}\ u^{*}_{\mathrm{ref}qj}]^{\top}$, $\vec{u}_{\mathrm{U}j}=[i_{dj}\ i_{qj}\ u_{\mathrm{C}dj}\ u_{\mathrm{C}qj}\ i_{gdj}\ i_{gqj}]^{\top}$.

$$\widetilde{A}_{\mathrm{U}j}=\begin{bmatrix}0&0\\0&0\end{bmatrix},\ \widetilde{F}_{\mathrm{U}1j}=\begin{bmatrix}1&0\\0&1\end{bmatrix},\ \widetilde{F}_{\mathrm{U}2j}=\begin{bmatrix}k_{\mathrm{v}}&0\\0&k_{\mathrm{v}}\end{bmatrix},$$

$$\widetilde{B}_{\mathrm{U}j}=\begin{bmatrix}0_{1\times2}&-1&0&0_{1\times2}\\0_{1\times2}&0&-1&0_{1\times2}\end{bmatrix},\ \widetilde{C}_{\mathrm{U}j}=\begin{bmatrix}2k_{\mathrm{vr}}\omega_{\mathrm{r}}&0\\0&2k_{\mathrm{vr}}\omega_{\mathrm{r}}\end{bmatrix},$$

$$\widetilde{D}_{\mathrm{U}j}=\begin{bmatrix}0_{1\times2}&-k_{\mathrm{v}}&-\omega^{*}C_{\mathrm{f}j}&1&0\\0_{1\times2}&\omega^{*}C_{\mathrm{f}j}&-k_{\mathrm{v}}&0&1\end{bmatrix}.$$

Similarly, the current error dynamics are defined as $\mathrm{d}\vartheta_{dj}/\mathrm{d}t=i^{*}_{dj}-i_{dj}$, $\mathrm{d}\vartheta_{dj}/\mathrm{d}t=i^{*}_{qj}-i_{qj}$. The state space equation of the current controller can be expressed as

$$\begin{cases}\dot{x}_{\mathrm{C}j}(t)=\widetilde{A}_{\mathrm{C}j}x_{\mathrm{C}j}(t)+\widetilde{B}_{\mathrm{C}j}\vec{u}_{\mathrm{C}j}(t)+\widetilde{F}_{\mathrm{C}1j}\vec{\omega}_{\mathrm{C}j}(t)\\ y_{\mathrm{C}j}(t)=\widetilde{C}_{\mathrm{C}j}x_{\mathrm{C}j}(t)+\widetilde{D}_{\mathrm{C}j}\vec{u}_{\mathrm{C}j}(t)+\widetilde{F}_{\mathrm{C}2j}\vec{\omega}_{\mathrm{C}j}(t)\end{cases}\tag{28}$$

where $x_{\mathrm{C}j}=[\vartheta_{dj}\ \vartheta_{qj}]^{\top}$, $y_{\mathrm{C}j}=[u^{*}_{dj}\ u^{*}_{qj}]^{\top}$, $\vec{\omega}_{\mathrm{C}j}=[i^{*}_{dj}\ i^{*}_{qj}]^{\top}$, $\vec{u}_{\mathrm{C}j}=[i_{dj}\ i_{qj}\ u_{\mathrm{C}dj}\ u_{\mathrm{C}qj}\ i_{gdj}\ i_{gqj}]^{\top}$.

$$\widetilde{A}_{\mathrm{C}j}=\begin{bmatrix}0&0\\0&0\end{bmatrix},\ \widetilde{F}_{\mathrm{C}1j}=\begin{bmatrix}1&0\\0&1\end{bmatrix},\ \widetilde{F}_{\mathrm{C}2j}=\begin{bmatrix}k_{\mathrm{c}}&0\\0&k_{\mathrm{c}}\end{bmatrix},$$

$$\widetilde{B}_{\mathrm{C}j}=\begin{bmatrix}-1&0&0_{1\times4}\\0&-1&0_{1\times4}\end{bmatrix},\ \widetilde{C}_{\mathrm{C}j}=\begin{bmatrix}2k_{\mathrm{cr}}\omega_{\mathrm{r}}&0\\0&2k_{\mathrm{cr}}\omega_{\mathrm{r}}\end{bmatrix},$$

$$\widetilde{D}_{\mathrm{C}j}=\begin{bmatrix}-k_{\mathrm{c}}&-\omega^{*}L_{\mathrm{f}j}&1&0&0_{1\times2}\\\omega^{*}L_{\mathrm{f}j}&-k_{\mathrm{c}}&0&1&0_{1\times2}\end{bmatrix}.$$

Combining (21)–(28), the state-space model of the overall PCS is developed as

$$\dot{\vec{x}}_j(t)=\hat{A}_j\vec{x}_j(t)+\hat{B}_j\vec{u}_j(t)+\hat{B}_{\mathrm{cur}j}\vec{u}_{\mathrm{cur}j}(t)+\Delta_{\mathrm{ref}}\tag{29}$$

where variables and coefficient matrices are defined in (30).

$$\vec{x}_j=[i_{dj}\ i_{qj}\ u_{\mathrm{C}dj}\ u_{\mathrm{C}qj}\ i_{\mathrm{g}dj}\ i_{\mathrm{g}qj}\ \hat{\delta}_j\ P^{+}_j\ Q^{+}_j\ I_{gdj}\ I_{gqj}\ \sigma_{dj}\ \sigma_{qj}\ \varrho_{dj}\ \varrho_{qj}\ \phi_{dj}\ \phi_{qj}\ \bar{\sigma}_{dj}\ \bar{\sigma}_{qj}\ \xi_{dj}\ \xi_{qj}\ \vartheta_{dj}\ \vartheta_{qj}\ \Xi^{\mathrm{z}}_j]^{\top},$$

$$\vec{u}_j=[\bar{u}_{\mathrm{g}dj}\ \bar{u}_{\mathrm{g}qj}\ \bar{i}_{\mathrm{g}dj}\ \bar{i}_{\mathrm{g}qj}\ i^{\mathrm{z}}_{\mathrm{g}j}]^{\top},\ \vec{u}_{\mathrm{cur}j}=[u_{\mathrm{g}dj}\ u_{\mathrm{g}qj}\ \bar{i}_{\mathrm{g}dk}\ \bar{i}_{\mathrm{g}qk}]^{\top},$$

$$\hat{A}_j=\begin{bmatrix}\alpha&\beta\widetilde{C}'^{\square}_{\mathrm{RD}j}&-\beta\widetilde{C}_{\mathrm{V}1j}&\beta(\widetilde{C}'^{\square}_{\mathrm{R}j}+\widetilde{C}'^{\square}_{\mathrm{R}j})&\beta\widetilde{C}_{\mathrm{CS}j}&\widetilde{B}_{\mathrm{LCL}1j}\widetilde{F}_{\mathrm{C}2j}\widetilde{C}_{\mathrm{U}j}&\widetilde{B}_{\mathrm{LCL}1j}\widetilde{C}_{\mathrm{C}j}&0\\ \widetilde{B}_{\mathrm{RD}j}&\widetilde{A}_{\mathrm{RD}j}&0_{3\times15}&&&&&\\ \widetilde{B}_{\mathrm{V}1j}&0_{2\times3}&\widetilde{A}_{\mathrm{V}1j}&0_{2\times13}&&&&\\ \widetilde{B}'^{\square}_{\mathrm{R}j}&0_{6\times5}&&\widetilde{A}_{\mathrm{R}j}&0_{6\times7}&&&\\ 0_{2\times17}&&&&\widetilde{A}_{\mathrm{CS}j}&0_{2\times5}&&\\ \widetilde{B}_{\mathrm{U}j}+\widetilde{F}_{\mathrm{U}1j}\widetilde{D}'^{\square}_{\mathrm{R}j}&\widetilde{F}_{\mathrm{U}1j}\widetilde{C}'^{\square}_{\mathrm{RD}j}&-\widetilde{F}_{\mathrm{U}1j}\widetilde{C}_{\mathrm{V}1j}&\widetilde{F}_{\mathrm{U}1j}(\widetilde{C}'^{\square}_{\mathrm{R}j}+\widetilde{C}'^{\square}_{\mathrm{R}j})&\widetilde{F}_{\mathrm{U}1j}\widetilde{C}_{\mathrm{CS}j}&\widetilde{A}_{\mathrm{U}j}&0_{2\times3}&\\ \widetilde{B}_{\mathrm{C}j}+\widetilde{F}_{\mathrm{C}1j}\widetilde{F}_{\mathrm{U}2j}\widetilde{D}'^{\square}_{\mathrm{R}j}&\widetilde{F}_{\mathrm{C}1j}\widetilde{F}_{\mathrm{U}2j}\widetilde{C}'^{\square}_{\mathrm{RD}j}&-\widetilde{F}_{\mathrm{C}1j}\widetilde{F}_{\mathrm{U}2j}\widetilde{C}_{\mathrm{V}1j}&\widetilde{F}_{\mathrm{C}1j}\widetilde{F}_{\mathrm{U}2j}(\widetilde{C}'^{\square}_{\mathrm{R}j}+\widetilde{C}'^{\square}_{\mathrm{R}j})&\widetilde{F}_{\mathrm{C}1j}\widetilde{F}_{\mathrm{U}2j}\widetilde{C}_{\mathrm{CS}j}&0_{2\times2}&\widetilde{A}_{\mathrm{C}j}&0\\ 0_{1\times23}&&&&&&&\widetilde{A}_{\mathrm{Z}j}\end{bmatrix},$$

$$\hat{B}_j=\begin{bmatrix}\beta(\widetilde{D}'^{\square}_{\mathrm{R}j}+\widetilde{D}_{\mathrm{CS}j})&0_{7\times5}&\widetilde{B}'^{\square}_{\mathrm{R}j}&\widetilde{B}_{\mathrm{CS}j}&0_{4\times5}&\widetilde{B}_{\mathrm{Z}j}\end{bmatrix}^{\top},\ \widetilde{B}_{\mathrm{cur}j}=\begin{bmatrix}\widetilde{B}_{\mathrm{LCL}2j}&0_{17\times2}\\0_{7\times2}&\widetilde{B}_{\mathrm{CS}k}\end{bmatrix},$$

$$\alpha=\widetilde{A}_{\mathrm{LCL}j}+\widetilde{B}_{\mathrm{LCL}1j}\widetilde{D}_{\mathrm{C}j}+\widetilde{B}_{\mathrm{LCL}1j}\widetilde{F}_{\mathrm{C}2j}\widetilde{D}_{\mathrm{U}j}+\beta\widetilde{D}'^{\square}_{\mathrm{R}j},\ \beta=\widetilde{B}_{\mathrm{LCL}1j}\widetilde{F}_{\mathrm{C}2j}\widetilde{F}_{\mathrm{U}2j}\tag{30}$$

The Lyapunov-based analysis is provided in the following part to verify the stability of the proposed approach.

Theorem 1: Given $\bar{c} > 0$ and a dynamic system $\dot{\vec{x}}_j = f(\vec{x}_j)$ composed of (29) under Assumption 1, if there exist $P_j > 0$ and $Q_j > 0$ such that $\Lambda^{\top} P_j + P_j \Lambda \leqslant -Q_j$, then the PCS is asymptotically stable when all states $\vec{x}_j$ are uniformly bounded.

Proof: Consider a Lyapunov function candidate as

$$V(\vec{x}_j) = \vec{x}_j^{\top} P_j \vec{x}_j \tag{31}$$

Taking the derivative of $V(\vec{x}_j)$, we have

$$\begin{aligned}
\dot{V}(\vec{x}_j) &= 2\,\vec{x}_j^{\top} P_j\,\dot{\vec{x}}_j \\
&= \vec{x}_j^{\top}[(\hat{A}_j + \hat{B}_j K_{1j} + \hat{B}_{\mathrm{cur}j}\, K_{2j})^{\top} P_j + \\
&\quad P_j(\hat{A}_j + \hat{B}_j K_{1j} + \hat{B}_{\mathrm{cur}j}\, K_{2j})]\vec{x}_j + 2\,\vec{x}_j^{\top} P_j \Delta_{\mathrm{ref}} \\
&= \vec{x}_j^{\top}(\Lambda^{\top} P_j + P_j \Lambda)\vec{x}_j + 2\,\vec{x}_j^{\top} P_j \Delta_{\mathrm{ref}} \\
&\leqslant \vec{x}_j^{\top}(-Q_j)\vec{x}_j + 2\,\vec{x}_j^{\top} P_j(-\bar{c})\vec{x}_j \\
&\leqslant -\tau_{\max}(Q_j)\|\vec{x}_j\|^2 - 2\tau_{\max}(P_j)\bar{c}\,\|\vec{x}_j\|^2 \\
&\leqslant -(\tau_{\max}(Q_j) + 2\bar{c}\tau_{\max}(P_j))\|\vec{x}_j\|^2 \\
&< 0
\end{aligned} \tag{32}$$

From (32), it reveals that the PCS (29) is asymptotically stable. The proof is completed.

Remark 3: The Lyapunov theory-based stability analysis proves the asymptotic stability of the PCS under the sense of large signals. Theorem 1 demonstrates the proposed largesignal model-based control approach can ensure Lyapunov stabilization of the PCS under unbalanced conditions and achieve the circulating current suppression. There exist the deviations of all variables tending to zero such that $\lim_{t\to\infty} U_{gdqj} \to U_{\mathrm{ref}dqj}$, $\lim_{t\to\infty} I_{gdqj} \to I_{\mathrm{ref}dqj}$, $\lim_{t\to\infty} U_{gdqj} \to U_{\mathrm{ref}dqj}$, $\lim_{t\to\infty} I_{zgj} \to I_{\mathrm{zref}j}$, $\lim_{t\to\infty} u_{Cdqj} \to u^{*}_{\mathrm{ref}dqj}$, and $\lim_{t\to\infty} i_{dqj} \to i^{*}_{dqj}$. That is to say, all state variables of the PCS can preciously track to their references under unbalanced conditions to realize stable operation.

IV. Experiment Results

A. Hardware-in-the-Loop Experiment Results

The proposed large-signal model-based control approach is implemented on hardware to validate the effectiveness and performance experimentally. The hardware-in-the-loop (HIL) experimental setup is illustrated in Fig. 4. The prototype inverter system uses PLECS RT Box1 Z-7030 to emulate the circuit characteristics, where the loads connected to the PCC consist of the unbalanced load and constant power load. The controller adopts Texas Instruments DSP (32-bit floatingpoint TMS320F28335) to drive IGBTs. The DSP Emulator (XDS100V3) is used for program download. The input channels of RT Box1 receive the digital signals PWM to drive the IGBTs and the output channels produce the analog signals (voltage, current, etc.). The waveforms are output to the oscilloscope (Tektronix MDO 3014 100MHz/4/2.5GS/s/10Mpoint). The

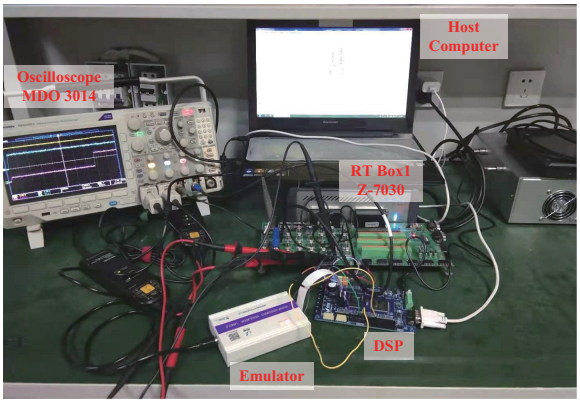


Fig. 4. Hardware-in-the-loop experimental setup.

TABLE I
Experimental Parameters

Parameter	Value
DC bus voltage, U_{dc}	400 V
Switching frequency, f_{s}	10 kHz
DC capacitor, C_{dc}	470 μF
Filter inductor1, $L_{\mathrm{f}j}$, $R_{\mathrm{f}j}$	2 mH, 0.61 Ω
Filter capacitor, $C_{\mathrm{f}j}$	15 μF
Filter inductor 2, L_{gj}, R_{gj}	1.3 mH, 0.642 Ω
Rated power, P_j^{*}, Q_j^{*}	18 kW, 0 Var
global reference angular frequency, ω_{ref}	314 rad/s
Cut-off frequency of LPF, ω_{c}	31.4 rad/s
Rated voltage, U^{*}	231 V
Droop coefficients, γ_j, ℓ_j	3e-5, 2e-4
Voltage gain, K_U	3
Initial VI values, R_0, C_0	0.15, 0.514
VI coefficients, μ, ν	1.3, 1.1
Estimation weight, λ	1.2
Droop controller gains, k_{drp}, k_{dri}	0.1, 100
Voltage controller gains, k_{v}, k_{vr}	0.2, 280.8
Current controller gains, k_{c}, k_{cr}	0.24, 500
Negative-sequence compensator gains, k_{up}, k_{ui}	4, 80
Negative-sequence compensator gains, k_{ip}, k_{ii}	4, 80
ZSCC controller gains, k_{z}, k_{zr}	0.08, 2.55
Current sharing gains, k_{cp}, k_{ci}	5, 400
Constant power load	50 W, 0 Var
Unbalanced load	10/20/40 Ω, 1 mH

experimental configurations are given in Table I.

1) Unbalanced voltage compensation performance case: To verify the performance of the proposed approach, the unbalanced voltage compensation example is investigated. Fig. 5 depicts the dynamic waveforms of the proposed approach with the unbalanced load. Stage 1 represents the state before the proposed approach is activated. Stage 2 represents the state after using the proposed approach. It is obvious from Fig. 5(a) that the three-phase voltage u_{abc} is unbalanced in Stage 1 and the VUF (based on IEEE Std. 936−1987) is 7.6%. At $t = t_1$, the proposed approach is activated. The VUF decreases to nearly 0.6%. The unbalanced voltage and voltage loss achieve effective compensation. The three phases are basically balanced due to VUF ≠ 0 in Stage 2. Note that based on IEEE Std. 1547, the VUF should be within 5%, namely, the VUF of the proposed approach (0.6%) is allowed.

Fig. 5(b) indicates the waveforms of the current and ZSCC.

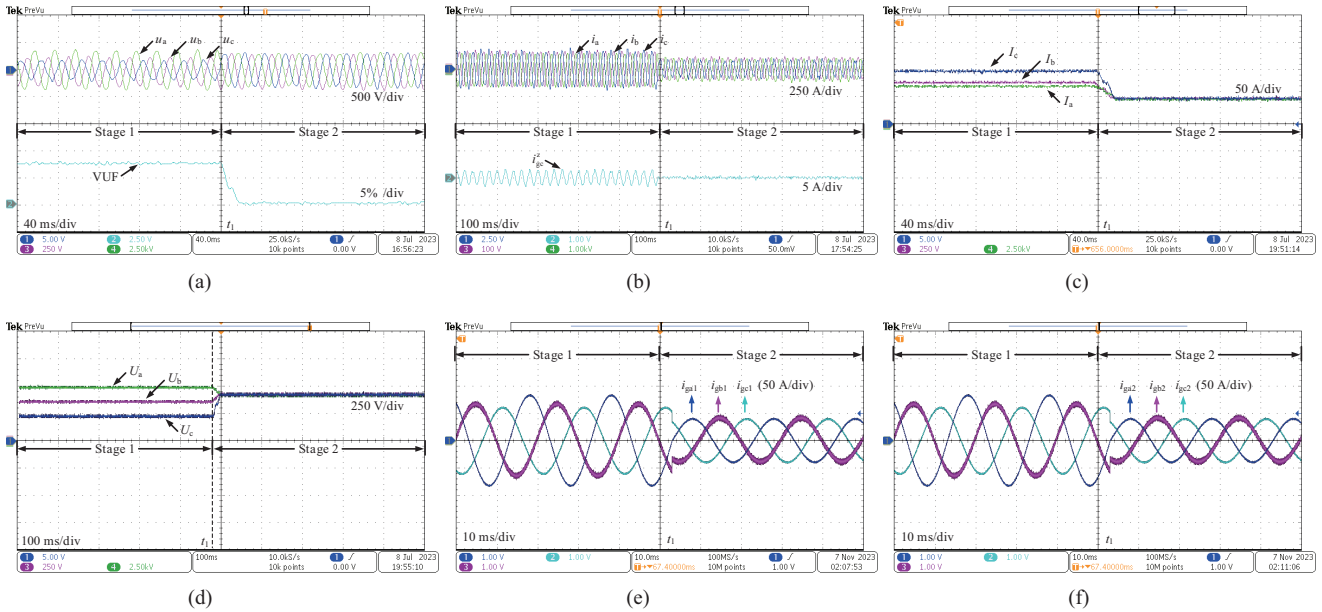


Fig. 5. Dynamic waveforms of unbalanced voltage compensation with the unbalanced load. (a) Three-phase bus voltage and VUF. (b) Three-phase bus current and ZSCC. (c) Bus current sharing. (d) Bus voltage balance. (e) Three-phase currents of inverter 1. (f) Three-phase currents of inverter 2.

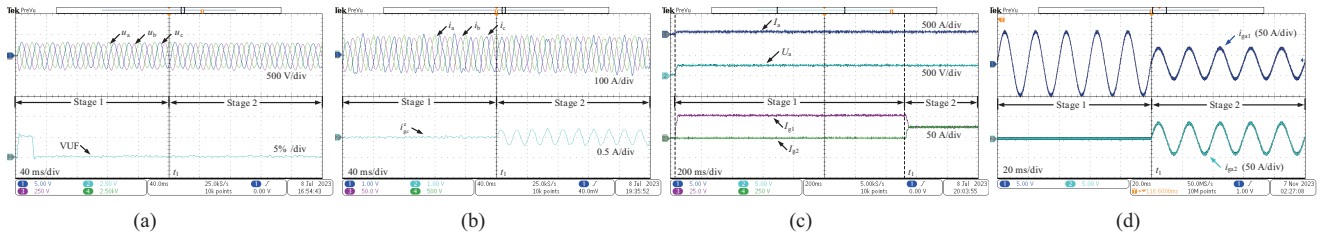


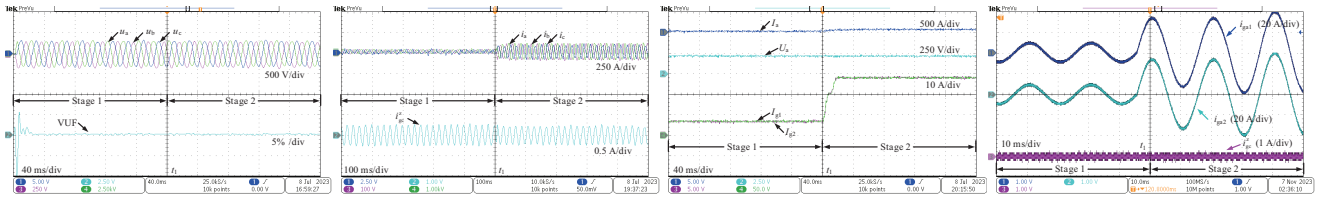
Fig. 6. Dynamic waveforms of plug-and-play performance. (a) Three-phase bus voltage and VUF. (b) Three-phase bus current and ZSCC. (c) RMSs of bus voltage, bus current, and two inverter currents. (d) Three-phase currents of inverter 1 and inverter 2.

Since the disturbances produced by filter parameters in the 0-axis are inevitable using the conventional method, the ZSCC cannot be fully eliminated. Feedforward control is used to offset these disturbance terms. It is clear that the ZSCC is significantly suppressed upon activation of the proposed approach (1.73 A → 0.49 A). Fig. 5(c) and (d) exhibit more visibly that the three-phase components are balanced and the system achieves stable operation. The reference voltage amplitude is 311 V under balanced conditions. It should be claimed that this example considers the equal line impedances of parallel branches.

2) Plug-and-play performance case: To test the plugand-play performance of PCSs, the proposed approach with the inverter switching example is implemented. The dynamic results are illustrated in Fig. 6. Stage 1 represents the state that one inverter is accessed into the system. Stage 2 represents the state that two parallel inverters are plugged into the system. In Fig. 6(a), when the system is initially operated, the proposed approach is activated and the VUF is 5.2%. The dynamic response is 31.8 ms. Then, the VUF decreases to around 0.48%. At $t = t_1$, the inverter 2 is plugged into the system. The VUF is still within the allowable standards. The Q-PR controllers with corresponding cut-off frequency are adopted to attenuate negative-sequence and zero-sequence components, therefore, three-phase symmetrical voltage and current (in Fig. 6(a) and (b)) are yielded.

In Stage 1, there exists no circulating loop in a single inverter, so the ZSCC is zero, as shown in Fig. 6(b). It can be noted that there is no high peak distortion. The ZSCC in Stage 2 reaches 0.48 A. It should be claimed that there exist the factors such as dead time and the difference of nonlinear devices making the ZSCC unable to completely zero. Fig. 6(c) exhibits the waveforms of RMSs of the bus voltage and current, and two inverter currents. It is clear that only inverter 1 supplies power in Stage 1. The positive-sequence voltage achieves the reference value (231 V) tracking, where the voltage deviations get compensated. In Stage 2, two inverters can share the load current well. The transient time is 18.7 ms. It turned out that the PCSs using the proposed approach have good steady-state and transient performance.

3) System performance with dynamic load change case: The dynamic waveforms of system performance with load change are exhibited in Fig. 7. Before Stage 1, the PSCs operate with the same load as the previous case. At $t = t_0$, a part of the load is cut off from the PSCs. The load change results in an increasing bus voltage and voltage transient unbalance. As can



(a) (b) (c) (d)

Fig. 7. Dynamic waveforms of system performance with load change. (a) Three-phase bus voltage and VUF. (b) Three-phase bus current and ZSCC. (c) RMSs of bus voltage, bus current, and two inverter currents. (d) Three-phase currents of inverter 1 and inverter 2, and ZSCC.

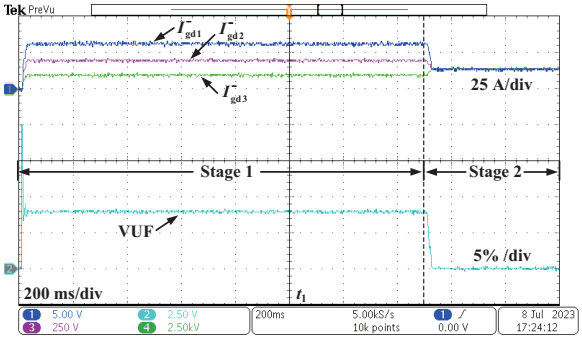


Fig. 8. Dynamic waveforms of negative-sequence *d*-axis currents.

be observed from Fig. 7(a), the three-phase voltage maintains balance in Stage 1 and the VUF is 0.34%. The transient time of the voltage balance is 24.2 ms. The PCSs operate stably and complete the unbalanced voltage and voltage drop compensation. At $t = t_1$, the load is reconnected to the PSCs. The voltage balanced factor is guaranteed. When the load increases at t_1, the unbalanced current is generated. However, the three phases of the current reach balance in 40 ms after t_1, as shown in Fig. 7(b). Fig. 7(c) depicts the waveforms of RMSs of the voltages and currents. It can be observed that after the load increases, both branch current and bus current increase respectively. The bus voltage still remains stable at the reference setting. The Q-PR control achieves zero steady-state error tracking of the bus voltage in a wide frequency band. Additionally, the VI presents capacitive characteristics, which is conducive to the suppression of higher harmonics. As seen from two output currents, the currentsharing effects in both stages are satisfactory and exact.

4) Negative-sequence current sharing performance case: To validate the negative-sequence current sharing performance using the proposed approach, three parallel inverters are applied to the PSCs for experimental implementation. In this case, the line impedances of three inverters are set to be different, with $0.12 + j0.002\ \Omega$ for inverter 1, $0.12 + j0.004\ \Omega$ for inverter 2, and $0.12 + j0.006\ \Omega$ for inverter 3, respectively. Fig. 8 shows the dynamic waveforms of the negative sequence *d*-axis currents. Stage 1 indicates the state before the proposed approach is activated. Stage 2 indicates the state after using the proposed approach. It is clear that due to the difference between line impedances, the negative-sequence currents of the different parallel inverters cannot be effectively shared in Stage 1 using the conventional approach. It takes 41 ms to stabilize. The bus VUF reaches 8%. At $t = t_1$, the proposed approach is activated. The VUF is reduced to 0.15%. It takes 160 ms for three negative-sequence d-axis currents to track the mean value of the negative-sequence current $\bar{i}_{gj}^{-}$ accurately. It reveals that the proposed approach can accomplish the sharing of the current d^{-} components.

5) Multiparalleled case: To verify the validity of the proposed approach for multiparalleled inverter applications, the proposed approach is tested with three-paralleled inverters. Dynamic waveforms of ZSCC and three-phase currents in three-paralleled inverters are presented in Fig. 9. It is evident that the three phases of the output current exhibit equal amplitudes, with phase differences measuring 120 degrees. Moreover, the three-paralleled inverters using the proposed approach achieve effective ZSCC suppression with different line impedances. The output results demonstrate that the system with the proposed approach attains the three-phase balance and improves the current quality.

B. Experiment Results

To validate the effectiveness of the proposed approach, the experiments are implemented with two parallel inverters. The experimental configuration is illustrated in Fig. 10. The capacity of the prototype system is 1.2 kW, where the range of switching frequency is [15, 24] kHz. The IGBT modules adopt FGA40N65SMD and the capacity of the DC capacitor is 470 μF. The DC source uses the ITECH 6513 (IT6513 200V/60A/1800W) for power supply and the local load uses ITECH electronic load (IT8514B+ 500V/60A/1500W). The waveforms are output to the oscilloscope (Tektronix MDO 3024 200MHz/4/2.5GS/s/10Mpoint).

Fig. 11 illustrates the dynamic waveforms of threephase currents with different line impedances ($L_1 = 2$ mH, $L_2 = 4$ mH, $L_3 = 3$ mH), with $k_z = 1.2$, $k_z = 0.08$. As depicted in Fig. 11(a), there are serious oscillations in the output current waveforms, indicating system instability. The experimental waveforms with the designed proportional gain are presented in Fig. 11(b). It is evident that the output current waveforms are stable and smooth. It shows that the proposed controller effectively reduces AC interference and ensures system stabilization. The results reveal the validation of the stability analysis under unbalanced conditions using the proposed approach.

The dynamic waveforms of three-phase currents with un-

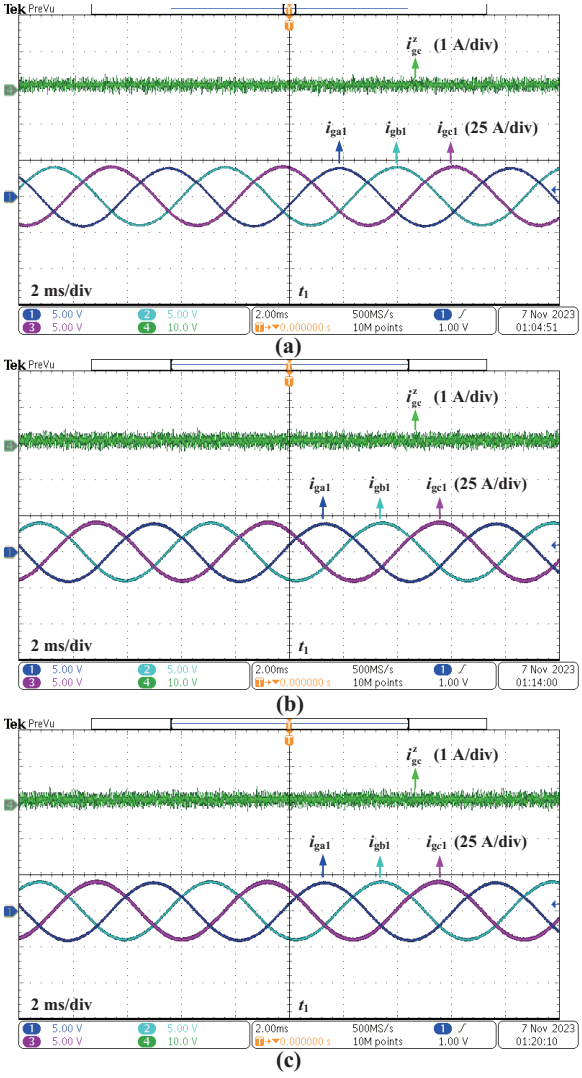


Fig. 9. Dynamic waveforms of ZSCC and three-phase currents with different line impedances. (a) Inverter 1. (b) Inverter 2. (c) Inverter 3.

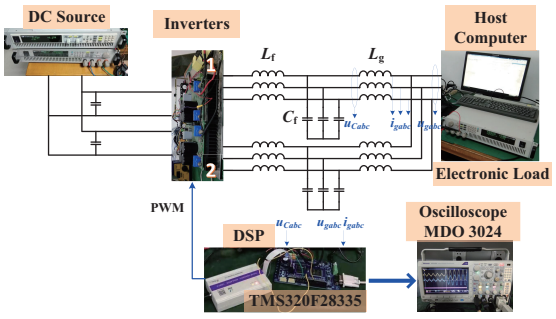


Fig. 10. Experimental configuration.

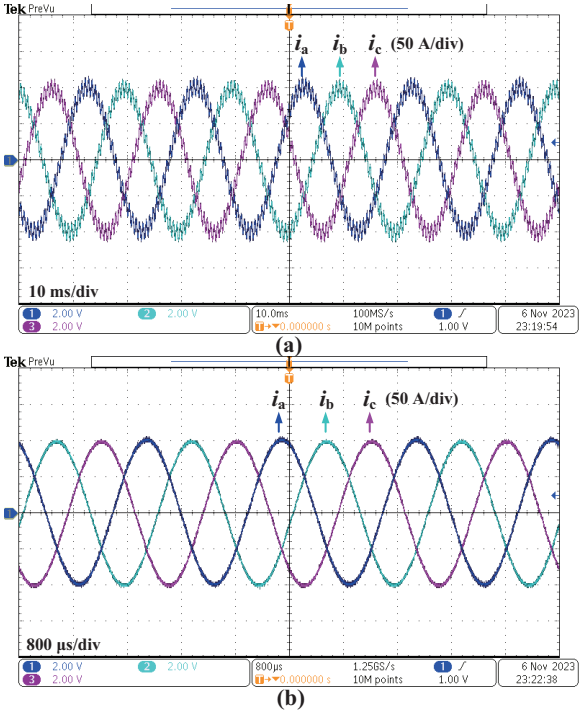


Fig. 11. Dynamic waveforms of three-phase currents with L_1 = 2 mH, L_2 = 4 mH, L_3 = 3 mH. (a) k_z = 1.2. (b) k_z = 0.08.

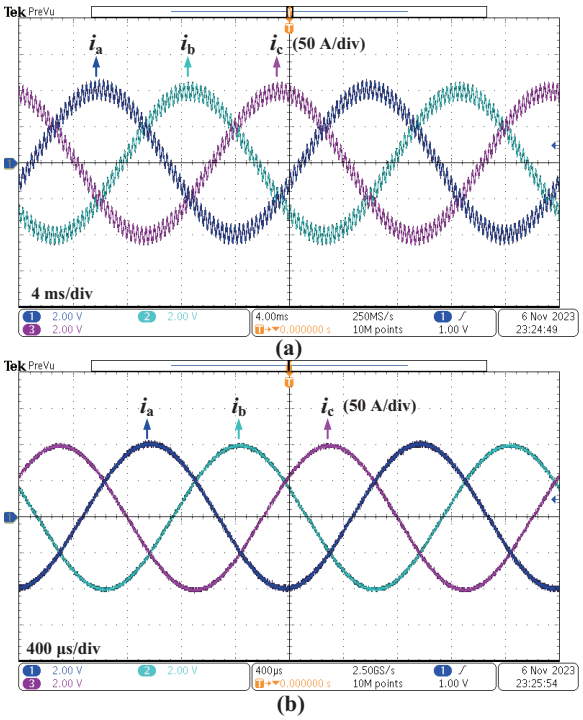


Fig. 12. Dynamic waveforms of three-phase currents with unbalanced load change. (a) k_z = 1.2. (b) k_z = 0.08.

balanced load change (from 20/20/20 Ω, 1 mH to 10/20/40 Ω, 1 mH) are illustrated in Fig. 12, with k_z = 1.2, k_z = 0.08. It can be observed from Fig. 12(a) that the three-phase current oscillations are apparent and the system output is unstable. Subsequently, the output results of the system with the designed control parameter are shown in Fig. 12(b) under the same conditions. It shows that the system output is stable, which has the same results as those in Fig. 11(b).

The dynamic waveforms of the output currents and ZSCC for two inverters with different line impedances (L_1 = 2 mH,

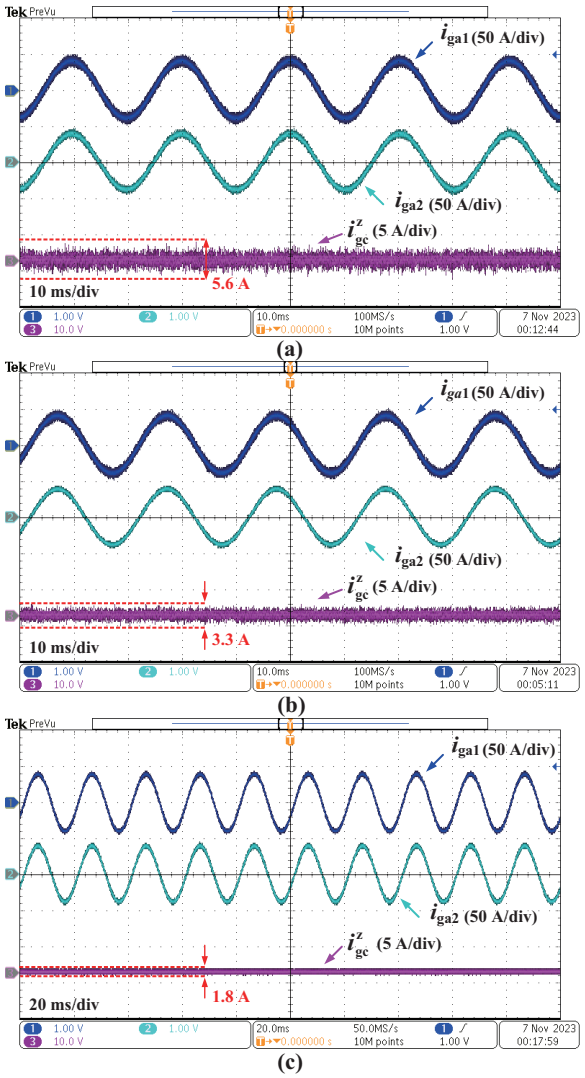


Fig. 13. Dynamic waveforms of output currents and ZSCC for two inverters. (a) PI control. (b) Method in [24]. (c) Proposed control approach.

L_2 = 4 mH, L_3 = 3 mH) are presented in Fig. 13. The ZSCC is caused by the filter parameters and unequal inductors. As observed in Fig. 13(a), the ZSCC cannot be effectively suppressed by the PI controller, resulting in a peak-to-peak value of 5.6 A. Apparent oscillations are presented in the output currents of the two inverters. The VI control can eliminate the difference in system output impedance. The VI method in [24] enhances the suppression effect of the PSCC and improves the current quality, as illustrated in Fig. 13(b). However, the ZSCC in Fig. 13(c) is significantly attenuated by the proposed approach and the system has improved output performance, while the peak-to-peak value of the ZSCC is notably reduced from 3.3 A to 1.8 A.

Dynamic waveforms of ZSCC and three-phase currents for inverter 1 and inverter 2 are exhibited in Fig. 14. It is observed that the current distortions and oscillations are apparently alleviated and the higher quality symmetrical three-phase currents are obtained, which reveals that the proposed controller can effectively attenuate the unbalanced components.

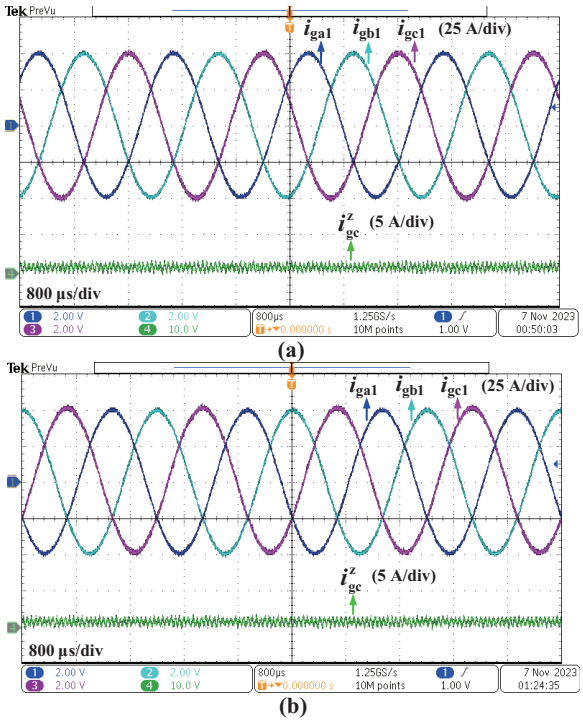


Fig. 14. Dynamic waveforms of ZSCC and three-phase currents using the proposed approach. (a) Inverter 1. (b) Inverter 2.

V. Conclusion

In this paper, a large-signal model-based circulating current control approach was proposed to achieve circulating current suppression and voltage compensation of the PCS under unbalanced conditions. The adaptive capacitive VI was developed based on the change of the current difference among different inverters to effectively mitigate the PSCC. The secondary control signal was designed and combined with the positivesequence voltage output to modify the voltage reference and compensate for the unbalanced voltage. Subsequently, a ZSCC controller was proposed by incorporating the Q-PR controller and the feedforward term to achieve the ZSCC suppression and the elimination of disturbances caused by the filter capacitor. Furthermore, the PCS with the proposed approach exhibited good dynamic performance and satisfied the requirements of plug and play. Extensive experimental cases demonstrated the effectiveness of the proposed approach.

References

[1] Y. Li, Y. Gu, and T. C. Green, "Revisiting grid-forming and grid following inverters: A duality theory," in *IEEE Transactions on Power Systems*, vol. 37, no. 6, pp. 4541–4554, Nov. 2022.

[2] T. Liu and X. Wang, "Unified voltage control for grid-forming inverters," in *IEEE Transactions on Industrial Electronics*, vol. 71, no. 3, pp. 2578–2589, Mar. 2024.

[3] M. Mao, C. Qian, and Y. Ding, "Decentralized coordination power control for islanding microgrid based on PV/BES-VSG," in *CPSS Transactions on Power Electronics and Applications*, vol. 3, no. 1, pp. 14–24, 2018.

[4] Q. Wang, W. Qin, X. Han, P. Wang, L. Wang, and Y. Zhang, "Robustness evaluation for harmonic suppression of LCL-type converter based on converter-side current feedback strategy under weak and distorted grid," in *CPSS Transactions on Power Electronics and Applications*, vol. 6, no. 2, pp. 166–177, Jun. 2021.

[5] Y. Luo, M. A. Awal, W. Yu, and I. Husain, "FPGA implementation for rapid prototyping of high performance voltage source inverters," in *CPSS Transactions on Power Electronics and Applications*, vol. 6, no. 4, pp. 320–331, Dec. 2021.

[6] M. M. Shabestary and Y. A.-R. I. Mohamed, "Maximum asymmetrical support in parallel-operated grid-interactive smart inverters," in *IEEE Transactions on Sustainable Energy*, vol. 13, no. 1, pp. 14–30, Jan. 2022.

[7] O. Babayomi, Z. Li, and Z. Zhang, "Distributed secondary frequency and voltage control of parallel-connected VSCs in microgrids: A predictive VSG-based solution," in *CPSS Transactions on Power Electronics and Applications*, vol. 5, no. 4, pp. 342–351, Dec. 2020.

[8] M. S. Golsorkhi, D. J. Hill, and M. Baharizadeh, "A secondary control method for voltage unbalance compensation and accurate load sharing in networked microgrids," in *IEEE Transactions on Smart Grid*, vol. 12, no. 4, pp. 2822–2833, Jul. 2021.

[9] F. Wang, Y. Wang, Q. Gao, C. Wang, and Y. Liu, "A control strategy for suppressing circulating currents in parallel-connected PMSM drives with individual DC links," in *IEEE Transactions on Power Electronics*, vol. 31, no. 2, pp. 1680–1691, Feb. 2016.

[10] H. A. Porkia, J. Adabi, and F. Zare, "Elimination of circulating current in a parallel PWM rectifier using an interface circuit," in *IEEE Transactions on Power Electronics*, vol. 37, no. 1, pp. 264–273, Jan. 2022.

[11] W. Jiang, Y. Gao, B. Xiao, J. Wang, X. Ding, and L. Wang, "Suppression of high-frequency circulating current caused by asynchronous carriers for parallel three-phase grid-connected converters," in *IEEE Transactions on Industrial Electronics*, vol. 65, no. 2, pp. 1031–1040, Feb. 2018.

[12] H. Xu, L. Xu, C. Li, K. Wang, Z. Zheng, and Y. Li, "Improved interleaved discontinuous PWM for zero-sequence circulating current reduction in three-phase paralleled converters," in *IEEE Transactions on Industrial Electronics*, vol. 68, no. 9, pp. 8676–8686, Sept. 2021.

[13] Z. Liang, X. Lin, X. Qiao, Y. Kang, and B. Gao, "A coordinated strategy providing zero-sequence circulating current suppression and neutral-point potential balancing in two parallel three-level converters," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 1, pp. 363–376, Mar. 2018.

[14] J. Wang, F. Hu, W. Jiang, W. Wang, and Y. Gao, "Investigation of zero sequence circulating current suppression for parallel three-phase grid-connected converters without communication," in *IEEE Transactions on Industrial Electronics*, vol. 65, no. 10, pp. 7620–7629, Oct. 2018.

[15] C. Zhang, Z. Wang, X. Xing, X. Li, and X. Liu, "Modeling and suppression of circulating currents among parallel single-phase three-level grid-tied inverters," in *IEEE Transactions on Industrial Electronics*, vol. 69, no. 12, pp. 12967–12979, Dec. 2022.

[16] J. Wang, X. Han, H. Ma, and Z. Bai, "Analysis and injection control of circulating current for modular multilevel converters," in *IEEE Transactions on Industrial Electronics*, vol. 66, no. 3, pp. 2280–2290, Mar. 2019.

[17] W. Jiang, W. Ma, J. Wang, W. Wang, X. Zhang, and L. Wang, "Suppression of zero sequence circulating current for parallel three-phase grid-connected converters using hybrid modulation strategy," in *IEEE Transactions on Industrial Electronics*, vol. 65, no. 4, pp. 3017–3026, Apr. 2018.

[18] X. Xing, C. Zhang, A. Chen, H. Geng, and C. Qin, "Deadbeat control strategy for circulating current suppression in multi paralleled three-level inverters," in *IEEE Transactions on Industrial Electronics*, vol. 65, no. 8, pp. 6239–6249, Aug. 2018.

[19] X. Zhang, W. Li, Y. Xiao, G. Wang, and D. Xu, "Analysis and suppression of circulating current caused by carrier phase difference in parallel voltage source inverters with SVPWM," in *IEEE Transactions on Power Electronics*, vol. 33, no. 12, pp. 11007–11020, Dec. 2018.

[20] B. Wei, J. M. Guerrero, J. C. Vásquez, and X. Guo, "A circulating current suppression method for parallel-connected voltage-source inverters with common DC and AC buses," in *IEEE Transactions on Industry Applications*, vol. 53, no. 4, pp. 3758–3769, Jul.-Aug. 2017.

[21] M. Castilla, M. Velasco, J. Miret, Á. Borrell, and R. Guzmán, "Control scheme for negative-sequence voltage compensation and current sharing in inverter based grid-connected microgrids," in *IEEE Transactions on Power Electronics*, vol. 37, no. 6, pp. 6556–6567, Jun. 2022.

[22] C. Qin, C. Zhang, A. Chen, X. Xing, and G. Zhang, "Circulating current suppression for parallel three-level inverters under unbalanced operating conditions," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 1, pp. 480–492, Mar. 2019.

[23] A. Vijay, N. Parth, S. Doolla, and M. C. Chandorkar, "An adaptive virtual impedance control for improving power sharing among inverters in islanded AC microgrids," in *IEEE Transactions on Smart Grid*, vol. 12, no. 4, pp. 2991–3003, Jul. 2021.

[24] B. Zhang, X. Han, C. Ren, D. Zhang, L. Wang, and T. Song, "Circulating current suppression method with adaptive virtual impedance for multi-bidirectional power converters under unbalanced conditions," in *CSEE Journal of Power and Energy Systems*, vol. 9, no. 1, pp. 77–87, Jan. 2023.

[25] M. Aquib, A. S. Vijay, S. Doolla, and M. C. Chandorkar, "On circulating current mitigation for modular UPS/inverters," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 11, no. 1, pp. 1179–1190, Feb. 2023.

[26] M. Zhang, B. Song, and J. Wang, "Circulating current control strategy based on equivalent feeder for parallel inverters in islanded microgrid," in *IEEE Transactions on Power Systems*, vol. 34, no. 1, pp. 595–605, Jan. 2019.

[27] Y. Huang, F. Chen, D. Wang, S. Zhang, G. Zhu, and K. Zhou, "Small signal modeling and interaction analysis of multi-VSCs system connected to weak grid," in *CPSS Transactions on Power Electronics and Applications*, vol. 8, no. 1, pp. 74–86, Mar. 2023.

[28] S. P. Nandanoori, S. Kundu, W. Du, F. K. Tuffner, and K. P. Schneider, "Distributed small-signal stability conditions for inverter-based unbalanced microgrids," in *IEEE Transactions on Power Systems*, vol. 35, no. 5, pp. 3981–3990, Sept. 2020.

[29] R. Wang, Q. Sun, D. Ma, and Z. Liu, "The small-signal stability analysis of the droop-controlled converter in electromagnetic timescale," in *IEEE Transactions on Sustainable Energy*, vol. 10, no. 3, pp. 1459–1469, Jul. 2019.

[30] Y. Peng, Z. Shuai, J. M. Guerrero, Y. Li, A. Luo, and Z. J. Shen, "Performance improvement of the unbalanced voltage compensation in islanded microgrid based on small-signal analysis," in *IEEE Transactions on Industrial Electronics*, vol. 67, no. 7, pp. 5531–5542, Jul. 2020.

[31] A. Akhavan, S. Golestan, J. C. Vasquez, and J. M. Guerrero, "Control and stability analysis of current-controlled grid-connected inverters in asymmetrical grids," in *IEEE Transactions on Power Electronics*, vol. 37, no. 12, pp. 14252–14264, Dec. 2022.

[32] Q. Taoufik, H. Wu, X. Wang, and I. Colak, "Variable virtual impedance based overcurrent protection for grid-forming inverters: Small-signal, large-signal analysis and improvement," in *IEEE Transactions on Smart Grid*, vol. 14, no. 5, pp. 3324–3336, Sept. 2023.

[33] Y. Du, Y. Men, L. Ding, and X. Lu, "Large-signal stability analysis for inverter-based dynamic microgrids reconfiguration," in *IEEE Transactions on Smart Grid*, vol. 14, no. 2, pp. 836–852, Mar. 2023.

[34] J. Lu, B. Zhang, X. Hou, and J. M. Guerrero, "A distributed control strategy for unbalanced voltage compensation in islanded AC microgrids without continuous communication," in *IEEE Transactions on Industrial Electronics*, vol. 70, no. 3, pp. 2628–2638, Mar. 2023.

[35] M. Kabalan, P. Singh, and D. Niebur, "A design and optimization tool for inverter-based microgrids using large-signal nonlinear analysis," in *IEEE Transactions on Smart Grid*, vol. 10, no. 4, pp. 4566–4576, Jul. 2019.

[36] Y. Jin, Q. Xiao, H. Jia, Y. Mu, Y. Ji, R. Teodorescu, and T. Dragičević, "A dual-layer back-stepping control method for Lyapunov stability in modular multilevel converter based STATCOM," in *IEEE Transactions on Industrial Electronics*, vol. 69, no. 3, pp. 2166–2179, Mar. 2022.

[37] X. Xiong, X. Wang, D. Liu, F. Blaabjerg, and C. Zhao, "Common-mode insertion indices compensation with capacitor voltages feedforward to suppress circulating current of MMCs," in *CPSS Transactions on Power*

Electronics and Applications, vol. 5, no. 2, pp. 103–113, Jun. 2020.

[38] K. Sun, X. Lin, Y. Li, Y. Gao, and L. Zhang, "Improved modulation mechanism of parallel-operated t-type three-level PWM rectifiers for neutral-point potential balancing and circulating current suppression," in *IEEE Transactions on Power Electronics*, vol. 33, no. 9, pp. 7466–7479, Sept. 2018.

[39] C. V. S. Anirudh and V. S. S. Kumar, "Estimation of symmetrical component phasors and frequency of three-phase voltage signals using transformations," in *IEEE Transactions on Power Delivery*, vol. 38, no. 1, pp. 189–199, Feb. 2023.

[40] J. M. Alcala, M. Castilla, L. G. de Vicuña, J. Miret, and J. C. Vasquez, "Virtual impedance loop for droop-controlled single-phase parallel inverters using a second-order general-integrator scheme," in *IEEE Transactions on Power Electronics*, vol. 25, no. 12, pp. 2993–3002, Dec. 2010.

[41] Q.-C. Zhong and Y. Zeng, "Control of inverters via a virtual capacitor to achieve capacitive output impedance," in *IEEE Transactions on Power Electronics*, vol. 29, no. 10, pp. 5568–5578, Oct. 2014.

[42] A. Micallef, M. Apap, C. Spiteri-Staines, and J. M. Guerrero, "Mitigation of harmonics in grid-connected and islanded microgrids via virtual admittances and impedances," in *IEEE Transactions on Smart Grid*, vol. 8, no. 2, pp. 651–661, Mar. 2017.

[43] T. Wang, H. Nian, Z. Q. Zhu, L. Ding, and B. Zhou, "Flexible compensation strategy for voltage source converter under unbalanced and harmonic condition based on a hybrid virtual impedance method," in *IEEE Transactions on Power Electronics*, vol. 33, no. 9, pp. 7656–7673, Sept. 2018.

[44] H.-J. Yoo, T.-T. Nguyen, and H.-M. Kim, "Consensus-based distributed coordination control of hybrid AC/DC microgrids," in *IEEE Transactions on Sustainable Energy*, vol. 11, no. 2, pp. 629–639, Apr. 2020.

Guangyu Song received the B.Sc. degree in electrical engineering from University of Jinan, Jinan, China, in 2018, and the M.Sc. degree in control engineering from Inner Mongolia University of Science & Technology, Baotou, China, in 2020. He is currently working toward Ph.D. degree in electrical engineering, Xi'an University of Technology, Xi'an, China. His research interests include hybrid energy storage systems, photovoltaic generation systems, power converter control, and microgrid control and stability.

Xinghua Liu received the B.S. degree from Jilin University, Changchun, China, in 2009; and the Ph.D. degree in automation from University of Science and Technology of China, Hefei, in 2014. From 2014 to 2015, he was invited as a visiting fellow at RMIT University in Melbourne, Australia. From 2015 to 2018, he was a Research Fellow at the School of Electrical and Electronic Engineering in Nanyang Technological University, Singapore. Dr. Liu has joined Xi'an University of Technology as a professor since September 2018. His research interest includes state estimation and control, intelligent systems, autonomous vehicles, cyberphysical systems, robotic systems, etc.

Gaoxi Xiao received the B.S. and M.S. degrees in applied mathematics from Xidian University, Xi'an, China, in 1991 and 1994, respectively, and the Ph.D. degree in computing from Hong Kong Polytechnic University, Hung Hom, Hong Kong, in 1998. He was an Assistant Lecturer with Xidian University from 1994 to 1995. He was a Postdoctoral Research Fellow with Polytechnic University, Brooklyn, NY, USA, in 1999, and a Visiting Scientist with the University of Texas at Dallas, TX, USA, from 1999 to 2001. In 2001, he joined the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore, where he is currently an Associate Professor. His research interests include complex systems and complex networks, communication networks, smart grids, and system resilience and risk regulation.

Liansong Xiong received the M.S. and Ph.D. degrees in electrical engineering from Xi'an Jiaotong University (XJTU), Xi'an, China, in 2012 and 2016, respectively. Since 2014, he has been with the School of E-learning, XJTU, as a part-time Faculty Member. In 2016, he joined the School of Automation, Nanjing Institute of Technology (NJIT), Nanjing, China, introduced in High-Level Academic Talent Plan of NJIT. From 2017 to 2019, he was with the Department of Electrical Engineering, The Hong Kong Polytechnic University (PolyU), Hong Kong, as a Research Associate. His current research interests include power quality, multilevel converter, renewable energy generation, and power systems stability.

Badong Chen received the Ph.D. degree in computer science and technology from Tsinghua University, Beijing, China, in 2008. He was a Post-Doctoral Researcher with Tsinghua University from 2008 to 2010 and a Post-Doctoral Associate with the Computational NeuroEngineering Laboratory, University of Florida, Gainesville, FL, USA, from 2010 to 2012. He was a Visiting Researcher Scientist with Nanyang Technological University, Singapore, in 2015. He is currently a Professor with the Institute of Artificial Intelligence and Robotics, Xi'an Jiaotong University, Xi'an, China. His research interests are in signal processing, machine learning, artificial intelligence, and robotics.

Peng Wang received the B.Sc. degree from Xi'an Jiaotong University, Xi'an, China, in 1978, the M.Sc. degree from Taiyuan University of Technology, Taiyuan, China, in 1987, and the M.Sc. and Ph.D. degrees from the University of Saskatchewan, Saskatoon, SK, Canada, in 1995 and 1998, respectively, all in electrical engineering. He is currently a Professor at Nanyang Technological University, Singapore. His research interests include Power system planning and operation, renewable energy planning, solar/electricity conversion system, power market and power system reliability analysis.