A Modular Multiport DC-DC Converter With MVDC Integration for Multiple DC Units

Xiaoquan ZHU, Jintao HOU, Ke JIN, and Bo ZHANG

***Abstract*—This paper deals with a modular input-independent output-series (IIOS) multiport dc power electronic transformer (DCPET), which can interface with multiple dc units (such as PV array, storage devices and dc loads) to the medium-voltage dc (MVdc) bus directly without extra low-voltage dc (LVdc) converters. Therefore, the number of converters and the system expend are greatly reduced and saved when compared with the conventional dc distributed network. Due to the input power of these dc units are different and the multiple modules are in serial connection on MVdc side, which will lead to the output voltage imbalance between submodules (SMs). By inserting a single LC branch between adjacent SMs to transfer the differential power in the proposed topology, SM output voltage mismatched problem can be solved. Moreover, all SM power switches can realize zero voltage switching (ZVS), which further ameliorates the system efficiency. Finally, the above theoretical analysis is verified by simulation and experimental results, and the proposed multiport PET can operate stably in different working states.**

***Index Terms*—DC distribution network, IIOS, modular dc-dc converter, power balancing.**

I. Introduction

With the advanced development of power electronic technologies and the vigorously exploitation of renewable energy, the concept of multiple distributed energy resources MVdc integration interface is becoming a research hotspot in dc distributed network fields [1]. And the integration of distributed photovoltaic energy into MVdc distribution network is an important form of new energy grid connection in the near future.

The traditional ac distribution network is undergoing significant changes due to the increasing connection of variable distributed dc units [2]. The use of a dc distribution network is a promising option for integrating distributed renewable energy resources, storage devices and dc loads, which can improve the transmission capacity and power conversion efficiency. A typical traditional MVdc distribution network topology is shown in Fig. 1, which includes two dc voltage buses (MVdc bus and LVdc bus). The power electronic transformer (PET) serves as a critical component, acting as a bridge between the MVdc and LVdc buses. Different from the traditional large volume, bulky weight and low-frequency transformers, PET can operate at high-frequency and possess the function of voltage level transformation, electrical isolation, fault handling and power flow control [3].

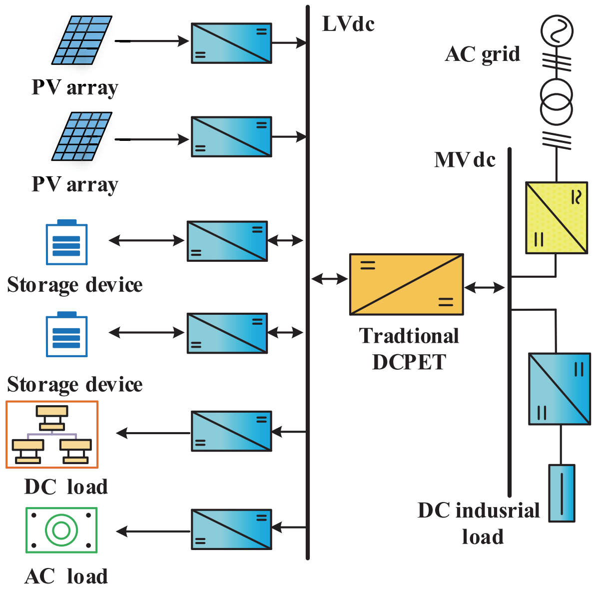


Fig. 1. DC distribution network with the traditional DCPET.

In the medium voltage ac-ac topology architecture, cascaded H-bridge modules can be used to connect different voltage levels. The input stage, isolation stage and output stage are typical structures of PET. In general, these three stages mainly include cascaded H-bridge modules, dual active bridge modules and three-phase inverter modules. Based on the ac-ac PET topology, various PET topologies have been proposed, such as: ac-ac PET [4]–[6] or hybrid PET [7]–[9], where the LVdc bus uses the additional dc-dc conversion to integrate distributed PV energy, dc loads and fuel cells. The PET proposed by [10] includes three stages: MVac-MVdc stage, MVdc-LVdc stage and LVdc-LVac stage. The MVdc-

---

Manuscript received July 8, 2023; revised September 20, 2023; accepted October 25, 2023. Date of publication March 30, 2024; date of current version November 1, 2023. This work was supported in part by the National Natural Science Foundation of China under Grant 62201256; in part by the Fundamental Research Funds for Central Universities under Grant 56XAA21057 and YAH19087; in part by the Postgraduate Research & Practice Innovation Program of NUAA under Grant xcxjh20220349. *(Corresponding author: Xiaoquan Zhu.)*

X. Zhu, J. Hou and K. Jin are with the College of Automation Engineering, Nanjing University of Aeronautics and Astronautics, Nanjing 210016, China (e-mail: ijruexq@nuaa.edu.cn; Hjintao@nuaa.edu.cn; jinke@nuaa.edu.cn).

B. Zhang is with the School of Electric Power, South China University of Technology, Guangzhou 510640, China (e-mail: epbzhang@ scut.edu.cn).

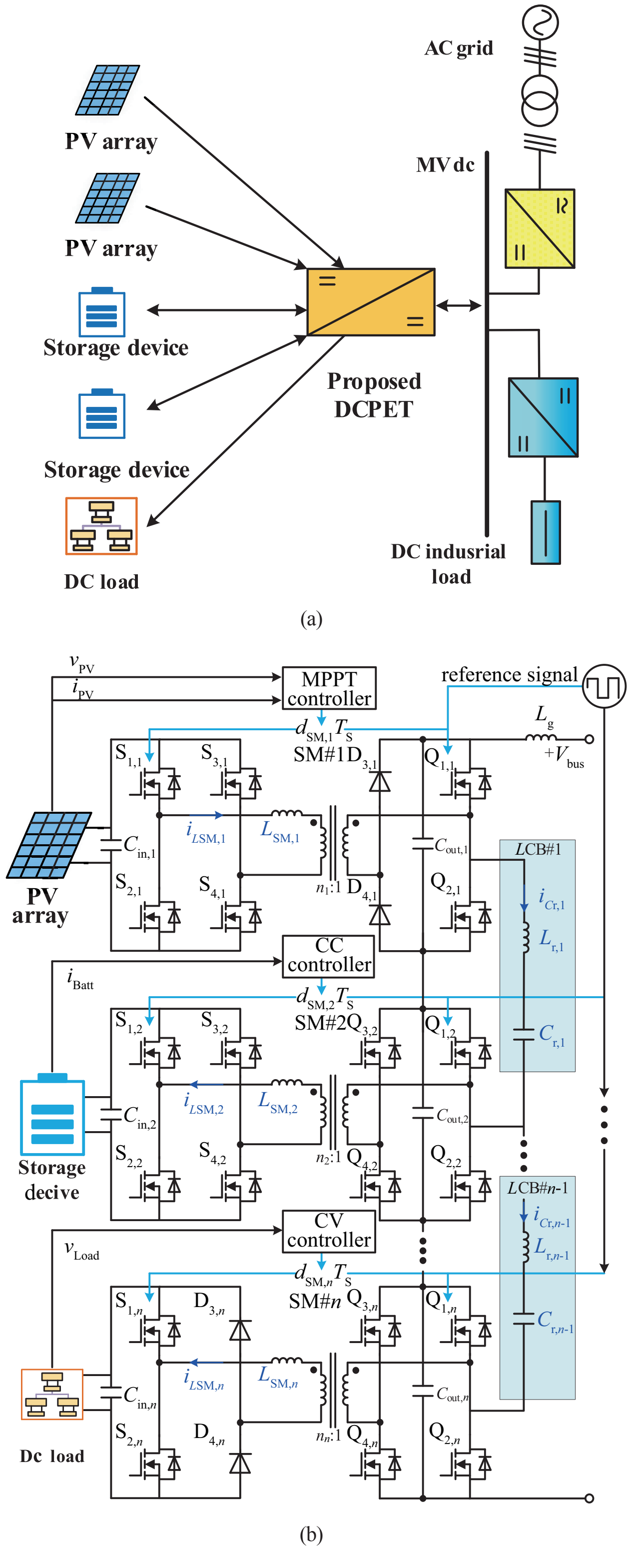
Digital Object Identifier 10.24295/CPSSTPEA.2023.00047

LVdc substructure realizes power conversion, long-distance transmission capability and flexible power control, so it is also called the dc power electronic transformer (DCPET).

For the case where the MVdc voltage level is not very high, Ref. [11] proposes a medium-frequency PET to connect the MVdc and LVdc buses. When the voltage level of MVdc is higher than 10 kV, the PET based on input-parallel output-series (IPOS) structure generally adopts multiple dc-dc converter modules to establish the bus voltage level, which can balance power flows, regulate bus voltages and has good modular characteristics [12]. An extended-phase-shift control strategy applied for the DAB-based DCPET has been proposed in [13], [14] to diminish the backflow power and peak current of each submodule (SM). A hybrid input-series output-parallel (ISOP) PET structure is proposed in [15]–[17] to realize higher conversion efficiency and voltage power regulation. When a short-circuit fault occurs at MVdc bus of the ISOP converter, Ref. [18] proposes a switched-capacitor-based PET to solve the large discharge current. However, these topologies still require extra LVdc converters to build connections between LVdc bus and dc units (e.g., storage devices, PV arrays and dc loads). Besides, when the dc units or LVdc bus occurs short-circuit fault, the system will stop working in order to maintain the safety of components in the converter system.

In [19], the basic theoretical concept of the MVdc integration interface for multiple distributed photovoltaics was proposed, and the input-independent output-series (IIOS) architecture can be used to directly connect PV solar energy to the MVdc bus [20]–[23]. Compared with IIOS structure type, the additional LVdc converters in ISOP type increases the power consumption and the number of active switches [21]. However, in IIOS structure, the different power of input ports will lead to a deviation in the output voltage between SMs. Then, the output power of each SM will be different due to the voltage imbalance. To address this issue, Zhuang et al. [22] proposes the adjacent secondary-side switches have phase shifts to deliver the unbalance power, which requires more regulators. In [23], [24], another method referred to as the series resonant LC branch was utilized to solve the problem without the complex control method. However, all input ports in [20]–[24] only connect the PV arrays is compromised when other distributed dc units need to transfer power.

To address the above issue, this paper proposes a modular multiport IIOS dc-dc converter, which can act as a DCPET for the directly MVdc integration interface of multiple dc units, as shown in Fig. 2. In the proposed converter architecture, the distributed dc units can directly connect to MVdc bus only through the proposed DCPET without extra LVdc bus and LVdc converters. Meanwhile, the corresponding series resonant LC branches are inserted between the adjacent SMs to transfer the differential power and maintain the same voltage between adjacent output capacitors. Finally, the configuration of the converter and operation principle analysis is presented in this paper, which has been verified by both simulation and experiment results.



(a)

(b)

Fig. 2. (a) The proposed DC distribution network with DCPET. (b) Structure of proposed multiport modular DCPET.

II. TOPOLOGY DESCRIPTION AND OPERATING PRINCIPLE

A. Topology Description

As shown in Fig. 2, the proposed IIOS converter contains both semi-dual-active-bridge (SDAB) and dual-active-bridge (DAB) SM converters. Considering the cost and the unidirectional power transmission of PV arrays and dc loads, the SM output port of PV arrays and the SM input port of dc loads adopt semi-active structure, as shown in Fig. 2(b), respectively. Because the storage devices need to be charged and discharged, so DAB SMs are selected as the first choice. To reduce the complexity and cost of control scheme, single phase shift (SPS) modulation is applied for the proposed converter. In Fig. 2(b), the drive signals of $S_{1,n}$ and $S_{4,n}$ in DAB modules are the same, as well as for $S_{2,n}$ and $S_{3,n}$. $S_{1,n}$ (= $S_{4,n}$) and $S_{2,n}$ (= $S_{3,n}$) are complementary conducted. Complementary drive signals for secondary side switches $Q_{1,n}$ (= $Q_{4,n}$) and $Q_{2,n}$ (= $Q_{3,n}$). The duty cycle is fixed at 50% for all power switches. The drive signals of SDAB modules are similar to those of the DAB modules, except that the $S_{3,n}$, $S_{4,n}$ and $Q_{3,n}$, $Q_{4,n}$ are replaced by diodes $D_{3,n}$ and $D_{4,n}$, so that the control method remains the same. All switches in the SMs can realize zero-voltage-switching (ZVS), which can reduce the switching power loss and improve the conversion efficiency.

B. Operating Principle

Fig. 3 shows the typical waveforms of SDAB modules and its equivalent circuit diagrams in different operation modes. As can be seen in Fig. 3(a), the circuit waveforms are symmetrical in one complete switching cycle, and it has six working modes. Therefore, the analysis process of the first three working modes is presented in Fig. 3(b). In Mode 1, $v_{L\mathrm{SM},k}$ is equal to $V_{\mathrm{PV},k} + V_{\mathrm{SM},k}$, $i_{L\mathrm{SM},k}$ begins to increase until the end of Mode 1. When the current of $i_{L\mathrm{SM},k}$ reaches zero and its direction occurs change, $D_{3,k}$ and $Q_{1,k}$ will be turn on in Mode 2. Since the upper arm is conducting in the meantime, there is no current flow through $C_{\mathrm{out},k}$. $v_{L\mathrm{SM},k}$ is equal to $V_{\mathrm{PV},k}$, and $i_{L\mathrm{SM},k}$ continues to increase. In Mode 3, $Q_{2,k}$ can be turned off, $D_{4,k}$ and $Q_{1,k}$ flow through currents. $v_{L\mathrm{SM},k}$ equals to $V_{\mathrm{PV},k}-V_{\mathrm{SM},k}$, and $i_{L\mathrm{SM},k}$ remains unchanged. In this mode, $C_{\mathrm{out},k}$ starts charging and the PV power transfers to MVdc bus by the SDAB modules.

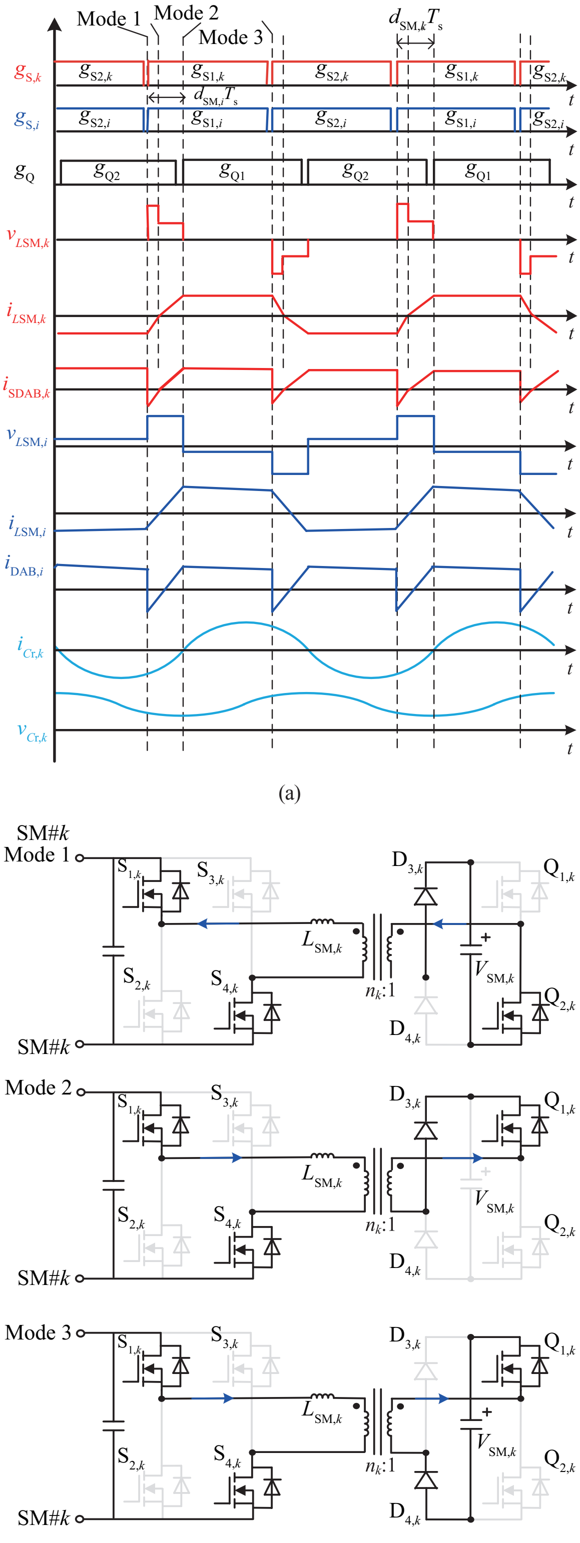
The waveforms of $i_{\mathrm{SDAB},k}$ and $i_{\mathrm{DAB},i}$ are shown in Fig. 3(a), respectively. Their average values in one half cycle can be derived as

$$\begin{cases} I_{\mathrm{SDAB},k} = \dfrac{2}{T_s}\displaystyle\int_0^{T_s/2} i_{L\mathrm{SM},k}\,\mathrm{d}t = \dfrac{2V_{\mathrm{SM},k}d_{\mathrm{SM},k}}{3nf_s L_{\mathrm{SM},k}}\left(1-\dfrac{5}{3}d_{\mathrm{SM},k}\right) \\ I_{\mathrm{DAB},i} = \dfrac{2}{T_s}\displaystyle\int_0^{T_s/2} i_{L\mathrm{SM},i}\,\mathrm{d}t = \dfrac{V_{\mathrm{SM},i}d_{\mathrm{SM},i}}{f_s L_{\mathrm{SM},i}}\left(1-2d_{\mathrm{SM},i}\right) \end{cases} \tag{1}$$

Then the expressions of power transferred by SDAB and DAB modules can be obtained as

$$\begin{cases} P_{\mathrm{SDAB},k} = V_{\mathrm{SDAB},k}I_{\mathrm{SDAB},k} = \dfrac{2V_{\mathrm{SDAB},k}V_{\mathrm{SM},k}d_{\mathrm{SM},k}}{3f_s L_{\mathrm{SM},k}}\left(1-\dfrac{5}{3}d_{\mathrm{SM},k}\right) \\ P_{\mathrm{DAB},i} = V_{\mathrm{DAB},i}I_{\mathrm{DAB},i} = \dfrac{V_{\mathrm{DAB},i}V_{\mathrm{SM},i}d_{\mathrm{SM},i}}{f_s L_{\mathrm{SM},i}}\left(1-2d_{\mathrm{SM},i}\right) \end{cases} \tag{2}$$

According to (2), if SDAB and DAB modules desire to output maximum power, d_{SM} should satisfy (3) in the following.



(a)

(b)

Fig. 3. (a) Typical waveforms of SDAB and DAB in the proposed converter. (b) Equivalent circuits of different operating modes in SDAB module.

$$\begin{cases} P_{\mathrm{SDAB,max}} = \dfrac{V_{\mathrm{SDAB}}V_{\mathrm{SM}}}{10f_s L_{\mathrm{SM}}}, d_{\mathrm{SM,SDAB}} = 0.3 \\ P_{\mathrm{DAB,max}} = \dfrac{V_{\mathrm{DAB}}V_{\mathrm{SM}}}{8f_s L_{\mathrm{SM}}}, d_{\mathrm{SM,DAB}} = 0.25 \end{cases} \tag{3}$$

C. Power Transmission of LC Branch

It can be seen from Fig. 2 that the LC branches are inserted to transfer power between the adjacent SMs, so the power of the *k*th LC branch ($P_{\mathrm{r},k}$) should satisfy

$$\left(\sum_{i=1}^{k} P_{\mathrm{SM},i} - P_{\mathrm{r},k}\right)/k = \left(\sum_{i=1}^{k} P_{\mathrm{SM},i} + P_{\mathrm{r},k}\right)/(N-k) \tag{4}$$

where $P_{\mathrm{SM},i}$ denotes the power of the *i*th SM, and N represents the number of all SMs. Then, it can be derived that

$$P_{\mathrm{r},k} = \frac{(N-k)}{N}\sum_{i=1}^{k} P_{\mathrm{SM},i} - \frac{k}{N}\sum_{i=k+1}^{N} P_{\mathrm{SM},i} \tag{5}$$

According to (3), for convenience of analysis, the rated input power of each module can be estimated by $P_{\mathrm{SM},i} = P_{\mathrm{SDAB}}$. When the SM#*k*+1–SM#N all connect the dc loads, the maximum value expression of $P_{\mathrm{r},k}$ can be calculated by

$$P_{\mathrm{r},k} = \frac{2(N-k)k}{N} P_{\mathrm{SDAB,max}} \tag{6}$$

Taking the differential form of $P_{\mathrm{r},k}$ with respect to *k*, it can be derived that

$$\mathrm{d}\left(P_{\mathrm{r},k}\right) = \frac{2(N-2k)}{N} P_{\mathrm{SDAB,max}}\,\mathrm{d}(k) \tag{7}$$

Then, as can be seen from (7), the maximum value of $P_{\mathrm{r},k}$ appears when $k = N/2$. Therefore, the maximum power of the *k*th LC branch can be obtained as

$$P_{\mathrm{r},k,\max} = \frac{2}{N} P_{\mathrm{SDAB,max}} \tag{8}$$

D. Control Strategy of LC Branch

In order to realize modular standard design, the output voltage of all SMs need to be made consistent through control strategies. The secondary side switches use 50% duty cycle open-loop control scheme to produce identical square wave voltages at both terminals of the serial LC branches, thus having the function of an ideal transformer. The series LC resonant power balance unit embedded in this manner can achieve 1:1 transformer conversion, so as to realize the same output capacitor voltage between adjacent SMs. The resonant current and voltage waveforms of C_r are shown in Fig. 3(a) on the basis of theoretical analysis. Based on Fig. 4, the detailed analysis of the voltage balancing capability and power delivery mechanism is described as follows.

As can be seen Fig. 4(a), the LC branch#*k* (LCB#*k*) connected the bridge legs of SM#*k* and SM#*k*+1, so the terminal voltages of $\mathrm{Q}_{4,k}$ and $\mathrm{Q}_{3,k+1}$ act as the ac-terminal voltages of LCB#*k*. The ac-component equivalent model of LCB#*k* with various power transmission directions is constructed, as shown in Fig. 4(b) and (c), respectively. When the driving signals of $\mathrm{Q}_{3,k}$ and $\mathrm{Q}_{3,k+1}$ arrive, the power flow from $C_{\mathrm{out},k}$ to $C_{\mathrm{out},k+1}$. $v_{\mathrm{Q4},k,\mathrm{ac}}$ and $v_{\mathrm{Q3},k+1,\mathrm{ac}}$ represent the ac-component of $v_{\mathrm{Q4},k}$ and $v_{\mathrm{Q3},k+1}$, respectively, as presented in Fig. 4(b). In Fig. 4(c), $\mathrm{Q}_{4,k}$ and $\mathrm{Q}_{4,k+1}$ are turned on and the power starts to transfer from $C_{\mathrm{out},k+1}$ to $C_{\mathrm{out},k}$, where $v_{\mathrm{Q3},k+1,\mathrm{ac}}$ and $v_{\mathrm{Q4},k,\mathrm{ac}}$ represent the ac-component of $v_{\mathrm{Q3},k+1}$ and $v_{\mathrm{Q4},k}$, respectively. Due to the resonant capacitor dealing with the dc voltage components of $Q_{4,k}$ and $Q_{3,k+1}$, so the amplitudes of $v_{\mathrm{Q4},k,\mathrm{ac}}$ and $v_{\mathrm{Q3},k+1,\mathrm{ac}}$ are $V_{\mathrm{SM},k}/2$ and $V_{\mathrm{SM},k+1}/2$. R_{eq} represents the equivalent resistance of the imbalance power $P_{\mathrm{r},k}$ at the ac side, it can be expressed as

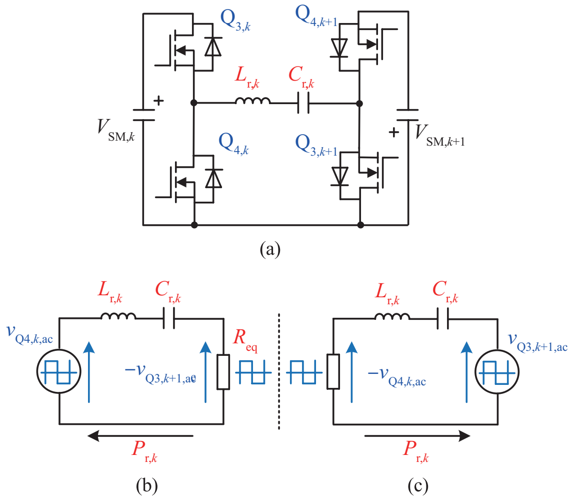


Fig. 4. Equivalent circuit and power flow model of LCB#*k*. (a) Equivalent circuit, (b) forward power flow model and (c) reversed power flow model.

$$R_{\mathrm{eq}} = \frac{2V_{\mathrm{SM},k}^2}{\pi^2 P_{\mathrm{r},k}} \tag{9}$$

Therefore, based on the equivalent model of series resonant circuit, the conversion gain M_r expression of output capacitor voltage between adjacent SMs can be obtained as

$$M_\mathrm{r} = \frac{V_{\mathrm{SM},k}}{V_{\mathrm{SM},k+1}} = \frac{1}{\sqrt{1+Q^2\left(f_\mathrm{s}/f_{\mathrm{r},k} - f_{\mathrm{r},k}/f_\mathrm{s}\right)^2}} \tag{10}$$

$$f_\mathrm{r} = 1\big/2\pi\sqrt{L_{\mathrm{r},k}/C_{\mathrm{r},k}}\ ,\ Q = \sqrt{L_{\mathrm{r},k}/C_{\mathrm{r},k}}\big/R_{\mathrm{eq}} \tag{11}$$

where f_s is the switching frequency, $f_{\mathrm{r},k}$ is the resonant frequency of LC branch, and Q represents the quality factor of resonant circuit. It can be found from (10) and (11) that the voltage balance effect is mainly affected by resonance parameters, switching frequency and imbalanced power. Based on the voltage gain expression obtained in (10), when Q is taken as certain values, the changes of voltage gain M_r versus $f_\mathrm{s}/f_{\mathrm{r},k}$ are shown in Fig. 5. As can be seen from Fig. 5, when $f_\mathrm{s}/f_{\mathrm{r},k}$ is taken as certain values, it can be found that the voltage gain M_r increases as Q decreases. Therefore, Q should be properly designed small enough.

E. Control Strategy of SM and Operation States

For the proposed modular IIOS converter, different dc units have different controllers. In Fig. 6, the PV arrays adopt maximum power point control (MPPT) strategy, and the output of the controller is denoted as $d_{\mathrm{SM,PV}}$. The storage devices adopt constant current (CC) control scheme, and the output of this controller is denoted as $d_{\mathrm{SM,Batt}}$. The dc loads adopt constant voltage (CV) control scheme, and the output of the controller is denoted as $d_{\mathrm{SM,Load}}$. Moreover, in order to guarantee the MVdc

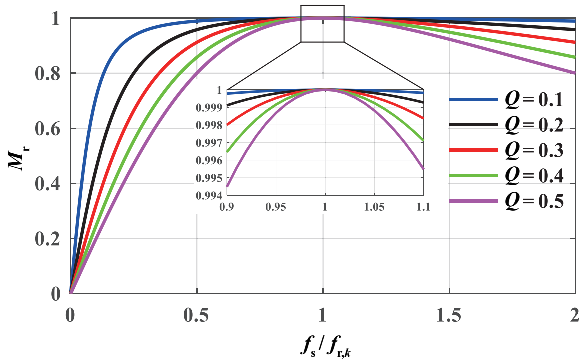
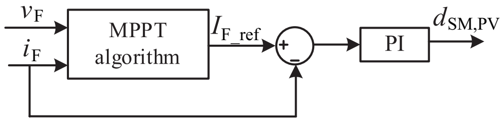
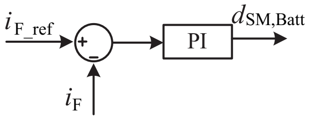


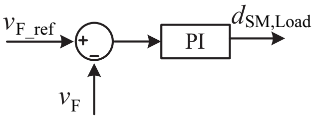
Fig. 5. Conversion gain of LCB#k when $f_{r,k}$ deviates from f_s.



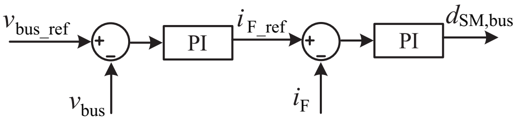
(a) Maximum power point control



(b) Constant current control



(c) Constant voltage control



(d) Constant bus voltage control

Fig. 6. The block diagrams of control strategy. (a) MPPT control, (b) CC control, (c) CV control and (d) CBV control.

bus voltage constant after the IIOS converter is disconnected from MVdc bus, a constant bus voltage (CBV) control strategy is also designed for storage devices and PV arrays, and the output of this controller is denoted as $d_{SM,bus}$.

Fig. 7 shows the six main operating states of the proposed three-SM DCPET, where SM#1 is connected to PV array, SM#2 is connected to storage device and SM#3 connects a dc load. When the DCPET is connected to MVdc grid, the storage device does not participate in system operation as a backup power supply. When the DCPET is disconnected from grid, the PV array and storage device jointly work together to maintain the MVdc bus voltage and SM output power balance. Defining P_{PV} as the power of the PV array, P_{Batt} as the power of the storage device, P_{Load} as the power of dc load and P_{Grid} as the dc grid power. The operating states can be described as:

State A: $P_{PV} = P_{Load} + P_{Grid}$. SM#1 uses MPPT control method to transmit power to SM#3, and its excess power is transferred to the MVdc grid. While, SM#2 is disconnected.

State B: $P_{PV} + P_{Grid} = P_{Load}$. SM#1 maintains the MPPT control unchanged. And the system requires MVdc grid to supplement the appropriate power to SM#3 as the dc load power increases or the PV array decreases due to external conditions.

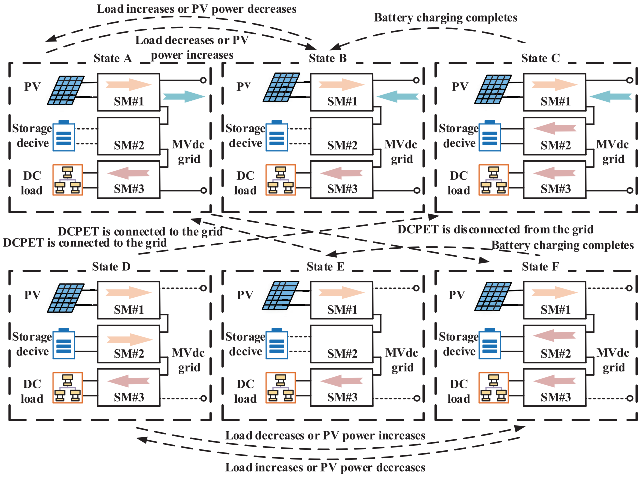


Fig. 7. The six main working states of the proposed three-SM MDCPET.

State C: $P_{PV} + P_{Grid} = P_{Load} + P_{Batt}$. SM#1 and MVdc grid supply power to both SM#2 and SM#3, while SM#1 is still controlled by MPPT control and SM#2 is controlled by cc control strategy. When the storage device is fully charged and disconnected from the interface, operating state C switches to state B.

State D: $P_{PV} + P_{Batt} = P_{Load}$. DCPET is disconnected from the MVdc grid, and the power in DCPET is transmitted among various SMs while the MVdc bus voltage still remains constant. SM#2 acts as a bridge to control the power balance. When the power generated by SM#1 is insufficient to maintain the normal operation of SM#3, SM#2 is discharged to provide balanced power. Then, SM#1 continues to be controlled by MPPT, SM#2 is controlled by CBV. When the DCPET is connected to the MVdc grid, SM#2 needs to charge the storage device, thus SM#2 switches from CBV control to CC control. And the operating state D switches to state C.

State E: $P_{PV} = P_{Load}$. The proposed DCPET is disconnected from the MVdc grid, the storage device is disconnected after it has been fully charged, the output power of SM#1 only meets SM#3, therefore SM#1 uses CBV control instead of MPPT control to maintain the CBV. When the DCPET is connected to the MVdc grid, state E switches to state A.

State F: $P_{PV} = P_{Batt} + P_{Load}$. SM#1 output power reaches maximum value, the load port is connected to a purely resistive load and the excess power is charged to the storage device. Operating state D will change to state F. SM#1 uses MPPT control to achieve maximum output power, the bus voltage is maintained by SM#2 under CBV control strategy. After storage device has been fully charged, state F switches to state E.

III. PARAMETER DESIGN GUIDELINE

A. SM Leakage Inductance Design

The transformer leakage inductance L_{SM} is the key SM parameter, and its value determines the power-transmission

TABLE I
PAEAMETERS FOR SIMULATION AND EXPERIMENTS

Parameters	Simulation	Experiment
PV array/DC sources parameters		
Open circuit voltage	36.3 V	--
Voltage at MPP	31 V	--
Current at MPP	6.6 A	--
Maximum solar power of one single PV subarray	204.6 W	--
No. of series module	13	--
No. of parallel module	6	--
Nominal voltage	403 V	48 V
Rate power	16 kW	288 W
Battery parameters		
Cut off voltage	276 V	--
Fully charged voltage	428 V	50 V
Rated capacity	40 AH	16 AH
Battery response time	30 s	--
Loads parameters		
Resistor	10 Ω, 10 Ω	12 Ω, 6 Ω
Nominal voltage	400 V	48 V
Rated power	16 kW	384 W
SM parameters		
Switching frequency (f_s)	20 kHz	10 kHz
Leakage inductance (L_{SM})	10 μH	40 μH
Turn ratio of transformer	1:1	1:1
LCB parameters		
Reasonant inductance (L_r)	6.5 μH	13 μH
Reasonant capacitance (C_r)	10 μF	20 μF

ability of the SMs. The output maximum power of SDAB and DAB modules is obtained by (3), so it can be known that the range of L_{SM} can be derived as

$$\begin{cases} L_{\mathrm{SM,\,SDAB}} \leqslant \dfrac{V_{\mathrm{SDAB}}V_{\mathrm{SM}}}{10 f_{\mathrm{s}} P_{\mathrm{SDAB,max}}} \\ L_{\mathrm{SM,\,DAB}} \leqslant \dfrac{V_{\mathrm{DAB}}V_{\mathrm{SM}}}{8 f_{\mathrm{s}} P_{\mathrm{DAB,max}}} \end{cases} \tag{12}$$

In order to realize the non-error balance of SM output voltage, based on the analysis in Section II, the resonant frequency f_{r} should be set close to the switching frequency f_{s},

$$f_{\mathrm{r}} = 1\big/2\pi\sqrt{L_{\mathrm{r},k}/C_{\mathrm{r},k}} \approx f_{\mathrm{s}} \tag{13}$$

Then by substituting (8), (9) and (11) into (13), the resonant frequency f_{r} is calculated as

$$f_{\mathrm{r}} = \frac{1}{2\pi\sqrt{L_{\mathrm{r},k}/C_{\mathrm{r},k}}} = \frac{\pi P_{\mathrm{r},k}}{4QV_{\mathrm{SM},k}} \leqslant \frac{\pi P_{\mathrm{r},k,\max}}{4QV_{\mathrm{SM},k}} \tag{14}$$

In addition, when the operating frequency deviates from resonant frequency of LC branch, the characteristic impedance Z_{r} should be large, then it has high harmonic suppression ability. Based on above analysis, the selected resonant inductor $L_{\mathrm{r},k}$ and resonant capacitor $C_{\mathrm{r},k}$ should ensure that (14) is established.

IV. SIMULATION AND EXPERIMENTAL VEVRIFICATIONS

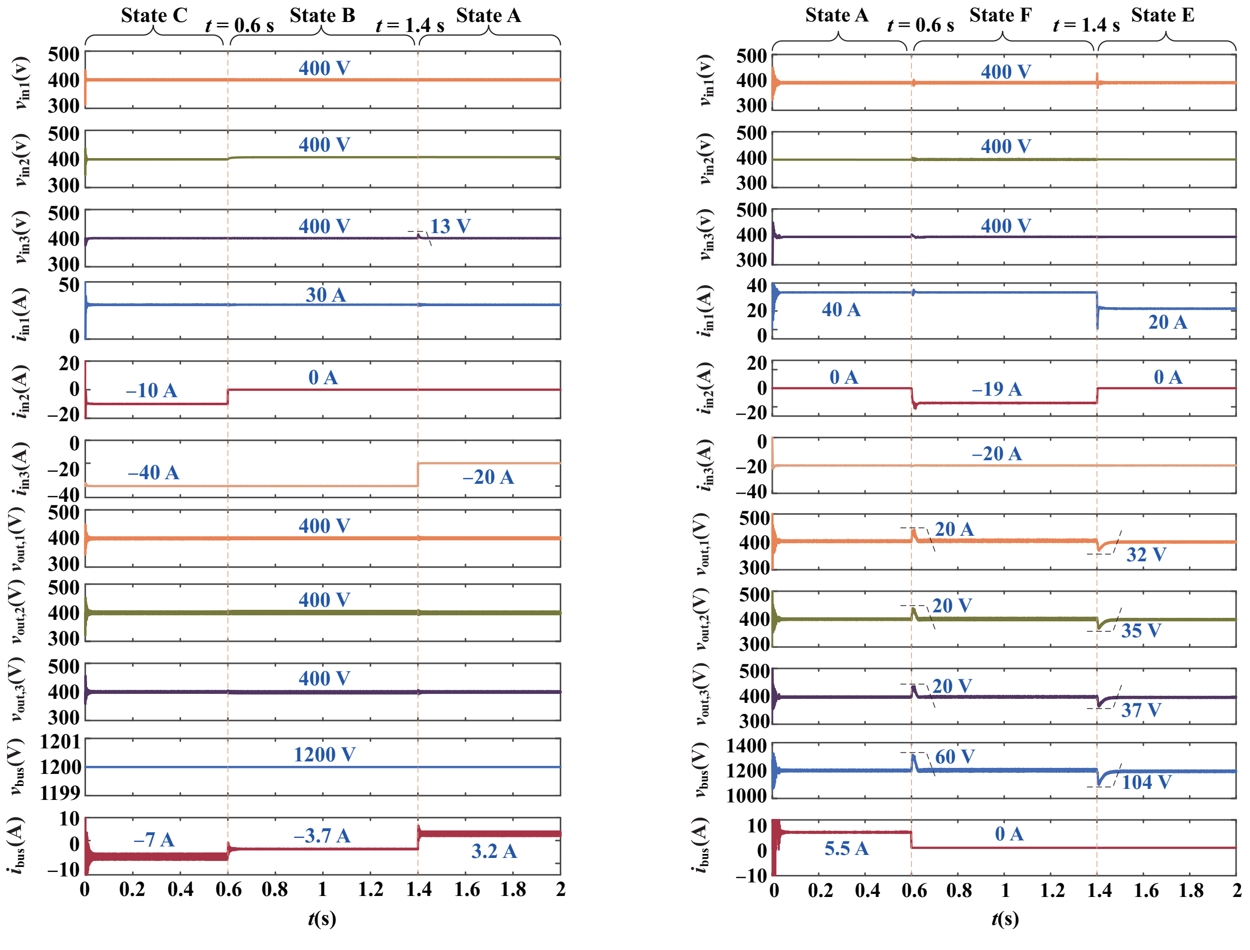
A. Simulation Results

Based on Fig. 2, the three-SM circuit simulation model of the proposed DCPET is built on the MATLAB/Simulink platform. The simulation step is set at 100 ns and the simulation parameters of the DCPET are listed as in Table I.

Fig. 8(a) shows the simulation results when DCPET works in on-grid. When $0 < t < 0.6$ s, the DCPET works in state C, the input current i_{in},1 of SM#1 is 30 A, the output current ($-i_{\mathrm{in},2}$) of SM#2 is 10 A, and the output current ($-i_{\mathrm{in},3}$) of SM#3 is 40 A. The power of SM#1 is about 30 A × 400 V = 12 kW, the power of the storage device is about 10 A × 400 V = 4 kW, and the power of SM#3 is about 40 A × 400 V = 16 kW. The power of the grid is 12 kW − 4 kW − 16 kW = −8 kW, so the current of the grid should be 8 kW/1200 V = −6.7 A. Therefore, the simulation result of the grid current ibus is about −6.7 A. When $t = 1.4$ s, the storage device does not work. At this time, the current of the grid should be −4 kW/1200 V = −3.7 A, and the DCPET is switched from state C to B. When $t = 1.4$ s, the dc load current changes to 20 A, and the power of dc load is less than the power of SM#1. At this time, the grid power is 12 kW − 8 kW = 4 kW and the grid current should be 4 kW/1200 V = 3.3 A. Therefore, the additional power is transferred to MVdc grid, the grid current is changed from −3.7 A to 3.2 A, and DCPET is switched from state B to A.

Fig. 8(b) shows the simulation results when the proposed DCPET works in off-grid. When $0 < t < 0.6$ s, the DCPET works in state A, the input current of SM#1 is 40 A, SM#2 is disconnected, and the output current of SM#3 is 20 A. The input power of PV is about 40 A × 400 V = 16 kW, and the power of the dc load is about 20 A × 400 V = 8 kW. The power of the grid is 16 kW − 8 kW = 8 kW, so the current of the grid is about 8 kW/1200 V = 6.7 A. Therefore, with the power loss considered, SM#1 provides 5.5 A current to the grid. When $t = 0.6$ s, the storage device is connected and the grid is disconnected. The power of the storage device is about 19 A × 400 V = 7.6 kW. At this time, SM#1 supplies energy to SM#2 and SM#3, and the DCPET is switched from state A to state F. When $t = 1.4$ s, the storage device is disconnected, the PV array current changes to 20 A, SM#1 is responsible for transmitting power to SM#3, and the DCPET is switched from state F→E.

From these simulation results in Fig. 8, it can be found that when the working state changes, the input and output port voltage v_{in} and v_{out} of each SM is still 400 V, and the bus voltage v_{bus} is maintained at about 1200 V. Considering the power loss, the power of each SM is conserved in each working state. When the working state changes or DCPET is



(a) (b)

Fig. 8. Simulation results when the proposed DCPET works in steady state. (a) States C→B→A. (b) States A→F→E.

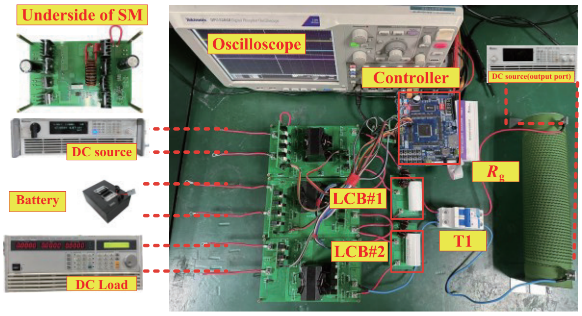


Fig. 9. Down-scaled experimental hardware prototype.

TABLE II

Downscaled Experimental Parameters

Equipment		Specification
(1) PV source	A dc source with constant voltage	Chroma 62180H-1800S
(2) Storage	Lithium-ion battery	44.4V/22Ah/20C
(3) Load	A dc electronic load	Chroma63202
(4) Dc bus	A dc source with constant voltage	Chroma 62150H-600S Resistor: RXG20-1000W-50R

disconnected from the dc grid, the voltage of the MVdc grid and all input ports can still remain stable due to the adjustment of the control strategies of the PV array and the storage device. Therefore, from the above simulation results it can be verified that the proposed DCPET can improve the energy utilization rate and the reliability of the whole converter system.

B. Experimental Verification

To verify the proposed DCPET, as shown in Fig. 9, a down-scaled experimental prototype with three SMs and a dc bus 144 V was built for demonstrating the theoretical analysis. The detailed parameters of the prototype are listed in Table I and the other specifications can be found in Table II. The prototype mainly includes a dc source (Chroma62180H-1800S), all SM converters and LC power balance units, a DSP controller (TMS320F28335), a CV load (Chroma63202), and an output dc source (Chroma62150H-600S). Due to the limitation of experimental conditions, SM#1 input port is connected to a 48 V dc source in the experiment. The MPPT control is simplified to constant power control, and a 144 V CV dc source is used to simulate the dc bus. A resistor R_g can be adopted to

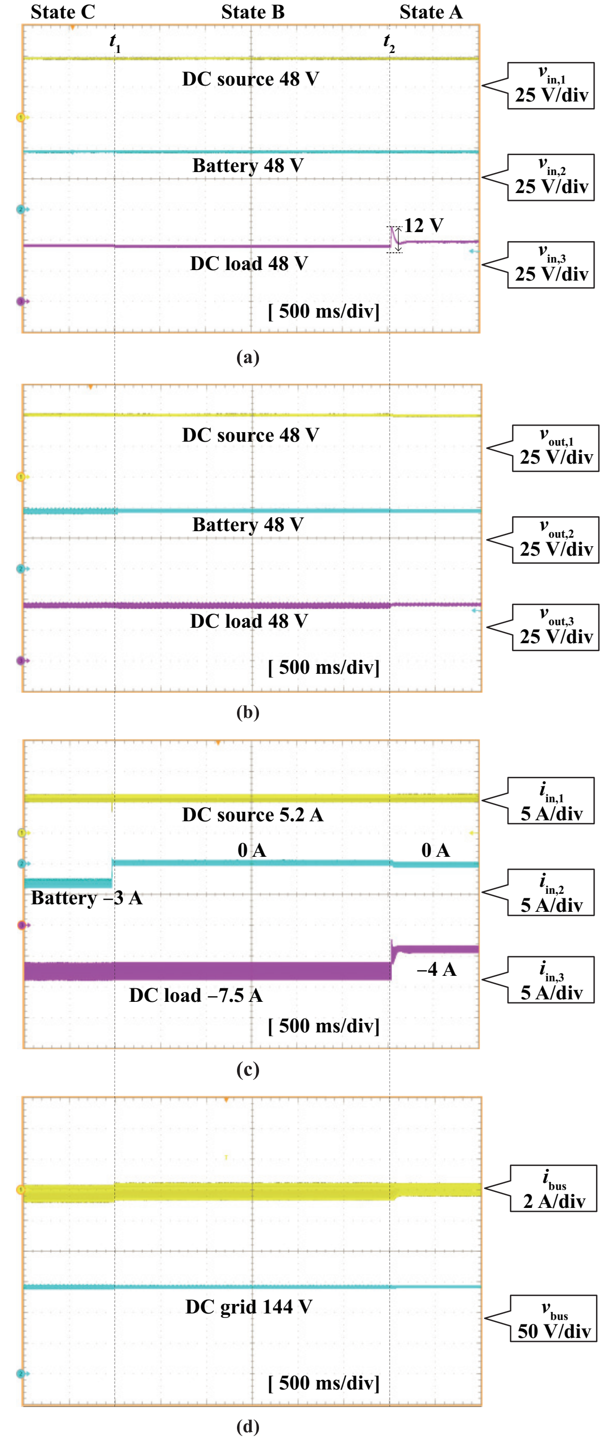


Fig. 10. Experimental waveforms when the DCPET works in state C→B→A. The dc grid sends out the balance power in state C and B and absorbs the excess power in state A. (a)$v_{\text{in},1}$, $v_{\text{in},2}$, and $v_{\text{in},3}$. (b)$v_{\text{out},1}$, $v_{\text{out},2}$, and $v_{\text{out},3}$. (c)$i_{\text{in},1}$, $i_{\text{in},2}$, and $i_{\text{in},3}$. (d)i_{bus} and v_{bus}.

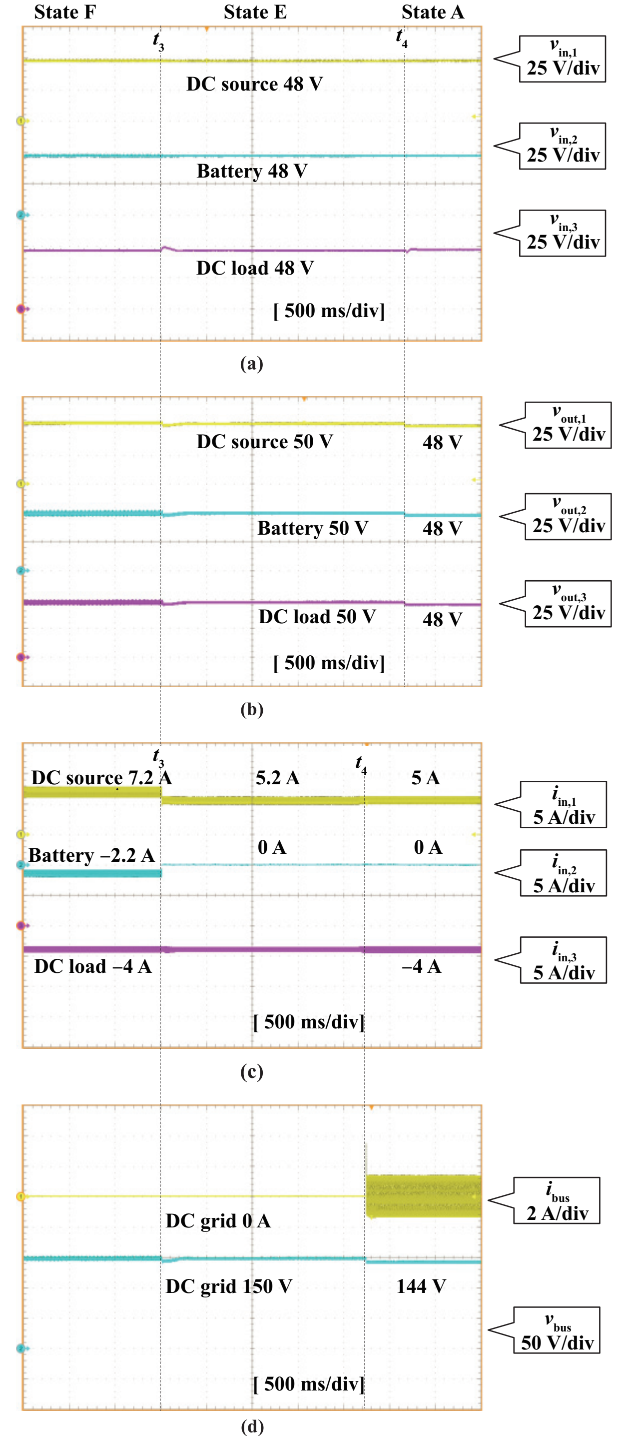


Fig. 11. Experimental results when the DCPET works in state F→E→A.The PV array or battery provides the balance of power in state F and E.The dc grid voltage can be kept stable when the working state is changed.(a)$v_{\text{in},1}$, $v_{\text{in},2}$, and $v_{\text{in},3}$. (b)$v_{\text{out},1}$, $v_{\text{out},2}$, and $v_{\text{out},3}$. (c)$i_{\text{in},1}$, $i_{\text{in},2}$, and $i_{\text{in},3}$. (d)i_{bus} and v_{bus}.

consume the power in order to guarantee that the dc source can output power.

Fig.10 shows the experimental results when the proposed DCPET works in state C, state B, and state A. When $t < t_1$, the DCPET works in state C, the input current of SM#1 is about 5.2 A, the output current of SM#2 is about 3 A, and the output current of SM#3 is about 7.5 A. The power of SM#1 is about 5.2 A × 48 V = 249.6 W, the power of storage device is about 3 A × 48 V = 144 W, and the power of SM#3 is about 7.5 A × 48 V = 360 W. The power of the dc grid is 249.6 W – 144 W – 360 W = –254.4 W, so the current of the grid is about – 254.4 W/144 V = –1.8 A. At t_1, the storage device is charged fully

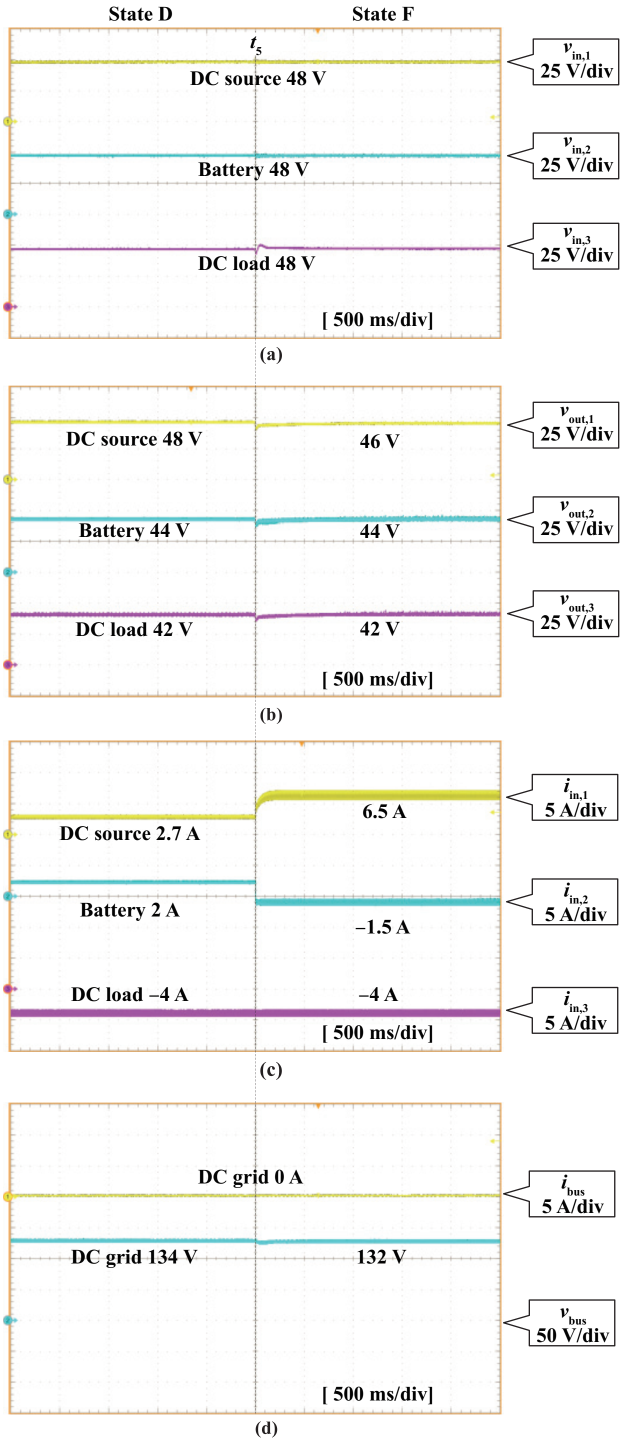


Fig. 12. Steady-state waveforms when DCPET is switched from state D to F. The bus voltage is established by the storage device in these two states.(a)$v_{in,1}$, $v_{in,2}$, and $v_{in,3}$. (b)$v_{out,1}$, $v_{out,2}$, and $v_{out,3}$. (c)$i_{in,1}$, $i_{in,2}$, and $i_{in,3}$. (d)i_{bus} and v_{bus}.

and the current of SM#2 becomes zero. But the output power of SM#1 still is satisfied with the power of the dc load, the grid current should be 110.4 W/144 V = –0.8A. At t_2, the load resistance is changed from 6 Ω to 12 Ω, the consuming power is 48 V × 4 A = 192 W. Then, the power of SM#1is larger than the dc load power, the dc grid can provide about 249.6 W – 192 W = 57.6 W power. And the measured grid input current is about 0.2 A under the consideration of parasitic parameters. Moreover, the input and output voltages of each SM can be kept stable in these three states. Therefore, the experimental results indicate that the proposed DCPET converter has good voltage balance characteristic.

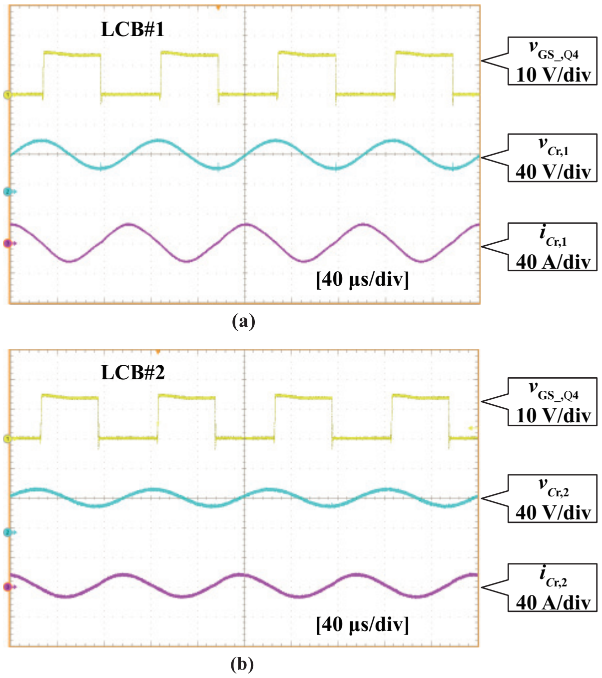
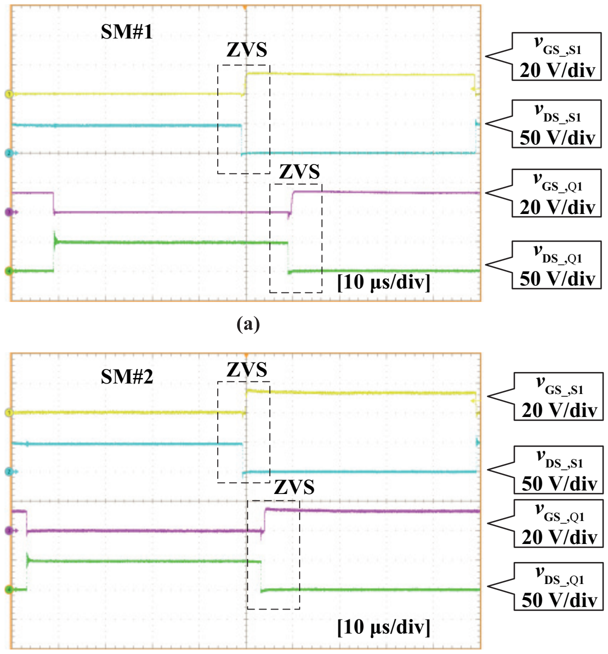


Fig. 13. Key experimental waveforms of LC branches when DCPET works in state C. (a) LCB#1 and (b) LCB#2.

When the proposed DCPET works in states F, E, and A, the corresponding experimental results are presented in Fig. 11. As can be seen from Fig. 11, the DCPET starts to work in off-grid condition. SM#1 provides about 7.2 A × 48 V = 345.6 W power. The power of SM#3 is about –4 A × 48 V = –192 W. The excess power (345.6 W – 192 W = 153.6 W) is transferred to the battery, and $i_{in,2}$ should be 153.6/48 = 3.2 A. With the power loss considered, the battery current is measured about 2A. At t_3, the storage device finished the process of charging and the power of SM#1 is larger than the power of SM#3. Therefore, the CC control of SM#1 can be switched to the constant bus control. And the current of SM#1 decreases from 7.2 A to 5.2 A. At t_4, the DCPET is connected to the dc grid due to the contactor T_1 is closed. The current of the dc grid begins to appear and its voltage is decreased from 150 V to 144 V.

Fig. 12 shows the experimental waveforms of the CV control method corresponding to state D and state F. It can be seen from Fig. 12 that the power generated from SM#1 is less than the dc load, so the battery provides 2 A × 48 V = 96 W of power to balance the bus voltage. At t_5, the current reference of SM#1 is increased to 6.5 A. Therefore, the battery starts to be charged instead of discharging in order to maintain the system power balance.

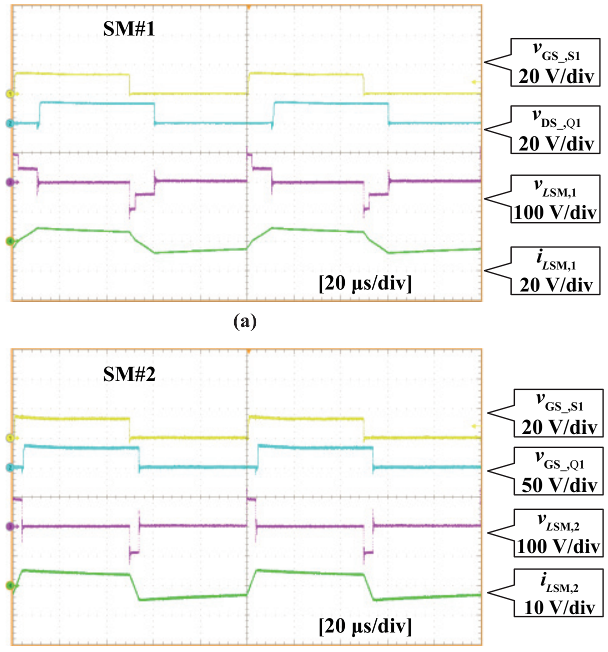
Fig. 13 shows the driving signal waveforms of switch Q_4 on secondary side bridge arm, voltage and current waveforms of resonant capacitor in these two LC branches when DCPET works in state C. Since SM#1 needs to send power to SM#2



(a)

(b)

Fig. 14. ZVS waveforms of primary and secondary side power switches of SMs. (a) SM#1 and (b) SM#2.



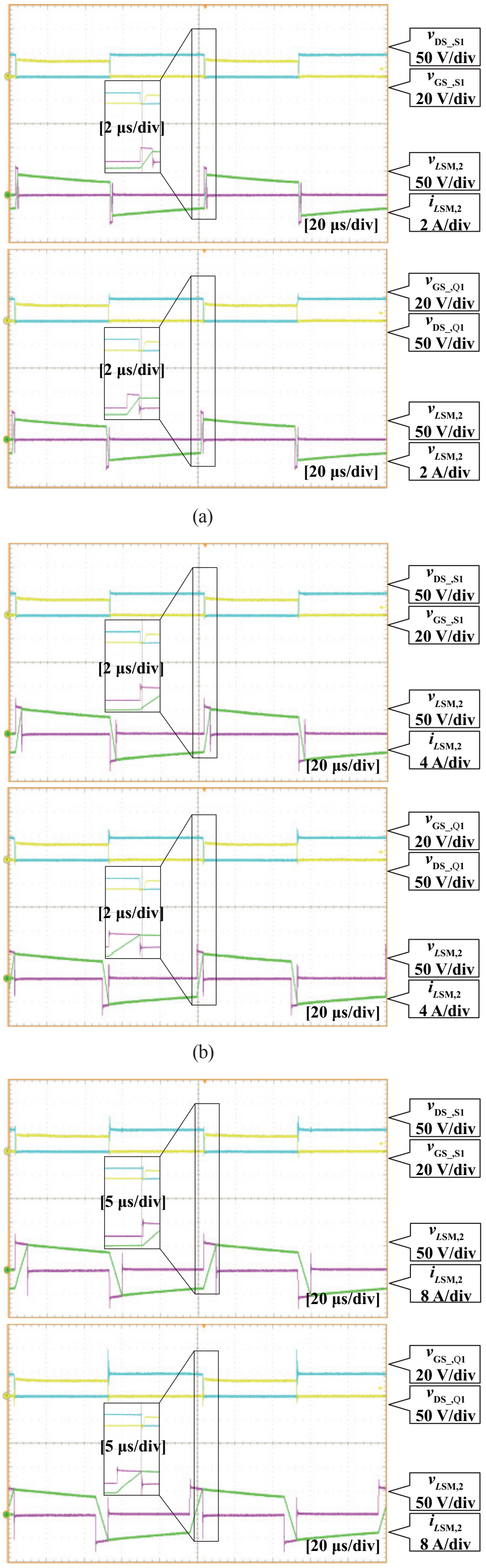
(a)

(b)

Fig. 15. Voltage and current waveforms of leakage inductor in steady state of SMs. (a) SM#1 and (b) SM#2.

and SM#3, it can be seen from the waveforms in Fig. 13 that the resonant current of LCB#1 and LCB#2 is negative when switch Q_3 is turned on.

Fig. 14 shows the driving signal voltage v_{GS} and drain-source voltage v_{DS} waveforms of switches $S_{1,1}$ and $Q_{1,1}$ in SM#1, and switches $S_{1,2}$ and $Q_{1,2}$ in SM#2. It can be seen from the waveforms in Fig. 14 that the v_{DS} of these switches have

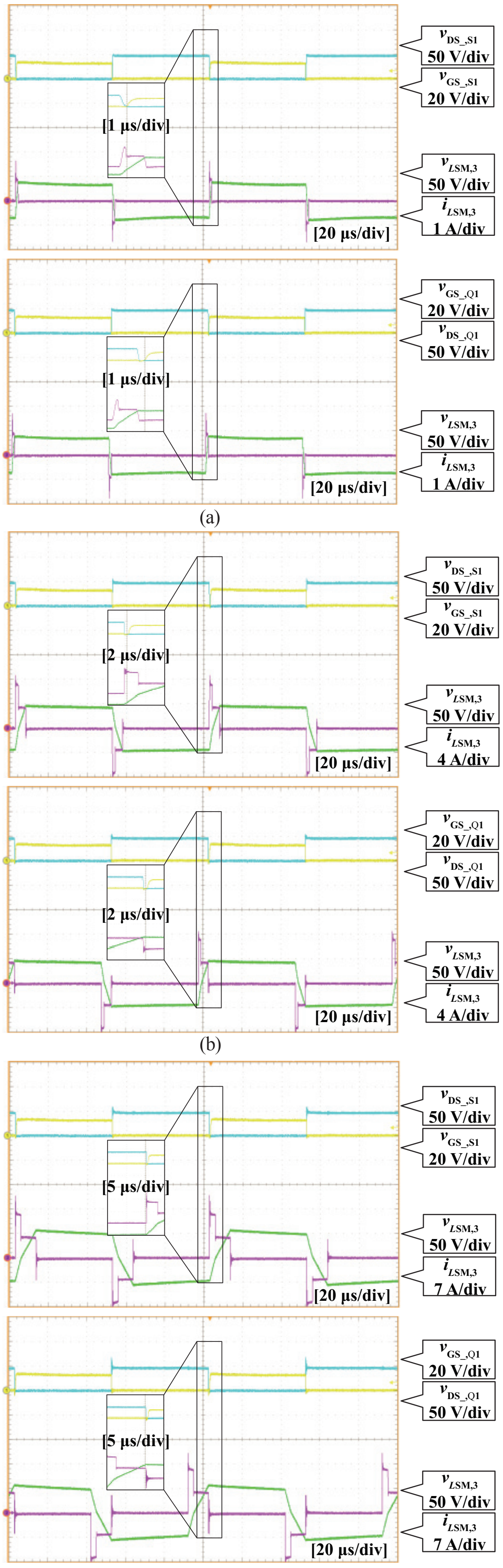


(a)

(b)

(c)

Fig. 16. ZVS waveforms of primary and secondary side power switches of DAB SM converter under different load conditions.(a) Light load (10%), (b) half load and (c) full load.



(a)

(b)

(c)

Fig. 17. ZVS waveforms of primary and secondary side power switches of SDAB SM converter under different load conditions. (a) Light load (10%), (b) half load and (c) full load.

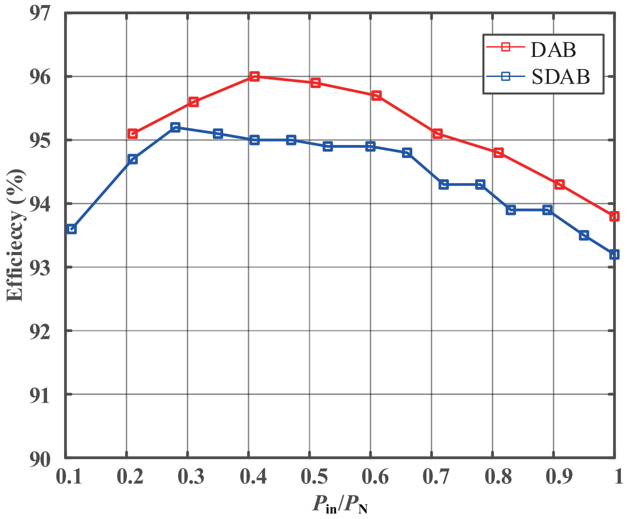


Fig. 18. The experimental efficiency of DAB and SDAB SMs under different input power conditions.

been reduced from 48 V to 0 V when v_{GS} begins to rise. Thus, the ZVS of all switches can be realized obviously. Fig. 15(a) shows the driving signal voltage v_{GS} waveforms of switches S_1 and Q_1, the leakage inductance voltage $v_{LSM,1}$ and current $i_{LSM,1}$ waveforms of the transformer when SM#1 is in steady-state operation. Fig. 15 (b) shows the driving voltage v_{GS} waveforms of switches S_1 and Q_1, the leakage inductance voltage $v_{LSM,2}$ and current $i_{LSM,2}$ waveforms of the transformer when SM#2 operates in steady state, which are also in good agreement with the simulation waveforms.

Moreover, the ZVS experimental waveforms of DAB and SDAB SM converters in the proposed modular multiport DCPET converter under different load conditions are measured and presented in Figs. 16 and 17, respectively. From these experimental waveforms in Figs. 16 and 17, it can be found that all switches on primary and secondary sides of the proposed DCPET converter can achieve zero-voltage switching within the full load range. In addition, the experimental efficiency of DAB and SDAB SM under different input power are measured and presented in Fig. 18, respectively, when they all work in the fully ZVS condition. From this figure, one can find that the experimental efficiency of each SM converter is higher than 93%, which can be further improved by using wide band-gap semiconductor devices.

V. CONCLUSION

A modular multiport DCPET converter has been proposed and analyzed in this paper, which can directly interface with multiple dc units, such as PV arrays, storage devices, and dc loads, without the requirement of extra LVdc bus or LVdc converters. Thus, the proposed method can significantly reduce system expenditure and volume. In addition, by applying the proposed control strategy and the IIOS architecture, all power switches can realize ZVS, and voltage balance can also be achieved among each SM. Therefore, the proposed DCPET converter would be suitable for the MVdc distribution network fields.

Reference

[1] Y. Wang, S. Z. Chen, Y. Wang, L. Zhu, Y. Guan, G. Zhang, L. Yang, and Y. Zhang, “A multiple modular isolated DC/DC converter with bidirectional fault handling and efficient energy conversion for DC distribution network,” in *IEEE Transactions on Power Electronics*, vol. 35, no. 11, pp. 11502–11517, Nov. 2020.

[2] J. Zhang, J. Liu, J. Yang, N. Zhao, Y. Wang, and T. Q. Zheng, “A modified DC power electronic transformer based on series connection of full-bridge converters,” in *IEEE Transactions on Power Electronics*, vol. 34, no. 3, pp. 2119–2133, Mar. 2019.

[3] F. Ruiz, M. A. Perez, J. R. Espinosa, T. Gajowik, S. Stynski, and M. Malinowski, “Surveying solid-state transformer structures and controls: Providing highly efficient and controllable power flow in distribution grids,” in *IEEE Industrial Electronics Magazine*, vol. 14, no. 1, pp. 56–70, Mar. 2020.

[4] T. Liu, X. Yang, W. Chen, Y. Li, Y. Xuan, L. Huang, and X. Hao, “Design and implementation of high efficiency control scheme of dual active bridge based 10kV/1MW solid state transformer for PV application,” in *IEEE Transactions on Power Electronics*, vol. 34, no. 5, pp. 4223–4238, May 2019.

[5] J. Huang, X. Zhang, Z. Shuai, X. Zhang, P. Wang, L. H. Koh, J. Xiao, and X. Tong, “Robust circuit parameters design for the CLLC-type DC transformer in the hybrid AC-DC microgrid,” in *IEEE Transactions on Power Electronics*, vol. 66, no. 3, pp. 1906–1918, Mar. 2019.

[6] D. Rothmund, T. Guillod, D. Bortis, and J. W. Kolar, “99% Efficient 10kV SiC-based 7kV/400V DC transformer for future data centers,” in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 2, pp. 753–767, Jun. 2019.

[7] H. Shi, H. Wen, Y. Hu, Y. Yang, and Y. Wang, “Efficiency optimization of DC solid-state transformer for photovoltaic power systems,” in *IEEE Transactions on Industrial Electronics*, vol. 67, no. 5, pp. 3583–3595, May 2020.

[8] Q. Ye, R. Mo, and H. Li, “Impedance modeling and DC bus voltage stability assessment of a solid-state-transformer-enabled hybrid AC-DC grid considering bidirectional power flow,” in *IEEE Transactions on Industrial Electronics*, vol. 67, no. 8, pp. 6531–6540, Aug. 2020.

[9] N. B. Y. Gorla, S. Kolluri, M. Chai, and S. K. Panda, “A comprehensive harmonic analysis and control strategy for improved input power quality in a cascaded modular solid state transformer,” in *IEEE Transactions on Power Electronics*, vol. 34, no. 7, pp. 6219–6232, Jul. 2019.

[10] A. Agrawal and C. S. Nalamati, “Hybrid DC-AC zonal microgrid enabled by solid-state transformer and centralized ESD integration,” in *IEEE Transactions on Industrial Electronics*, vol. 66, no. 11, pp. 9097–9107, Nov. 2019.

[11] H. Shi, H. Wen, Y. Hu, Y. Yang, and Y. Wang, “Efficiency optimization of DC solid-state transformer for photovoltaic power systems,” in *IEEE Transactions on Industrial Electronics*, vol. 67, no. 5, pp. 3583–3595, May 2020.

[12] T. Liu, X. Yang, W. Chen, Y. Li, Y. Xuan, L. Huang, and X. Hao, “Design and implementation of high efficiency control scheme of dual active bridge based 10kV/1MW solid state transformer for PV application,” in *IEEE Transactions on Power Electronics*, vol. 34, no. 5, pp. 4223–4238, May 2019.

[13] N. Denniston, A. M. Massoud, S. Ahmed, and P. N. Enjeti, “Multiple module high-gain high-voltage DC-DC transformers for offshore wind energy systems,” in *IEEE Transactions on Industrial Electronics*, vol. 58, no. 5, pp. 1877–1886, May 2011.

[14] H. Shi, H. Wen, J. Chen, Y. Hu, L. Jiang, G. Chen, and J. Ma, “Minimum-backflow-power scheme of DAB-based solidstate transformer with extended-phase-shift control,” in *IEEE Transactions on Industry Applications*, vol. 54, no. 4, pp. 3483–3496, Jul./Aug. 2018.

[15] Y. Sun, Z. Gao, C. Fu, C. Wu, and Z. Chen, “A hybrid modular DC solidstate transformer combining high efficiency and control flexibility,” in *IEEE Transactions on Power Electronics*, vol. 35, no. 4, pp. 3434–3449, Apr. 2020.

[16] J. Yao, W. Chen, C. Xue, Y. Yuan, and T. Wang, “An ISOP hybrid DC transformer combining multiple SRCs and DAB converters to interconnect MVDC and LVDC distribution networks,” in *IEEE Transactions on Power Electronics*, vol. 35, no. 11, pp. 11442–11452, Nov. 2020.

[17] B. Zhao, Q. Song, J. Li, and Q. Sun, “Full-process operation, control, and experiments of modular high-frequency-link DC transformer based on dual active bridge for flexible MVDC distribution: A practical tutorial,” in *IEEE Transactions on Power Electronics*, vol. 32, no. 9, pp. 6751–6766, Sept. 2017.

[18] B. Zhao, Q. Song, J. Li, W. Liu, G. Liu, and Y. Zhao, “High-frequency link DC transformer based on switched capacitor for medium-voltage DC power distribution application,” in *IEEE Transactions on Power Electronics*, vol. 31, no. 7, pp. 4766–4777, Jul. 2016.

[19] X. Li, M. Zhu, Y. Li, and X. Cai, “Cascaded MVDC integration interface for multiple DERs with enhanced wide-range operation capability: Concepts and small-signal analysis,” in *IEEE Transactions on Power Electronics*, vol. 35, no. 2, pp. 1182–1188, Feb. 2020.

[20] Y. Zhuang, F. Liu, Y. Huang, X. Zhang, and X. Zha, “A voltage-balancer-based cascaded DC-DC converter with a novel power feedforward control for the medium-voltage DC grid interface of photovoltaic systems,” in *IEEE Access*, vol. 7, pp. 178094–178107, 2019.

[21] X. Li, M. Zhu, M. Su, J. Ma, Y. Li, and X. Cai, “Input-independent and output-series connected modular DC-DC converter with intermodule power balancing units for MVdc integration of distributed PV,” in *IEEE Transactions on Power Electronics*, vol. 35, no. 2, pp. 1622–1636, Feb. 2020.

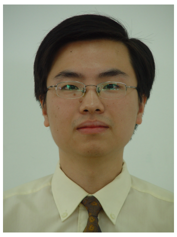
[22] Y. Zhuang F. Liu, Y. Huang, Z. Liu, S. Pan, X. Zha, and J. Jiang, “A multiport modular DC-DC converter with low-loss series LC power balancing unit for MVDC interface of distributed photovoltaics,” in *IEEE Transactions on Power Electronics*, vol. 36, no. 7, pp. 7736–7749, Jul. 2021.

[23] C. Sun, M. Zhu, X. Zhang, J. Huang, and X. Cai, “Output-series modular DC-DC converter with self-voltage balancing for integrating variable energy sources,” in *IEEE Transactions on Power Electronics*, vol. 35, no. 11, pp. 11321–11327, Nov. 2020.

[24] C. Sun, X. Zhang, J. Zhang, M. Zhu, and J. Huang, “Hybrid ISOS modular dc/dc converter constituted by resonant and non-resonant DAB modules,” in *IEEE Transactions on Industrial Electronics*, vol. 69, no. 1, pp. 1062–1069, Jan. 2021.

Xiaoquan Zhu received the Ph.D. degree in power electronics at the School of Electric Power Engineering, South China University of Technology, Guangzhou, China, in 2019. He is currently a lecturer with the College of Automation Engineering, Nanjing University of Aeronautics and Astronautics, Nanjing, China. His current research interests include renewable energy power generation systems and power electronic converters.

Jintao Hou was born in Henan, China, in 1998. He received the B.S. degree in electrical engineering from Henan Polytechnic University, China, in 2021. He is working toward the M.S. degree in power electronics from Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China. His current research interests include power electronics topologies and renewable energy systems.



Ke Jin received the Ph.D. degree in electrical engineering from Nanjing University of Aeronautics and Astronautics in 2006. From 2007 to 2008, he was a Postdoctoral Researcher with Center for Power Electronics Systems,Virginia Polytechnic Institute and State University. He is currently a Professor with College of Automation Engineering, NUAA. His main research interests include high-frequency soft-switching conversion and renewable power systems.

Bo Zhang received the Ph.D. degree in power electronics from Nanjing University of Aeronautics and Astronautics, in 1994. He is currently a Professor with School of Electric Power, South China University of Technology, Guangzhou, China. He has authored or coauthored six books in IEEE-Wiley and Springer, 450 technical papers. His research interests include modeling and control of power electronic converters and wireless power transfer applications.